

Intel® Quark™ SE Microcontroller C1000

Low Power Intel® Pentium® Processor-based x86 CPU, 32 MHz clock, 32-bit bus, Sensor Subsystem, Edge Analytics, USB, 384 kB on-die NVM + 8 kB OTP on-die NVM, Industry Standard I/O Hardware

Datasheet **February 2017**

Processor

- Intel® Pentium® Processor-based x86 ISA compatible CPU
- 32 MHz clock, 32-bit address bus
- 8 kB 2-way L1 instruction cache
- Low Latency Data Tightly Coupled Memory (TCM) Interface to on-die SRAM
- 1.49 DMIPs/MHz

Memory

- 384 kB of on-die NVM + 8 kB OTP on-die NVM
- 80 kB of on-die SRAM

Power Management

- SoC States: Active, Sleep and off
- Sensor subsystem: Sensing active, sensing wait and sensing standby
- Platform power DC-DC 1.8V, 3.3V
- Power consumption as low as
 - 250 μ A Low Power Sensing Standby
 - <1 μ A Sleep Mode (650 nA Comparator)

Clock

- 32 kHz and 32 MHz crystal oscillators
- 32 MHz Silicon oscillator
- 32 kHz RTC and AON Counters/Timers

Industry Standard I/O Hardware

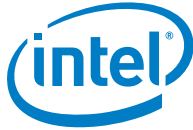
- USB 1.1 FS device
- 2 I²C master/slave with Standard, fast and fast mode plus
- 2 SPI master up to 16 MHz clock with 4 chip selects; 1 SPI Slave
- 2 UART
- 4 Timers
- 4 PWM
- 2 I2S
- 32 GPIOs + 6 GPIOs Always ON + 16 GPIOs Sensor Subsystem
- 19 Comparators

Pattern Matching Engine

- Parallel data recognition engine
- 128 vectors with 128 features per vector
- Supports *k*-Nearest Neighbors (*k*-NN) and Radial Basis Function (RBF) matching algorithms
- Recognition time proportional to the number of features
- 2 distance metrics: Lsup and Linfinity

Sensor Subsystem

- ARC EM4 DSP with floating point extensions
- 8kB L1 instruction cache, 8kB data CCM



- Tightly coupled IO to interface sensors/actuators
- 1.4 DMIPS/MHz

Sensor Subsystem Interfaces

- 2 I²C master with Standard and fast mode
- 2 SPI master up to 16 MHz clock with 4 chip selects
- 19 channel 12-bit ADC
- 16 GPIOs
- 2 Timers

Security

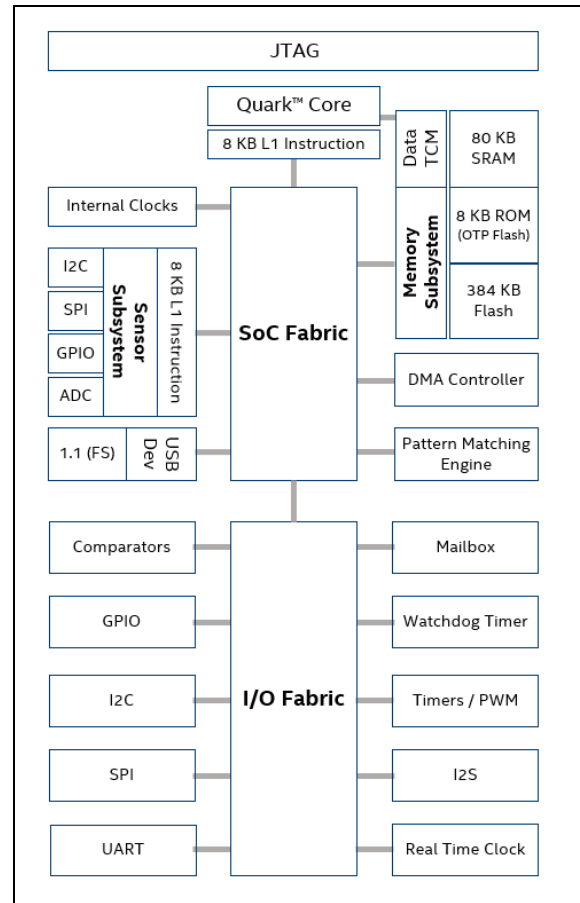
- JTAG Lockout
- Flash Protection
- Isolated SRAM regions
- On-die NVM read/write access control

Characteristics

- WLCSP - 144 pins
 - -25°C to +70°C ambient
 - 10 year reliability (Continuous operation)
 - WLCSP 6.4 x 6.33 x 0.52 mm²
- BGA – 144 pins
 - -40°C to +85°C ambient
 - 10 year reliability (Continuous operation)
 - BGA 10 X 10 X 0.930 mm²

Software Support

- Intel® System Studio for Microcontroller SDK
- Open OCD* Debugging support





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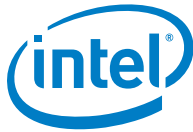
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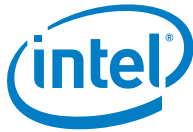
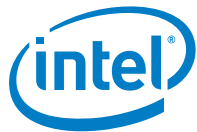


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Revision History

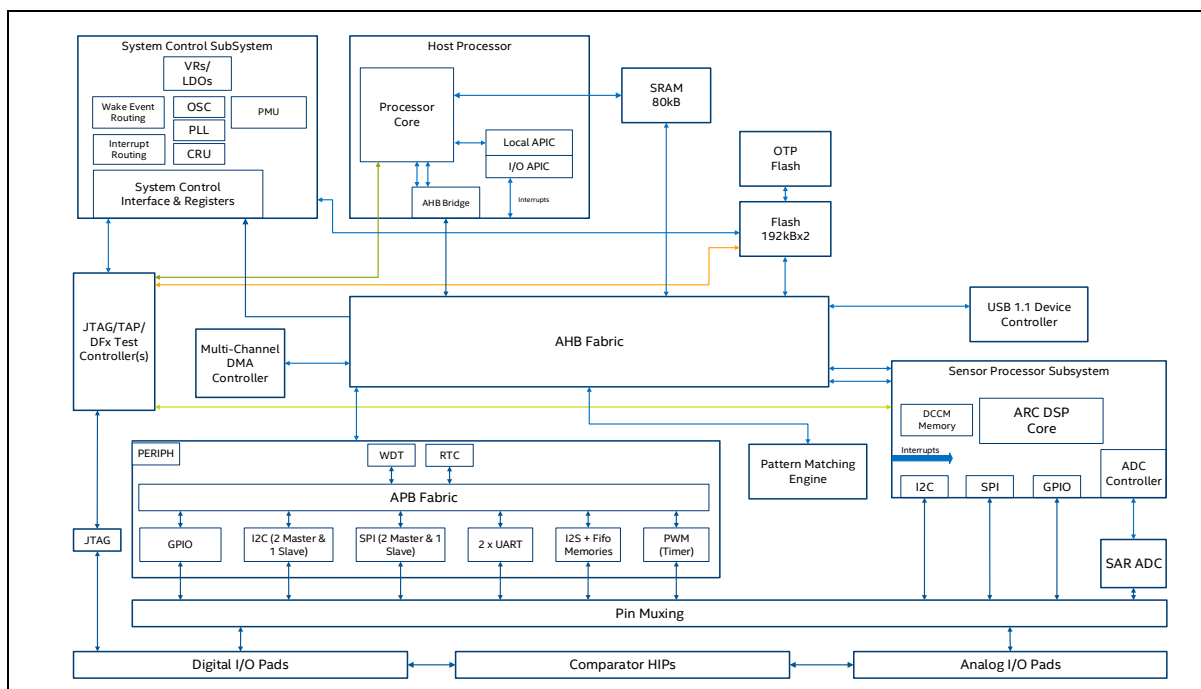
Date	Revision	Description
February 2017	005	Corrected values in Section 4.1.1, "Absolute Maximum Ratings" .
December 2016	004	Minor corrections.
November 2016	003	Added Pattern Matching Engine chapter.
August 2016	002	Added detailed clocking diagrams to Clocking chapter. Added additional information to Power Management chapter.
August 2016	001	Initial release.

1 Introduction

The Intel® Quark™ SE Microcontroller C1000 is an ultra-low power Intel Architecture (IA) device that integrates an Intel® Quark processor core, Sensor Subsystem, Memory Subsystem with on-die volatile and non-volatile storage and I/O interfaces into a single system-on-chip (SoC) solution.

[Figure 1](#) shows the system level block diagram of the Intel® Quark™ SE Microcontroller C1000. For detailed information on the functionality of the different interface blocks, see the subsequent chapters of this document.

Figure 1. Intel® Quark™ SE Microcontroller C1000 Block Diagram



1.1 Quark™ SE Processor Core

- 32 MHz Clock Frequency
- 32-bit Address Bus
- Pentium x86 ISA Compatible without x87 Floating Point Unit
- 8 kB L1 Instruction Cache
- Low Latency Data Tightly Coupled Memory (TCM) Interface to on-die SRAM



- Integrated Local APIC and I/O APIC
- Supports HW DMA

1.2 AHB / APB Bus

Advanced High-Performance Bus (AHB) sits above the Advanced Peripheral Bus (APB) and implements the features required for high-performance, high clock frequency systems. These features include the following:

Advanced High-Performance Bus (AHB)

- Multi-Layer (high performance)
- Pipelined operation
- Burst transfers
- Multiple bus masters

Advanced Peripheral Bus (APB)

- Low power
- Latched address and control
- Suitable for low speed interfaces

1.3 Sensor Subsystem

- Sensor Subsystem processor with Interrupt Controller
- Floating Point Extensions
- 8 kB L1 Instruction Cache (refer to [Chapter 14.1.5, “Flash Controller 0 Register Detailed Description”](#))
- 8 kB Data Closely Coupled Memory (CCM)
- Tightly coupled I/O for interfacing with sensors and actuators
- 2 I2C Master Interfaces with support for Standard and Fast Mode
- 2 SPI Master Interfaces with support for SPI clock frequencies up to 16 MHz
- 19-Channel ADC Controller (max. 12 bit)
- 16 GPIOs
- 2 Timers



1.4 USB Device

- Single USB 1.1 device port
- Supports full speed (12 Mbps) operation

1.5 I2C

- 2 I2C interfaces
- Supports three I2C speeds:
 - Standard Mode (100 Kbps)
 - Fast Mode (400 Kbps)
 - Fast Mode Plus (1 Mbps)
- Supports 7-bit and 10-bit Addressing
- Supports Master and Slave operation
- Supports FIFO mode (16B TX and RX FIFOs)
- Supports HW DMA with configurable FIFO thresholds

1.6 I2S

- 2 I2S Interfaces (one Transmit Interface and one Receive Interface)
- Sample size from 12 to 32-bits
- Supports Left Justified, Right Justified and DSP modes
- Each interface can operate in Master or Slave Mode
- Supports FIFO mode (16B TX and RX FIFOs)
- Supports HW DMA with configurable FIFO thresholds

1.7 UART

- 2 16550 compliant UART interfaces
- Supports baud rates from 300 to 2M
- Supports hardware and software flow control
- Supports FIFO mode (16B TX and RX FIFO)
- Supports HW DMA with configurable FIFO thresholds

1.8 SPI

- 2 SPI Master Interfaces with support for SPI clock frequencies up to 16 MHz
- 1 SPI Slave Interface with support for SPI clock frequencies up to 3.2 MHz



- Supports 4-bit up to 32-bit Frame Size
- Up to 4 Slave Select pins per Master interface
- Supports FIFO mode (8x32bit)
- Supports HW DMA with configurable FIFO thresholds

1.9 DMA Controller

- Provides 8 Unidirectional Channels
- Provides support for 16 HW Handshake Interfaces
- Supports Memory to Memory, Peripheral to Memory, Memory to Peripheral and Peripheral to Peripheral transfers
- Dedicated Hardware Handshaking interfaces with peripherals plus Software Handshaking Support
- Supports Single and Multi-Block Transfers

1.10 GPIO Controller

- Provides 32 independently configurable GPIOs
- All GPIOs are interrupt capable, supporting level sensitive and edge triggered modes
- Debounce logic for interrupt source
- 16 additional GPIOs available via Sensor Subsystem
- 6 additional Always-on interrupt and wake capable GPIOs

1.11 Timers and PWM

- 4 Counters capable of operating in PWM Mode or Timer Mode
- Configurable PWM High and Low time with granularity of a single 32MHz clock period per output
- Timer Mode supports 32-bit timer operating at 32 MHz

1.12 Watchdog Timer

- Configurable watchdog timer with support to trigger an interrupt or a system reset upon timeout.



1.13 Real Time Clock (RTC)

- 32-bit Counter running from 1Hz up to 32.768 kHz
- Supports interrupt and wake event generation upon matching a programmed value
- Only requires 32.768 kHz clock to run to generate interrupt and wake events
- Supports an additional 32-bit Always-On Counter
- Supports a 32-bit Always-On Timer with interrupt and wake capability

1.14 Analog Comparators

- Provides 19 Analog Comparators
- 6 high performance comparators
- 13 low power comparators
- Configurable polarity
- Interrupt and Wake Event capable

1.15 Interrupt Routing

- Configurable Routing of Intel® Quark™ SE microcontroller Interrupts with capability to route to the Interrupt Controller of either the Quark Processor or the Sensor Subsystem Processor

1.16 Power Management

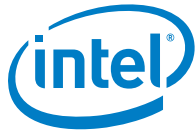
- Intel® Quark™ SE microcontroller System States: Active, Sleep, and Off
- Processor States: C0 – C2LP
- Sensor Subsystem States: Sensing Active, Sensing Wait and Sensing Standby

1.17 Clock Management

- Dynamic Frequency Scaling
- Dynamic Clock Gating
- Autonomous State Based Clock Gating
- Autonomous Peripheral Clock Gating

1.18 Debugging

- 5-pin IEEE 1149.1 JTAG interface



- Boundary scan support
- Sensor subsystem core metaware debugger
- OpenOCD Debugger
- On Chip Debugger controller

1.19 Package

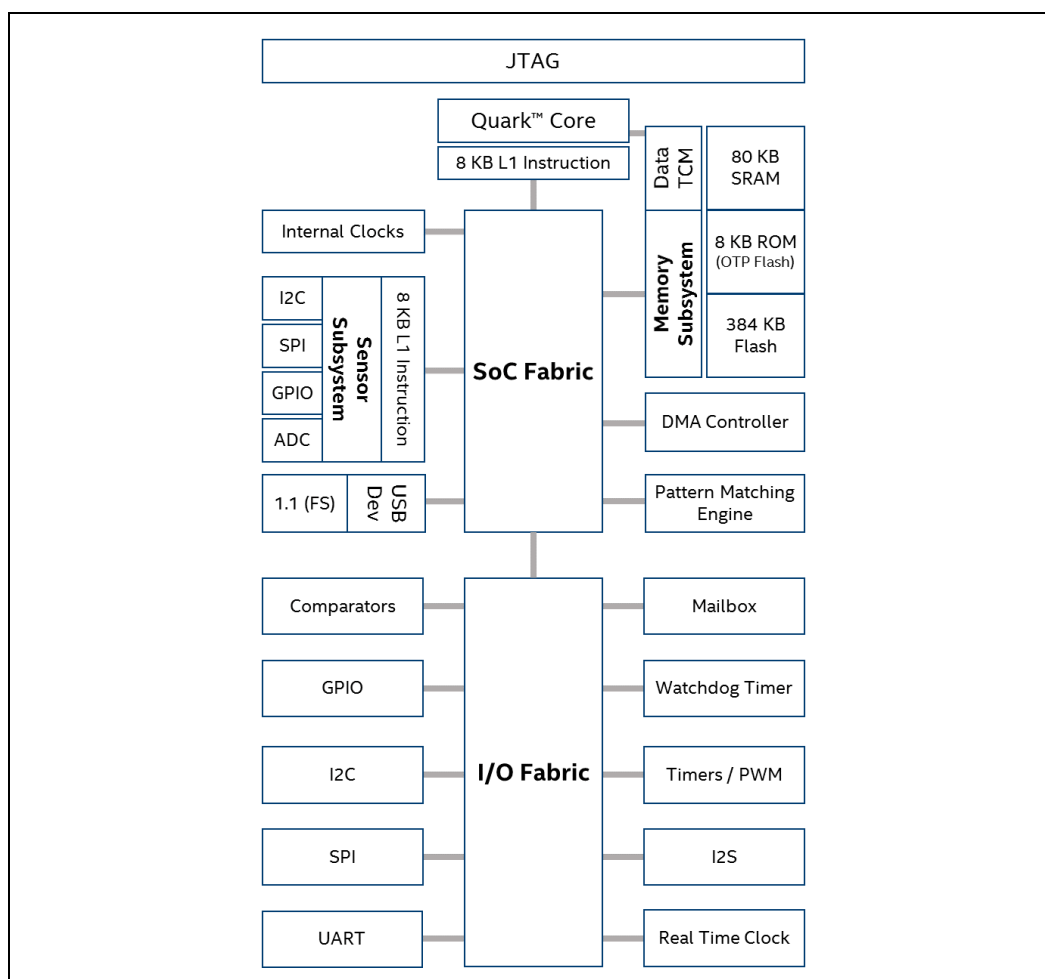
- WLCSP - 144 pins
 - -25°C to +70°C ambient
 - 10 year reliability (Continuous operation)
 - WLCSP 6.4 x 6.33 x 0.52 mm²
- BGA – 144 pins
 - -40°C to +85°C ambient
 - 10 year reliability (Continuous operation)
 - BGA 10 X 10 x 0.930 mm²

§

2 Physical Interfaces

Since the Intel® Quark™ SE Microcontroller C1000 has a small package, many interfaces share pins while some have dedicated physical pins.

Figure 2. Interfaces



2.1 Pin States Through Reset

All GPIO pins are configured as inputs on power-up or the assertion of a system reset. This is done by selecting the pin muxing mode (A), which ensures that no IOs are driven and removes platform bus conflicts. During sleep transition, you can configure the IOs to maintain their value while the HOST domain is powered from. This process is known as IO state retention (IOSR).



2.2 I²C Interface Signals

Table 1. I²C Interface Signals

Signal Name	Dir	Power	Reset	Sleep
I2C0_SCL	IO	VCC_IO_AON	High-Z	IOSR
I2C0_SDA	IO	VCC_IO_AON	High-Z	IOSR
I2C1_SCL	IO	VCC_IO_AON	High-Z	IOSR
I2C1_SDA	IO	VCC_IO_AON	High-Z	IOSR
I2C0_SS_SCL	IO	VCC_IO_AON	High-Z	IOSR
I2C0_SS_SDA	IO	VCC_IO_AON	High-Z	IOSR
I2C1_SS_SCL	IO	VCC_IO_AON	High-Z	IOSR
I2C1_SS_SDA	IO	VCC_IO_AON	High-Z	IOSR

2.3 SPI Interface Signals

Table 2. SPI Interface Signals

Signal Name	Dir	Power	Reset	Sleep
SPI0_M_SCK	O	VCC_IO_AON	High-Z	IOSR
SPI0_M_MISO	I	VCC_IO_AON	High-Z	IOSR
SPI0_M_MOSI	O	VCC_IO_AON	High-Z	IOSR
SPI0_M_CS_B[3:0]	O	VCC_IO_AON	High-Z	IOSR
SPI1_M_SCK	O	VCC_IO_AON	High-Z	IOSR
SPI1_M_MISO	I	VCC_IO_AON	High-Z	IOSR
SPI1_M_MOSI	O	VCC_IO_AON	High-Z	IOSR
SPI1_M_CS_B[3:0]	O	VCC_IO_AON	High-Z	IOSR
SPI0_SS_SCK	O	VCC_IO_AON	High-Z	IOSR
SPI0_SS_SSISO	I	VCC_IO_AON	High-Z	IOSR
SPI0_SS_SSOSI	O	VCC_IO_AON	High-Z	IOSR
SPI0_SS_CS_B[3:0]	O	VCC_IO_AON	High-Z	IOSR
SPI1_SS_SCK	O	VCC_IO_AON	High-Z	IOSR
SPI1_SS_SSISO	I	VCC_IO_AON	High-Z	IOSR
SPI1_SS_SSOSI	O	VCC_IO_AON	High-Z	IOSR
SPI1_SS_CS_B[3:0]	O	VCC_IO_AON	High-Z	IOSR
SPI_S_SCK	I	VCC_IO_AON	High-Z	IOSR
SPI_S_MISO	O	VCC_IO_AON	High-Z	IOSR
SPI_S_MOSI	I	VCC_IO_AON	High-Z	IOSR



Signal Name	Dir	Power	Reset	Sleep
SPI_S_CS_B	I	VCC_IO_AON	High-Z	IOSR

2.4 GPIO Interface Signals

Table 3. GPIO Interface Signals

Signal Name	Dir	Power	Reset	Sleep
GPIO[31:0]	IO	VCC_IO_AON	High-Z	IOSR
GPIO_SS[15:0]	IO	VCC_IO_AON	High-Z	IOSR
GPIO_AON	IO	VCC_IO_AON	High-Z	IOSR

2.5 UART Interface Signals

Table 4. UART Interface Signals

Signal Name	Dir	Power	Reset	Sleep
UART0_RXD	I	VCC_IO_AON	High-Z	IOSR
UART0_TXD	O	VCC_IO_AON	High-Z	IOSR
UART0_CTS_B	I	VCC_IO_AON	High-Z	IOSR
UART0_RTS_B	O	VCC_IO_AON	High-Z	IOSR
UART1_RXD	I	VCC_IO_AON	High-Z	IOSR
UART1_TXD	O	VCC_IO_AON	High-Z	IOSR
UART1_CTS_B	I	VCC_IO_AON	High-Z	IOSR
UART1_RTS_B	O	VCC_IO_AON	High-Z	IOSR

2.6 PWM Interface Signals

Table 5. PWM Interface Signals

Signal Name	Dir	Power	Reset	Sleep
PWM[3:0]	IO	VCC_IO_AON	High-Z	IOSR

2.7 I2S Interface Signals

Table 6. I2S Interface Signals

Signal Name	Dir	Power	Reset	Sleep
I2S_RXD	I	VCC_IO_AON	High-Z	IOSR



Signal Name	Dir	Power	Reset	Sleep
I2S_RSCK	IO	VCC_IO_AON	High-Z	IOSR
I2S_RWS	IO	VCC_IO_AON	High-Z	IOSR
I2S_TSCK	IO	VCC_IO_AON	High-Z	IOSR
I2S_TWS	IO	VCC_IO_AON	High-Z	IOSR
I2S_TXD	O	VCC_IO_AON	High-Z	IOSR

2.8 PLT_CLK Interface Signals

Table 7. PLT_CLK Interface Signals

Signal Name	Dir	Power	Reset	Sleep
PLT_CLK[1:0]	O	VCC_IO_AON	High-Z	IOSR

2.9 USB Interface Signals

Table 8. USB Interface Signals

Signal Name	Dir	Power	Reset	Sleep
USB_DP	IO	VCC_USB_3P3	High-Z	OFF
USB_DN	IO	VCC_USB_3P3	High-Z	OFF

2.10 ADC Interface Signals

Table 9. ADC Interface Signals

Signal Name	Dir	Power	Reset	Sleep
AI[18:0]	I	VCC_ADC	Input	OFF

2.11 Hardware Straps

Table 10. Hardware Straps

Signal Name	Power	Function
PLT_REG_EN	VCC_AVD_OPM_2P6	Configures the power on sequence for the Intel® Quark™ SE Microcontroller C1000. 0b: Power On Sequence using Internal Regulators 1b: Power On Sequence using External Regulators



3 Ballout and Package Information

The Intel® Quark™ SE Microcontroller C1000 comes in a 6.410 X 6.33 X 0.520 mm Wafer Level Chip Scale Package (WLCSP) package and a 10mm x 10mm Ball Grid Array (BGA) Package.

3.1 WLCSP SoC Attributes

- Package parameters: 6.410 X 6.330 X 0.520 mm (WLCSP)
- Ball Count: 144
- Temperature qualification: -25°C to +70°C

All Units: mm

Tolerances if not specified:

- .X: ± 0.1
- .XX: ± 0.05

Angles: ± 1.0 degrees

3.2 BGA SoC Attributes

- Package parameters: 10 X 10 X 0.930 mm (BGA)
- Pin Count: 144
- Temperature qualification: -40°C to +85°C ambient

All units: mm

Tolerances if not specified:

- .X: ± 0.1
- .XX: ± 0.05
- Angles: ± 1.0 degrees



3.3 Package Diagrams for WLCSP/BGA

Figure 3. Mechanical Drawing of BGA Package

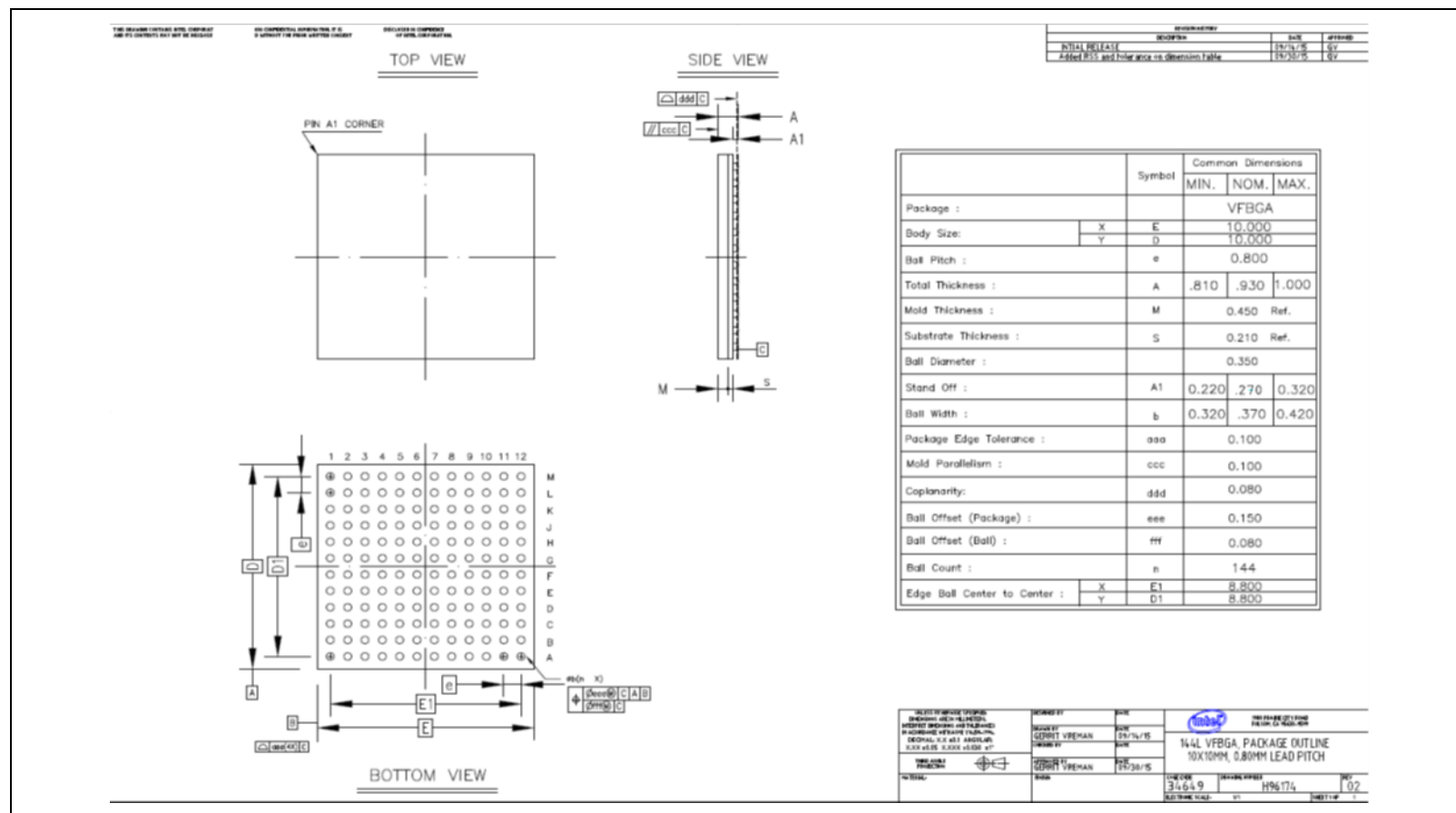
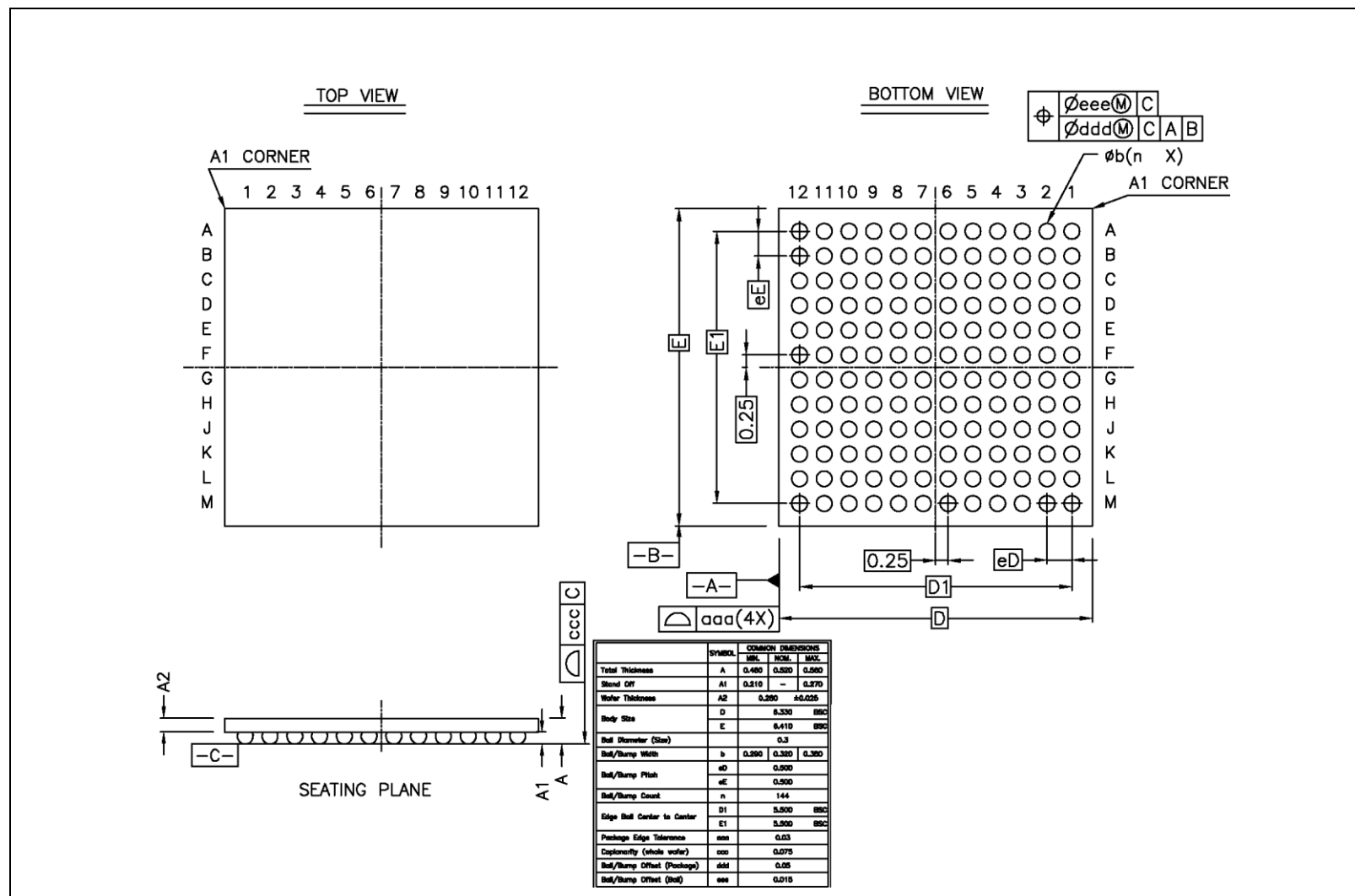




Figure 4. Mechanical Drawing of WLSCP Package





3.4 Alphabetical Ball Listing For WLCSP Package

Many I/Os are configurable GPIOs. These I/Os are multiplexed with other signals in the ball list. The table below matches the locations and functions of every ball with all possible multiplexed signals (denoted as GPIO Functions). Configurable GPIOs default to function 0 during power on. The Intel® Quark™ SE Microcontroller C1000 firmware is responsible for enabling the platform specific configuration. By default, all F0 function pins are enabled.

Table 11. Alphabetical Ball Listing for WLCSP Package

Location	Ballmap Name	Function_0	Function_1	Function_2	Description
A1	VSS	VSS - Ground			Ground
A2	VCC_AON_1P8	VCC_AON_1P8			1.8v supply voltage for AON counter
A3	EXTERNAL_PAD_27	I2C1_SS_SCL			Clock for I2C1 on SensorSubsystem
A4	EXTERNAL_PAD_34	SPI0_SS_CS_B[3]	GPIO[30]		Chip select 3 for SPI0 on SensorSubsystem/ GPIO[30]
A5	VCC_HOST_1P8	VCC_HOST_1P8			1.8v from platform to SOC
A6	EXTERNAL_PAD_40	SPI1_SS_CS_B[2]	UART0_CTS_B		SPI1 Chip Select 2 on SensorSubsystem/ UART0 Clear to Send Active low
A7	EXTERNAL_PAD_48	GPIO[14]	SPI1_M_CS_B[3]		GPIO[14]/SPI1 Master Chip Select 3
A8	EXTERNAL_PAD_50	GPIO[16]	I2S_RSCK		GPIO[16]/I2S Receive Clock
A9	EXTERNAL_PAD_52	GPIO[18]	I2S_TSCK		GPIO[18]/I2S Transmit Clock
A10	EXTERNAL_PAD_59	GPIO[25]	SPI0_M_CS_B[1]		GPIO[25]/SPI0 Master Chip Select 1
A11	VCC_IO_AON	VCC_IO_AON			IO supply voltage
A12	NC	NC			No Connect
B1	VSS	VSS			Ground
B2	EXTERNAL_PAD_19	UART0_TXD	GPIO[31]		UART0 transmit/GPIO[31]
B3	EXTERNAL_PAD_26	I2C1_SS_SDA			I2C1 Sensor Subsystem Data
B4	EXTERNAL_PAD_33	SPI0_SS_CS_B[2]	GPIO[29]		SPI0 Sensor Subsystem Chip Select 2/GPIO[29]
B5	EXTERNAL_PAD_35	SPI1_SS_MISO			SPI1 Sensor Subsystem Master In Slave Out
B6	EXTERNAL_PAD_41	SPI1_SS_CS_B[3]	UART0_RTS_B		SPI1 Sensor Subsystem Chip Select 3/UART-ready to send



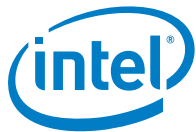
Location	Ballmap Name	Function_0	Function_1	Function_2	Description
B7	EXTERNAL_PAD_47	GPIO[13]	SPI1_M_CS_B[2]		GPIO[13]/SPI1 Master Chip Select 2
B8	EXTERNAL_PAD_49	GPIO[15]	I2S_RXD		GPIO[15]/I2S Receive
B9	EXTERNAL_PAD_51	GPIO[17]	I2S_RWS		GPIO[17]/I2S Receive Write Select
B10	EXTERNAL_PAD_60	GPIO[26]	SPI0_M_CS_B[2]		GPIO[26]/SPI0 Master Chip Select 2
B11	EXTERNAL_PAD_66	GPIO_SS[13]	PWM[3]		GPIO Sensor Subsystem [13]/Pulse Width Modulation[3]
B12	VSS_IO_AON	VSS_IO_AON			Ground for IO
C1	EXTERNAL_PAD_20	I2C0_SCL			I2C0 Clock
C2	EXTERNAL_PAD_21	I2C0_SDA - data			I2C0 Data
C3	EXTERNAL_PAD_28	SPI0_SS_MISO			SPI0 Sensor Subsystem Master In Slave Out
C4	EXTERNAL_PAD_32	SPI0_SS_CS_B[1]			SPI0 Sensor Subsystem Chip Select 1
C5	EXTERNAL_PAD_36	SPI1_SS_MOSI			SPI1 Sensor Subsystem Master Out Slave In
C6	EXTERNAL_PAD_42	GPIO[8]	SPI1_M_SCK -		GPIO[8]/SPI1 Master Clock
C7	EXTERNAL_PAD_46	GPIO[12]	SPI1_M_CS_B[1]		GPIO[12]/SPI1 Master Chip Select 1
C8	VCC_SRAM_1P8	VCC_SRAM_1P8			1.8 SRAM supply voltage
C9	EXTERNAL_PAD_53	GPIO[19]	I2S_TWS		GPIO[19]/I2S Transmit Write Select
C10	EXTERNAL_PAD_61	GPIO[27]	SPI0_M_CS_B[3]		GPIO[27]/SPI0 Master Chip Select 3
C11	EXTERNAL_PAD_65	GPIO_SS[12]	PWM[2]		GPIO for Sensor Subsystem[12]/ PWM[2]
C12	EXTERNAL_PAD_68	GPIO_SS[15]	PLT_CLK[1]		GPIO for Sensor Subsystem[15]/ Platform Clock Output 1
D1	EXTERNAL_PAD_22	I2C1_SCL			I2C1 serial clock
D2	EXTERNAL_PAD_23	I2C1_SDA			I2C1 serial data
D3	EXTERNAL_PAD_30	SPI0_SS_SCK			SPI0 SensorSubsystem Clock
D4	EXTERNAL_PAD_31	SPI0_SS_CS_B[0]			SPI0 SensorSubsystem Chip Select 0
D5	EXTERNAL_PAD_37	SPI1_SS_SCK			SPI1 Sensor Subsystem Clock



Location	Ballmap Name	Function_0	Function_1	Function_2	Description
D6	EXTERNAL_PAD_43	GPIO[9]	SPI1_M_MISO		GPIO[9]/SPI1 Master in Slave Out
D7	EXTERNAL_PAD_45	GPIO[11]	SPI1_M_CS_B[0]		GPIO[11]/SPI1 Master Chip Select 0
D8	EXTERNAL_PAD_55	GPIO[21]	SPI0_M_SCK		GPIO[21]/SPI0 Master Clock
D9	EXTERNAL_PAD_54	GPIO[20]	I2S_TXD		GPIO[20]/I2S transmit data
D10	EXTERNAL_PAD_62	GPIO[28]			GPIO[28]
D11	EXTERNAL_PAD_64	GPIO_SS[11]	PWM[1]		GPIO Sensor Subsystem[11]/ PWM[1]
D12	EXTERNAL_PAD_67	GPIO_SS[14]	PLT_CLK[0]		GPIO for Sensor Subsystem[14]/ Platform Clock 0
E1	EXTERNAL_PAD_24	I2C0_SS_SDA			I2C0 SensorSubsystem Data
E2	EXTERNAL_PAD_25	I2C0_SS_SCL			I2C0 SensorSubsystem Clock
E3	EXTERNAL_PAD_29	SPI0_SS_MOSI			SPI0 SensorSubsystem Master Out Slave In
E4	EXTERNAL_PAD_39	SPI1_SS_CS_B[1]			SPI1 Sensor Subsystem Chip Select 1
E5	EXTERNAL_PAD_38	SPI1_SS_CS_B[0]			SPI1 Sensor Subsystem Chip Select 0
E6	EXTERNAL_PAD_44	GPIO[10]	SPI1_M_MOSI		GPIO[10]/SPI1 Master Out Slave In
E7	EXTERNAL_PAD_56	GPIO[22]	SPI0_M_MISO		GPIO[22]/SPI0 Master In Slave Out
E8	EXTERNAL_PAD_58	GPIO[24]	SPI0_M_CS_B[0]		GPIO[24]/ SPI0 Master Chip Select 0
E9	EXTERNAL_PAD_57	GPIO[23]	SPI0_M_MOSI		GPIO[23]/SPI0 Master Out Slave In
E10	EXTERNAL_PAD_63	GPIO_SS[10]	PWM[0]		GPIO for Sensor Subsystem[10]/ PWM[0]
E11	AON_GPIO_PAD_1	AON_GPIO_1			Always on GPIO [1]
E12	AON_GPIO_PAD_2	AON_GPIO_2			Always on GPIO [2]
F1	EXTERNAL_PAD_14	GPIO_SS[6]	AIN[14]		GPIO for Sensor Subsystem[6]/ Analog input [14]
F2	EXTERNAL_PAD_00	GPIO[0]	AIN[0]	SPI_S_CS_B	GPIO[0]/Analog Input [0]/SPI Slave Chip Select
F3	VSS	VSS			Ground
F4	TDI_PAD	TDI			JTAG data in



Location	Ballmap Name	Function_0	Function_1	Function_2	Description
F5	AREF_PAD	AREF			Analog reference voltage
F6	TMS_PAD	TMS			JTAG master select
F7	VSS_IO_AON	VSS_IO_AON			Ground for IO AON
F8	TDO_PAD	TDO			JTAG data out
F9	AON_GPIO_PAD_3	AON_GPIO_3			Always On GPIO [3]
F10	AON_GPIO_PAD_4	AON_GPIO_4			Always On GPIO [4]
F11	RST_N_PAD	RST_N			Main reset for SOC
F12	AON_PWR_GOOD_PAD	AON_PWR_GOOD			Power good input
G1	EXTERNAL_PAD_11	GPIO_SS[3]	AIN[11]		GPIO for Sensor Subsystem[3]/ Analog Input [11]
G2	EXTERNAL_PAD_13	GPIO_SS[5]	AIN[13]		GPIO for Sensor Subsystem[5]/ Analog Input [13]
G3	EXTERNAL_PAD_07	GPIO[7]	AIN[7]		GPIO[7]/ Analog Input [7]
G4	EXTERNAL_PAD_01	GPIO[1]	AIN[1]	SPI_S_MISO	GPIO[1]/ Analog Input [1]/SPI Slave Master in Slave Out
G5	TRST_PAD	TRST			JTAG reset
G6	VCC_IO_AON	VCC_IO_AON			Input voltage for AON IO
G7	TCK_PAD	TCK			JTAG clock
G8	AON_GPIO_PAD_5	AON_GPIO_5			Always on GPIO[5]
G9	AON_GPIO_PAD_0	AON_GPIO_0			Always on GPIO[0]
G10	VCC_RTC_1P8	VCC_RTC_1P8			1.8 supply voltage for RTC
G11	RTC_XTALI_PAD	RTC_XTALI			RTC Clock Input
G12	RTC_XTALO_PAD	RTC_XTALO			RTC Clock output
H1	USB_PADP	USB_P			USB positive
H2	USB_PADN	USB_N			USB negative
H3	VSS_AVSS_CMP	VSS_AVSS_CMP			Comparator ground
H4	EXTERNAL_PAD_06	GPIO[6]	AIN[6]		GPIO[6]/Analog Input [6]
H5	EXTERNAL_PAD_02	GPIO[2]	AIN[2]	SPI_S_SCK	GPIO[2]/Analog Input [2]/SPI Slave Clock
H6	VCC_HOST_1P8	VCC_HOST_1P8			1.8 host supply
H7	VSS_AVSS_ESR2	VSS_AVSS_ESR2			Ground for switching regulator 2



Location	Ballmap Name	Function_0	Function_1	Function_2	Description
H8	VSS_GNDSSENSE_ESR2	VSS_GNDSSENSE_ESR2			Ground sense on switching regulator 2
H9	VCC_VSENSE_ESR1	VCC_VSENSE_ESR1			VSense on Switching Regulator1
H10	REG_PLAT_PAD	REG_PLAT			Internal or external regulator select
H11	VSS_RTC	VSS_RTC			RTC ground
H12	VSS	VSS			Ground
J1	VSS_USB	VSS_USB			USB ground
J2	VCC_USB_3P3	VCC_USB_3P3			3.3 supply voltage for USB
J3	VCC_CMP_3P3	VCC_CMP_3P3			3.3 comparators supply voltage
J4	EXTERNAL_PAD_12	GPIO_SS[4]	AIN[12]		GPIO for Sensor Subsystem[4]/ Analog Input[12]
J5	EXTERNAL_PAD_15	GPIO_SS[7]	AIN[15]		GPIO for Sensor Subsystem[7]/ Analog Input[15]
J6	EXTERNAL_PAD_03	GPIO[3]	AIN[3]	SPI_S_MOSI	GPIO[3]/Analog Input[3]/SPI slave Master Out slave in
J7	VCC_AON_1P8	VCC_AON_1P8			1.8 supply voltage to AON
J8	VCCOUT_ESR1_3P3	VCCOUT_ESR1_3P3			Output voltage for switching reg1
J9	VCCOUT_QLR1_3P3	VCCOUT_QLR1_3P3			Output voltage for linear reg1
J10	VCC_VSENSE_ESR2	VCC_VSENSE_ESR2			VSense on Switching Regulator2
J11	VCCOUT_QLR2_1P8	VCCOUT_QLR2_1P8			Output voltage for linear reg2
J12	VCCOUT_ESR2_1P8	VCCOUT_ESR2_1P8			Output voltage for switching reg2
K1	HYB_XTALO_PAD	HYB_XTALO			Hybrid clock out
K2	HYB_XTALI_PAD	HYB_XTALI			Hybrid clock in
K3	VCC_PLL_1P8	VCC_PLL_1P8			1.8 PLL supply voltage
K4	EXTERNAL_PAD_18	UART0_RXD	AIN[18]		UART0 receiver data/Analog input[18]
K5	EXTERNAL_PAD_10	GPIO_SS[2]	AIN[10]		GPIO for Sensor Subsystem[2]/ Analog input[10]
K6	EXTERNAL_PAD_04	GPIO[4]	AIN[4]		GPIO[4]/ Analog input[4]



Location	Ballmap Name	Function_0	Function_1	Function_2	Description
K7	VSS_GNDSSENSE_OPM	VSS_GNDSSENSE_OPM			Ground Sense for over voltage protection module
K8	VCCOUT_AON_1P8	VCCOUT_AON_1P8			1.8 Supply voltage AON
K9	VCCOUT_ESR3_1P8	VCCOUT_ESR3_1P8			1.8 Supply voltage ESR3
K10	VCCOUT_HOST_1P8	VCCOUT_HOST_1P8			1.8 host supply output
K11	VCCOUT_AVD_OPM_2P6	VCCOUT_AVD_OPM_2P6			2.6 Output voltage supply for OPM
K12	VCC_AVD_OPM_2P6	VCC_AVD_OPM_2P6			2.6 voltage supply for OPM
L1	VSS_AVSS_CMP	VSS_AVSS_CMP			Ground for comparators
L2	VSS_PLL	VSS_PLL			Ground for PLL
L3	VSS_ADC_AGND	VSS_ADC_AGND			ADC ground
L4	EXTERNAL_PAD_16	GPIO_SS[8]	AIN[16]	UART1_TXD	GPIO for Sensor Subsystem[8]/ Analog In[16]/ UART1 Transmit data
L5	EXTERNAL_PAD_08	GPIO_SS[0]	AIN[8]	UART1_CTS_B	GPIO for Sensor Subsystem[0]/ Analog In[8]/UART1 Clear to send
L6	EXTERNAL_PAD_05	GPIO[5]	AIN[5]		GPIO[5]/Analog input[5]
L7	VSS_AVS_ESR1	VSS_AVS_ESR1			Ground for switching regulator 1
L8	VSS_GNDSSENSE_ESR1	VSS_GNDSSENSE_ESR1			Ground sense for switching regulator 1
L9	VCC_VSENSE_ESR3	VCC_VSENSE_ESR3			Vsense for Switching regulator 3
L10	VCC_BATT_OPM_3P7	VCC_BATT_OPM_3P7			Main supply voltage for OPM
L11	VCC_BATT_ESR2_3P7	VCC_BATT_ESR2_3P7			Main supply voltage for Switching regulator 2
L12	VSS	VSS			Ground
M1	VSS	VSS			Ground
M2	VCC_CMP_3P3	VCC_CMP_3P3			3.3 comparators supply voltage
M3	VCC_ADC_3P3	VCC_ADC_3P3			3.3 ADC supply voltage
M4	EXTERNAL_PAD_17	GPIO_SS[9]	AIN[17]	UART1_RXD	GPIO for Sensor Subsystem[9]/ Analog[17]/UART1 Receive Data
M5	EXTERNAL_PAD_09	GPIO_SS[1]	AIN[9]	UART1_RTS_B	GPIO for Sensor Subsystem[1]/ Analog In[9]/UART1 Ready to Send



Location	Ballmap Name	Function_0	Function_1	Function_2	Description
M6	VSS	VSS			Ground
M7	VSS_GNDSense_ESR3	VSS_GNDSense_ESR3			Ground Sense for ESR3
M8	VSS_AVS_ESR3	VSS_AVS_ESR3			Ground for ESR3
M9	VCC_BATT_ESR3_3P7	VCC_BATT_ESR3_3P7			Mains supply voltage for ESR3
M10	VCC_BATT_ESR1_3P7	VCC_BATT_ESR1_3P7			Mains supply voltage for ESR1
M11	VSS	VSS			Ground
M12	VSS	VSS			Ground

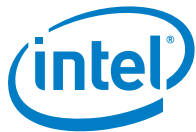
3.5 Alphabetical Function Listing For WLCSP Package

Table 12. Alphabetical Function Listing for WLCSP Package

Location	Ballmap Name	Function_0	Function_1	Function_2
G9	AON_GPIO_PAD_0	AON_GPIO_0		
E11	AON_GPIO_PAD_1	AON_GPIO_1		
E12	AON_GPIO_PAD_2	AON_GPIO_2		
F9	AON_GPIO_PAD_3	AON_GPIO_3		
F10	AON_GPIO_PAD_4	AON_GPIO_4		
G8	AON_GPIO_PAD_5	AON_GPIO_5		
F12	AON_PWR_GOOD_PAD	AON_PWR_GOOD		
F5	AREF_PAD	AREF		
F2	EXTERNAL_PAD_00	GPIO[0]	AIN[0]	SPI_S_CS_B
G4	EXTERNAL_PAD_01	GPIO[1]	AIN[1]	SPI_S_MISO
H5	EXTERNAL_PAD_02	GPIO[2]	AIN[2]	SPI_S_SCK
J6	EXTERNAL_PAD_03	GPIO[3]	AIN[3]	SPI_S_MOSI
K6	EXTERNAL_PAD_04	GPIO[4]	AIN[4]	
L6	EXTERNAL_PAD_05	GPIO[5]	AIN[5]	
H4	EXTERNAL_PAD_06	GPIO[6]	AIN[6]	
G3	EXTERNAL_PAD_07	GPIO[7]	AIN[7]	
C6	EXTERNAL_PAD_42	GPIO[8]	SPI1_M_SCK	



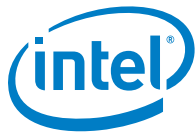
Location	Ballmap Name	Function_0	Function_1	Function_2
D6	EXTERNAL_PAD_43	GPIO[9]	SPI1_M_MISO	
E6	EXTERNAL_PAD_44	GPIO[10]	SPI1_M_MOSI	
D7	EXTERNAL_PAD_45	GPIO[11]	SPI1_M_CS_B[0]	
C7	EXTERNAL_PAD_46	GPIO[12]	SPI1_M_CS_B[1]	
B7	EXTERNAL_PAD_47	GPIO[13]	SPI1_M_CS_B[2]	
A7	EXTERNAL_PAD_48	GPIO[14]	SPI1_M_CS_B[3]	
B8	EXTERNAL_PAD_49	GPIO[15]	I2S_RXD	
A8	EXTERNAL_PAD_50	GPIO[16]	I2S_RSCK	
B9	EXTERNAL_PAD_51	GPIO[17]	I2S_RWS	
A9	EXTERNAL_PAD_52	GPIO[18]	I2S_TSCK	
C9	EXTERNAL_PAD_53	GPIO[19]	I2S_TWS	
D9	EXTERNAL_PAD_54	GPIO[20]	I2S_TXD	
D8	EXTERNAL_PAD_55	GPIO[21]	SPI0_M_SCK	
E7	EXTERNAL_PAD_56	GPIO[22]	SPI0_M_MISO	
E9	EXTERNAL_PAD_57	GPIO[23]	SPI0_M_MOSI	
E8	EXTERNAL_PAD_58	GPIO[24]	SPI0_M_CS_B[0]	
A10	EXTERNAL_PAD_59	GPIO[25]	SPI0_M_CS_B[1]	
B10	EXTERNAL_PAD_60	GPIO[26]	SPI0_M_CS_B[2]	
C10	EXTERNAL_PAD_61	GPIO[27]	SPI0_M_CS_B[3]	
D10	EXTERNAL_PAD_62	GPIO[28]		
L5	EXTERNAL_PAD_08	GPIO_SS[0]	AIN[8]	UART1_CTS_B
M5	EXTERNAL_PAD_09	GPIO_SS[1]	AIN[9]	UART1_RTS_B
K5	EXTERNAL_PAD_10	GPIO_SS[2]	AIN[10]	
G1	EXTERNAL_PAD_11	GPIO_SS[3]	AIN[11]	
J4	EXTERNAL_PAD_12	GPIO_SS[4]	AIN[12]	
G2	EXTERNAL_PAD_13	GPIO_SS[5]	AIN[13]	
F1	EXTERNAL_PAD_14	GPIO_SS[6]	AIN[14]	
J5	EXTERNAL_PAD_15	GPIO_SS[7]	AIN[15]	
L4	EXTERNAL_PAD_16	GPIO_SS[8]	AIN[16]	UART1_TXD
M4	EXTERNAL_PAD_17	GPIO_SS[9]	AIN[17]	UART1_RXD
E10	EXTERNAL_PAD_63	GPIO_SS[10]	PWM[0]	
D11	EXTERNAL_PAD_64	GPIO_SS[11]	PWM[1]	
C11	EXTERNAL_PAD_65	GPIO_SS[12]	PWM[2]	



Location	Ballmap Name	Function_0	Function_1	Function_2
B11	EXTERNAL_PAD_66	GPIO_SS[13]	PWM[3]	
D12	EXTERNAL_PAD_67	GPIO_SS[14]	PLT_CLK[0]	
C12	EXTERNAL_PAD_68	GPIO_SS[15]	PLT_CLK[1]	
K2	HYB_XTALI_PAD	HYB_XTALI		
K1	HYB_XTALO_PAD	HYB_XTALO		
C1	EXTERNAL_PAD_20	I2C0_SCL		
C2	EXTERNAL_PAD_21	I2C0_SDA		
D1	EXTERNAL_PAD_22	I2C1_SCL		
D2	EXTERNAL_PAD_23	I2C1_SDA		
E1	EXTERNAL_PAD_24	I2C0_SS_SDA		
E2	EXTERNAL_PAD_25	I2C0_SS_SCL		
B3	EXTERNAL_PAD_26	I2C1_SS_SDA		
A3	EXTERNAL_PAD_27	I2C1_SS_SCL		
A12	NC	NC		
H10	REG_PLAT_PAD	REG_PLAT		
F11	RST_N_PAD	RST_N		
G11	RTC_XTALI_PAD	RTC_XTALI		
G12	RTC_XTALO_PAD	RTC_XTALO		
C3	EXTERNAL_PAD_28	SPI0_SS_MISO		
E3	EXTERNAL_PAD_29	SPI0_SS_MOSI		
D3	EXTERNAL_PAD_30	SPI0_SS_SCK		
D4	EXTERNAL_PAD_31	SPI0_SS_CS_B[0]		
C4	EXTERNAL_PAD_32	SPI0_SS_CS_B[1]		
B4	EXTERNAL_PAD_33	SPI0_SS_CS_B[2]	GPIO[29]	
A4	EXTERNAL_PAD_34	SPI0_SS_CS_B[3]	GPIO[30]	
B5	EXTERNAL_PAD_35	SPI1_SS_MISO		
C5	EXTERNAL_PAD_36	SPI1_SS_MOSI		
D5	EXTERNAL_PAD_37	SPI1_SS_SCK		
E5	EXTERNAL_PAD_38	SPI1_SS_CS_B[0]		
E4	EXTERNAL_PAD_39	SPI1_SS_CS_B[1]		
A6	EXTERNAL_PAD_40	SPI1_SS_CS_B[2]	UART0_CTS_B	
B6	EXTERNAL_PAD_41	SPI1_SS_CS_B[3]	UART0_RTS_B	
G7	TCK_PAD	TCK		



Location	Ballmap Name	Function_0	Function_1	Function_2
F4	TDI_PAD	TDI		
F8	TDO_PAD	TDO		
F6	TMS_PAD	TMS		
G5	TRST_PAD	TRST		
K4	EXTERNAL_PAD_18	UART0_RXD	AIN[18]	
B2	EXTERNAL_PAD_19	UART0_TXD	GPIO[31]	
H2	USB_PADN	USB_N		
H1	USB_PADP	USB_P		
M3	VCC_ADC_3P3	VCC_ADC_3P3		
A2	VCC_AON_1P8	VCC_AON_1P8		
J7	VCC_AON_1P8	VCC_AON_1P8		
K12	VCC_AVD_OPM_2P6	VCC_AVD_OPM_2P6		
M10	VCC_BATT_ESR1_3P7	VCC_BATT_ESR1_3P7		
L11	VCC_BATT_ESR2_3P7	VCC_BATT_ESR2_3P7		
M9	VCC_BATT_ESR3_3P7	VCC_BATT_ESR3_3P7		
L10	VCC_BATT_OPM_3P7	VCC_BATT_OPM_3P7		
J3	VCC_CMP_3P3	VCC_CMP_3P3		
M2	VCC_CMP_3P3	VCC_CMP_3P3		
A5	VCC_HOST_1P8	VCC_HOST_1P8		
H6	VCC_HOST_1P8	VCC_HOST_1P8		
A11	VCC_IO_AON	VCC_IO_AON		
G6	VCC_IO_AON	VCC_IO_AON		
K3	VCC_PLL_1P8	VCC_PLL_1P8		
G10	VCC_RTC_1P8	VCC_RTC_1P8		
C8	VCC_SRAM_1P8	VCC_SRAM_1P8		
J2	VCC_USB_3P3	VCC_USB_3P3		
H9	VCC_VSENSE_ESR1	VCC_VSENSE_ESR1		
J10	VCC_VSENSE_ESR2	VCC_VSENSE_ESR2		
L9	VCC_VSENSE_ESR3	VCC_VSENSE_ESR3		
K8	VCCOUT_AON_1P8	VCCOUT_AON_1P8		
K11	VCCOUT_AVD_OPM_2P6	VCCOUT_AVD_OPM_2P6		
J8	VCCOUT_ESR1_3P3	VCCOUT_ESR1_3P3		
J12	VCCOUT_ESR2_1P8	VCCOUT_ESR2_1P8		



Location	Ballmap Name	Function_0	Function_1	Function_2
K9	VCCOUT_ESR3_1P8	VCCOUT_ESR3_1P8		
K10	VCCOUT_HOST_1P8	VCCOUT_HOST_1P8		
J9	VCCOUT_QLR1_3P3	VCCOUT_QLR1_3P3		
J11	VCCOUT_QLR2_1P8	VCCOUT_QLR2_1P8		
A1	VSS	VSS		
B1	VSS	VSS		
F3	VSS	VSS		
H12	VSS	VSS		
L12	VSS	VSS		
M1	VSS	VSS		
M6	VSS	VSS		
M11	VSS	VSS		
M12	VSS	VSS		
L3	VSS_ADC_AGND	VSS_ADC_AGND		
L7	VSS_AVS_ESR1	VSS_AVS_ESR1		
H7	VSS_AVS_ESR2	VSS_AVS_ESR2		
M8	VSS_AVS_ESR3	VSS_AVS_ESR3		
H3	VSS_AVSS_CMP	VSS_AVSS_CMP		
L1	VSS_AVSS_CMP	VSS_AVSS_CMP		
L8	VSS_GNDSSENSE_ESR1	VSS_GNDSSENSE_ESR1		
H8	VSS_GNDSSENSE_ESR2	VSS_GNDSSENSE_ESR2		
M7	VSS_GNDSSENSE_ESR3	VSS_GNDSSENSE_ESR3		
K7	VSS_GNDSSENSE_OPM	VSS_GNDSSENSE_OPM		
B12	VSS_IO_AON	VSS_IO_AON		
F7	VSS_IO_AON	VSS_IO_AON		
L2	VSS_PLL	VSS_PLL		
H11	VSS_RTC	VSS_RTC		
J1	VSS_USB	VSS_USB		



3.6 Alphabetical Ball Listing For BGA Package

Table 13. Alphabetical Ball Listing for BGA Package

Location	Ballmap Name	Function_0	Function_1	Function_2	Description
A1	VSS	VSS			Ground
A2	EXTERNAL_PAD_61	GPIO[27]	SPIO_M_CS_B[3]		GPIO[27]/SPI0 Master Chip Select 3
A3	EXTERNAL_PAD_55	GPIO[21]	SPIO_M_SCK		GPIO[21]/SPI0 Master Clock
A4	EXTERNAL_PAD_52	GPIO[18]	I2S_TSCK		GPIO[18]/I2S Transmit Clock
A5	EXTERNAL_PAD_47	GPIO[13]	SPI1_M_CS_B[2]		GPIO[13]/SPI1 Master Chip Select 2
A6	EXTERNAL_PAD_44	GPIO[10]	SPI1_M_MOSI		GPIO[10]/SPI1 Master Master-Out Slave-In
A7	EXTERNAL_PAD_39	SPI1_SS_CS_B[1]			SPI1 Sensor Subsystem Chip Select 1
A8	EXTERNAL_PAD_35	SPI1_SS_MISO			SPI1 Sensor Subsystem Master - Out Slave-In
A9	EXTERNAL_PAD_31	SPIO_SS_CS_B[0]			SPIO SensorSubsystem Chip Select 0
A10	EXTERNAL_PAD_28	SPIO_SS_MISO			SPIO SensorSubsystem Master-Out Slave-In
A11	EXTERNAL_PAD_24	I2CO_SS_SDA			I2CO SensorSubsystem Serial Data
A12	VSS	VSS			Ground
B1	EXTERNAL_PAD_64	GPIO_SS[11]	PWM[1]		GPIO Sensor Subsystem[11]/ PWM[1]
B2	EXTERNAL_PAD_60	GPIO[26]	SPIO_M_CS_B[2]		GPIO[26]/SPI0 Master Chip Select 2
B3	EXTERNAL_PAD_54	GPIO[20]	I2S_TXD		GPIO[20]/I2S transmit data
B4	EXTERNAL_PAD_50	GPIO[16]	I2S_RSCK		GPIO[16]/I2S Receive Clock
B5	EXTERNAL_PAD_46	GPIO[12]	SPI1_M_CS_B[1]		GPIO[12]/SPI1 Master Chip Select 1
B6	EXTERNAL_PAD_43	GPIO[9]	SPI1_M_MISO		GPIO[9]/SPI1 Master Master-In Slave-Out



Location	Ballmap Name	Function_0	Function_1	Function_2	Description
B7	EXTERNAL_PAD_36	SPI1_SS_MOSI			SPI1 Sensor Subsystem Master-Out Slave-In
B8	EXTERNAL_PAD_37	SPI1_SS_SCK			SPI1 Sensor Subsystem Clock
B9	EXTERNAL_PAD_33	SPI0_SS_CS_B[2]	GPIO[29]		SPI0 Sensor Subsystem Chip Select 2/GPIO[29]
B10	EXTERNAL_PAD_29	SPI0_SS_MOSI			SPI0 Sensor Subsystem Master-In Slave-Out
B11	EXTERNAL_PAD_25	I2C0_SS_SCL			I2C0 SensorSubsystem Serial Clock
B12	EXTERNAL_PAD_21	I2C0_SDA			I2C0 Serial Data
C1	EXTERNAL_PAD_66	GPIO_SS[13]	PWM[3]		GPIO Sensor Subsystem [13]/Pulse Width Modulation[3]
C2	EXTERNAL_PAD_62	GPIO[28]			GPIO[28]
C3	EXTERNAL_PAD_56	GPIO[22]	SPI0_M_MISO		GPIO[22]/SPI0 Master Master-In Slave-Out
C4	EXTERNAL_PAD_53	GPIO[19]	I2S_TWS		GPIO[19]/I2S Transmit Write Select
C5	EXTERNAL_PAD_49	GPIO[15]	I2S_RXD		GPIO[15]/I2S Receive
C6	EXTERNAL_PAD_45	GPIO[11]	SPI1_M_CS_B[0]		GPIO[11]/SPI1 Master Chip Select 0
C7	EXTERNAL_PAD_38	SPI1_SS_CS_B[0]			SPI1Sensor Subsystem Chip Select 0
C8	EXTERNAL_PAD_34	SPI0_SS_CS_B[3]	GPIO[30]		Chip select 3 for SPI0 on SensorSubsystem/ GPIO[30]
C9	EXTERNAL_PAD_30	SPI0_SS_SCK			SPI0 SensorSubsystem Serial Clock
C10	EXTERNAL_PAD_26	I2C1_SS_SDA			I2C1 Sensor Subsystem Serial Data
C11	EXTERNAL_PAD_23	I2C1_SDA			I2C1Serial Data
C12	EXTERNAL_PAD_20	I2C0_SCL			I2C0 Serial Clock
D1	EXTERNAL_PAD_67	GPIO_SS[14]	PLT_CLK[0]		GPIO for Sensor Subsystem[14]/ Platform Clock 0



Location	Ballmap Name	Function_0	Function_1	Function_2	Description
D2	EXTERNAL_PAD_63	GPIO_SS[10]	PWM[0]		GPIO for Sensor Subsystem[10]/ PWM[0]
D3	EXTERNAL_PAD_57	GPIO[23]	SPI0_M_MOSI		GPIO[23]/SPI0 Master Master-Out Slave-In
D4	EXTERNAL_PAD_51	GPIO[17]	I2S_RWS		GPIO[17]/I2S Receive Write Select
D5	EXTERNAL_PAD_48	GPIO[14]	SPI1_M_CS_B[3]		GPIO[14]/SPI1 Master Chip Select 3
D6	EXTERNAL_PAD_42	GPIO[8]	SPI1_M_SCK		GPIO[8]/SPI1 Master Serial Clock
D7	EXTERNAL_PAD_41	SPI1_SS_CS_B[3]	UART0_RTS_B		SPI1 Sensor Subsystem Chip Select 3/UART0 Ready to Send
D8	EXTERNAL_PAD_40	SPI1_SS_CS_B[2]	UART0_CTS_B		SPI1 Chip Select 2 on SensorSubsystem/ UART0 Clear to Send Active low
D9	EXTERNAL_PAD_32	SPI0_SS_CS_B[1]			SPI0 Sensor Subsystem Chip Select 1
D10	EXTERNAL_PAD_27	I2C1_SS_SCL			I2C1 SensorSubsystem Serial Clock
D11	EXTERNAL_PAD_22	I2C1_SCL			I2C1 Serial Clock
D12	EXTERNAL_PAD_0	GPIO[0]	AIN[0]	SPI_S_CS_B	GPIO[0]/Analog Input [0]/SPI Slave Chip Select
E1	EXTERNAL_PAD_68	GPIO_SS[15]	PLT_CLK[1]		GPIO for Sensor Subsystem[15]/ Platform Clock Output 1
E2	EXTERNAL_PAD_65	GPIO_SS[12]	PWM[2]		GPIO for Sensor Subsystem[12]/ PWM[2]
E3	EXTERNAL_PAD_59	GPIO[25]	SPI0_M_CS_B[1]		GPIO[25]/SPI0 Master Chip Select 1
E4	EXTERNAL_PAD_58	GPIO[24]	SPI0_M_CS_B[0]		GPIO[24]/ SPI0 Master Chip Select 0
E5	RST_N_PAD	RST_B			Main reset for SoC
E6	AON_GPIO_PAD_5	GPIO_AON[5]			Always on GPIO[5]
E7	VSS	VSS			Ground



Location	Ballmap Name	Function_0	Function_1	Function_2	Description
E8	EXTERNAL_PAD_18	UART0_RXD	AIN[18]		UART0 Receive/Analog Input[18]
E9	EXTERNAL_PAD_19	UART0_TXD	GPIO[31]		UART0 Transmit/GPIO[31]
E10	EXTERNAL_PAD_1	GPIO[1]	AIN[1]	SPI_S_MISO	GPIO[1]/ Analog Input [1]/SPI Slave Master-In Slave-Out
E11	EXTERNAL_PAD_2	GPIO[2]	AIN[2]	SPI_S_SCK	GPIO[2]/Analog Input [2]/SPI Slave Serial Clock
E12	EXTERNAL_PAD_3	GPIO[3]	AIN[3]	SPI_S_MOSI	GPIO[3]/Analog Input[3]/SPI slave Master-Out Slave-in
F1	AON_GPIO_PAD_4	GPIO_AON[4]			Always On GPIO [4]
F2	AON_GPIO_PAD_3	GPIO_AON[3]			Always On GPIO [3]
F3	AON_GPIO_PAD_0	GPIO_AON[0]			Always On GPIO [0]
F4	AON_GPIO_PAD_2	GPIO_AON[2]			Always On GPIO [2]
F5	AON_GPIO_PAD_1	GPIO_AON[1]			Always On GPIO [1]
F6	VCC_IO_AON	VCC_IO_AON			Ground for Always On I/O
F7	VSS	VSS			Ground
F8	VSS_RTC	VSS_RTC			RTC Ground
F9	EXTERNAL_PAD_4	GPIO[4]	AIN[4]		GPIO[4]/ Analog input[4]
F10	EXTERNAL_PAD_5	GPIO[5]	AIN[5]		GPIO[5]/Analog input[5]
F11	EXTERNAL_PAD_8	GPIO_SS[0]	AIN[8]	UART1_CTS	GPIO for Sensor Subsystem[0]/Analog In[8]/UART1 Clear to send
F12	EXTERNAL_PAD_9	GPIO_SS[1]	AIN[9]	UART1_RTS	GPIO for Sensor Subsystem[1]/Analog In[9]/UART1 Ready to Send
G1	TRST_PAD	TRST_B			JTAG reset
G2	TCK_PAD	TCK			JTAG clock
G3	TMS_PAD	TMS			JTAG master select
G4	TDI_PAD	TDI			JTAG data in
G5	AON_PWR_GOOD_PAD	VCC_HOST_1P8_PG			1.8v from platform to SoC



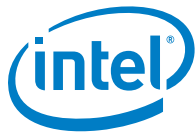
Location	Ballmap Name	Function_0	Function_1	Function_2	Description
G6	VSS_IO_AON	VSS_IO_AON			Ground for Always On I/O
G7	VSS	VSS			Ground
G8	VCC_IO_AON	VCC_IO_AON			Input voltage for Always On I/O
G9	EXTERNAL_PAD_10	GPIO_SS[2]	AIN[10]		GPIO for Sensor Subsystem[2]/Analog input[10]
G10	EXTERNAL_PAD_11	GPIO_SS[3]	AIN[11]		GPIO for Sensor Subsystem[3]/Analog Input [11]
G11	EXTERNAL_PAD_12	GPIO_SS[4]	AIN[12]		GPIO for Sensor Subsystem[4]/Analog Input[12]
G12	EXTERNAL_PAD_13	GPIO_SS[5]	AIN[13]		GPIO for Sensor Subsystem[5]/Analog Input [13]
H1	RTC_XTALO_PAD	OSC32K_OUT			
H2	RTC_XTALI_PAD	OSC32K_IN			
H3	TDO_PAD	TDO			JTAG data out
H4	VCC_AON_1P8	VCC_AON_1P8			1.8v supply voltage for Always On counter
H5	VCC_AON_1P8	VCC_AON_1P8			1.8v supply voltage for Always On counter
H6	VSS_GNDSense_ESR1	VSS_GNDSense_ESR1			Ground for switching regulator 1
H7	VCC_PLL_1P8	VCC_PLL_1P8			1.8 PLL supply voltage
H8	VSS	VSS			Ground
H9	AREF_PAD	COMP_AREF			Analog reference voltage
H10	VCC_IO_AON	VCC_IO_AON			Input voltage for Always On I/O
H11	EXTERNAL_PAD_16	GPIO_SS[8]	AIN[16]	UART1_TX	GPIO for Sensor Subsystem[8]/ Analog-In[16]/ UART1 Transmit data
H12	EXTERNAL_PAD_17	GPIO_SS[9]	AIN[17]	UART1_RX	GPIO for Sensor Subsystem[9]/ Analog[17]/UART1 Receive Data
J1	VCCOUT_AVD_OPM_2 P6	VCCOUT_AVD_O PM_2P6			2.6 Output voltage supply for OPM



Loc- ation	Ballmap Name	Function_0	Function_1	Function_2	Description
J2	VSS_GNDSense_ESR2	VSS_GNDSense_ESR2			Ground sense on switching regulator 2
J3	VSS_AVS_ESR2	VSS_AVS_ESR2			Ground for switching regulator 2
J4	VCC_RTC_1P8	VCC_RTC_1P8			1.8 supply voltage for RTC
J5	VCC_SRAM_1P8	VCC_SRAM_1P8			1.8 SRAM supply voltage
J6	VSS_AVS_ESR1	VSS_AVS_ESR1			Ground for switching regulator 1
J7	VCC_HOST_1P8	VCC_HOST_1P8			1.8v from platform to SoC
J8	VSS_AVS_ESR3	VSS_AVS_ESR3			Ground for ESR3
J9	VSS	VSS			Ground
J10	VSS_IO_AON	VSS_IO_AON			Ground for Always On I/O
J11	VSS_USB	VSS_USB			USB Ground
J12	VSS_PLL	VSS_PLL			Ground for PLL
K1	VCC_AVD_OPM_2P6	VCC_AVD_OPM_2P6			2.6 voltage supply for OPM
K2	VCC_BATT_ESR2_3P7	VCC_BATT_ESR2_3P7			Main supply voltage for Switching regulator 2
K3	REG_PLAT_PAD	PLT_REG_EN			
K4	VCCOUT_QLR2_1P8	VCCOUT_QLR2_1P8			Output voltage for linear reg2
K5	VCCOUT_QLR1_3P3	VCCOUT_QLR1_3P3			Output voltage for linear reg1
K6	VCCOUT_HOST_1P8	VCCOUT_HOST_1P8			1.8 host supply output
K7	VCC_HOST_1P8	VCC_HOST_1P8			
K8	EXTERNAL_PAD_7	GPIO[7]	AIN[7]		GPIO[7]/Analog Input [7]
K9	EXTERNAL_PAD_15	GPIO_SS[7]	AIN[15]		GPIO for Sensor Subsystem[7]/Analog Input[15]
K10	EXTERNAL_PAD_14	GPIO_SS[6]	AIN[14]		GPIO for Sensor Subsystem[6]/Analog Input[14]
K11	HYB_XTALO_PAD	OSC32M_OUT			
K12	HYB_XTALI_PAD	OSC32M_IN			



Location	Ballmap Name	Function_0	Function_1	Function_2	Description
L1	VCC_BATT_OPM_3P7	VCC_BATT_OPM_3P7			Main supply voltage for OPM
L2	VCC_BATT_ESR3_3P7	VCC_BATT_ESR3_3P7			Main supply voltage for Switching regulator 2
L3	VSS_GNDSENSE_OPM	VSS_GNDSENSE_OPM			Ground Sense for over voltage protection module
L4	VCC_VSENSE_ESR2	VCC_VSENSE_ESR2			VSense on Switching Regulator2
L5	VCC_VSENSE_ESR1	VCC_VSENSE_ESR1			VSense on Switching Regulator1
L6	VCC_VSENSE_ESR3	VCC_VSENSE_ESR3			VSense on Switching Regulator3
L7	VCC_HOST_1P8	VCC_HOST_1P8			1.8v from platform to SoC
L8	VSS_AVSS_CMP	VSS_AVSS_CMP			Comparator ground
L9	EXTERNAL_PAD_6	GPIO[6]	AIN[6]		GPIO[6]/Analog Input [6]
L10	VSS_ADC_AGND	VSS_ADC_AGND			ADC ground
L11	USB_PADP	USB_DP			USB positive
L12	VCC_USB_3P3	VCC_USB_3P3			3.3 supply voltage for USB
M1	VSS	VSS			Ground
M2	VCC_BATT_ESR1_3P7	VCC_BATT_ESR1_3P7			Mains supply voltage for ESR1
M3	VCCOUT_AON_1P8	VCCOUT_AON_1P8			1.8 Always On Supply voltage
M4	VCCOUT_ESR2_1P8	VCCOUT_ESR2_1P8			Output voltage for switching reg2
M5	VCCOUT_ESR1_3P3	VCCOUT_ESR1_3P3			Output voltage for switching reg1
M6	VCCOUT_ESR3_1P8	VCCOUT_ESR3_1P8			1.8 Supply voltage for switching regulator 3
M7	VSS_GNDSENSE_ESR3	VSS_GNDSENSE_ESR3			Ground Sense for switching regulator 3
M8	VCC_CMP_3P3	VCC_CMP_3P3			3.3 comparators supply voltage
M9	VSS_AVSS_CMP	VSS_AVSS_CMP			Ground for comparators



Location	Ballmap Name	Function_0	Function_1	Function_2	Description
M10	VCC_ADC_3P3	VCC_ADC_3P3			3.3 ADC supply voltage
M11	USB_PADN	USB_DN			USB negative
M12	VSS	VSS			Ground

3.7 Alphabetical Function Listing For BGA Package

Table 14. Alphabetical Function Listing for BGA Package

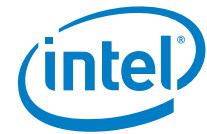
Location	Ballmap Name	Function_0	Function_1	Function_2
H9	AREF_PAD	COMP_AREF		
D12	EXTERNAL_PAD_0	GPIO[0]	AIN[0]	SPI_S_CS_B
E10	EXTERNAL_PAD_1	GPIO[1]	AIN[1]	SPI_S_MISO
A6	EXTERNAL_PAD_44	GPIO[10]	SPI1_M_MOSI	
C6	EXTERNAL_PAD_45	GPIO[11]	SPI1_M_CS_B[0]	
B5	EXTERNAL_PAD_46	GPIO[12]	SPI1_M_CS_B[1]	
A5	EXTERNAL_PAD_47	GPIO[13]	SPI1_M_CS_B[2]	
D5	EXTERNAL_PAD_48	GPIO[14]	SPI1_M_CS_B[3]	
C5	EXTERNAL_PAD_49	GPIO[15]	I2S_RXD	
B4	EXTERNAL_PAD_50	GPIO[16]	I2S_RSCK	
D4	EXTERNAL_PAD_51	GPIO[17]	I2S_RWS	
A4	EXTERNAL_PAD_52	GPIO[18]	I2S_TSCK	
C4	EXTERNAL_PAD_53	GPIO[19]	I2S_TWS	
E11	EXTERNAL_PAD_2	GPIO[2]	AIN[2]	SPI_S_SCK
B3	EXTERNAL_PAD_54	GPIO[20]	I2S_TXD	
A3	EXTERNAL_PAD_55	GPIO[21]	SPIO_M_SCK	
C3	EXTERNAL_PAD_56	GPIO[22]	SPIO_M_MISO	
D3	EXTERNAL_PAD_57	GPIO[23]	SPIO_M_MOSI	
E4	EXTERNAL_PAD_58	GPIO[24]	SPIO_M_CS_B[0]	
E3	EXTERNAL_PAD_59	GPIO[25]	SPIO_M_CS_B[1]	
B2	EXTERNAL_PAD_60	GPIO[26]	SPIO_M_CS_B[2]	
A2	EXTERNAL_PAD_61	GPIO[27]	SPIO_M_CS_B[3]	
C2	EXTERNAL_PAD_62	GPIO[28]		



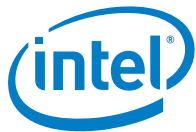
Location	Ballmap Name	Function_0	Function_1	Function_2
E12	EXTERNAL_PAD_3	GPIO[3]	AIN[3]	SPI_S_MOSI
F9	EXTERNAL_PAD_4	GPIO[4]	AIN[4]	
F10	EXTERNAL_PAD_5	GPIO[5]	AIN[5]	
L9	EXTERNAL_PAD_6	GPIO[6]	AIN[6]	
K8	EXTERNAL_PAD_7	GPIO[7]	AIN[7]	
D6	EXTERNAL_PAD_42	GPIO[8]	SPI1_M_SCK	
B6	EXTERNAL_PAD_43	GPIO[9]	SPI1_M_MISO	
F3	AON_GPIO_PAD_0	GPIO_AON[0]		
F5	AON_GPIO_PAD_1	GPIO_AON[1]		
F4	AON_GPIO_PAD_2	GPIO_AON[2]		
F2	AON_GPIO_PAD_3	GPIO_AON[3]		
F1	AON_GPIO_PAD_4	GPIO_AON[4]		
E6	AON_GPIO_PAD_5	GPIO_AON[5]		
F11	EXTERNAL_PAD_8	GPIO_SS[0]	AIN[8]	UART1_CTS
F12	EXTERNAL_PAD_9	GPIO_SS[1]	AIN[9]	UART1_RTS
D2	EXTERNAL_PAD_63	GPIO_SS[10]	PWM[0]	
B1	EXTERNAL_PAD_64	GPIO_SS[11]	PWM[1]	
E2	EXTERNAL_PAD_65	GPIO_SS[12]	PWM[2]	
C1	EXTERNAL_PAD_66	GPIO_SS[13]	PWM[3]	
D1	EXTERNAL_PAD_67	GPIO_SS[14]	PLT_CLK[0]	
E1	EXTERNAL_PAD_68	GPIO_SS[15]	PLT_CLK[1]	
G9	EXTERNAL_PAD_10	GPIO_SS[2]	AIN[10]	
G10	EXTERNAL_PAD_11	GPIO_SS[3]	AIN[11]	
G11	EXTERNAL_PAD_12	GPIO_SS[4]	AIN[12]	
G12	EXTERNAL_PAD_13	GPIO_SS[5]	AIN[13]	
K10	EXTERNAL_PAD_14	GPIO_SS[6]	AIN[14]	
K9	EXTERNAL_PAD_15	GPIO_SS[7]	AIN[15]	
H11	EXTERNAL_PAD_16	GPIO_SS[8]	AIN[16]	UART1_TX
H12	EXTERNAL_PAD_17	GPIO_SS[9]	AIN[17]	UART1_RX
C12	EXTERNAL_PAD_20	I2C0_SCL		
B12	EXTERNAL_PAD_21	I2C0_SDA		
B11	EXTERNAL_PAD_25	I2C0_SS_SCL		
A11	EXTERNAL_PAD_24	I2C0_SS_SDA		
D11	EXTERNAL_PAD_22	I2C1_SCL		



Location	Ballmap Name	Function_0	Function_1	Function_2
C11	EXTERNAL_PAD_23	I2C1_SDA		
D10	EXTERNAL_PAD_27	I2C1_SS_SCL		
C10	EXTERNAL_PAD_26	I2C1_SS_SDA		
H2	RTC_XTALI_PAD	OSC32K_IN		
H1	RTC_XTALO_PAD	OSC32K_OUT		
K12	HYB_XTALI_PAD	OSC32M_IN		
K11	HYB_XTALO_PAD	OSC32M_OUT		
K3	EG_PLAT_PAD	PLT_REG_EN		
E5	RST_N_PAD	RST_B		
A9	EXTERNAL_PAD_31	SPI0_SS_CS_B[0]		
D9	EXTERNAL_PAD_32	SPI0_SS_CS_B[1]		
B9	EXTERNAL_PAD_33	SPI0_SS_CS_B[2]	GPIO[29]	
C8	EXTERNAL_PAD_34	SPI0_SS_CS_B[3]	GPIO[30]	
A10	EXTERNAL_PAD_28	SPI0_SS_MISO		
B10	EXTERNAL_PAD_29	SPI0_SS_MOSI		
C9	EXTERNAL_PAD_30	SPI0_SS_SCK		
C7	EXTERNAL_PAD_38	SPI1_SS_CS_B[0]		
A7	EXTERNAL_PAD_39	SPI1_SS_CS_B[1]		
D8	EXTERNAL_PAD_40	SPI1_SS_CS_B[2]	UART0_CTS_B	
D7	EXTERNAL_PAD_41	SPI1_SS_CS_B[3]	UART0_RTS_B	
A8	EXTERNAL_PAD_35	SPI1_SS_MISO		
B7	EXTERNAL_PAD_36	SPI1_SS_MOSI		
B8	EXTERNAL_PAD_37	SPI1_SS_SCK		
G2	TCK_PAD	TCK		
G4	TDI_PAD	TDI		
H3	TDO_PAD	TDO		
G3	TMS_PAD	TMS		
G1	TRST_PAD	TRST_B		
E8	EXTERNAL_PAD_18	UART0_RXD	AIN[18]	
E9	EXTERNAL_PAD_19	UART0_TXD	GPIO[31]	
M11	USB_PADN	USB_DN		
L11	USB_PADP	USB_DP		
M10	VCC_ADC_3P3	VCC_ADC_3P3		
H4	VCC_AON_1P8	VCC_AON_1P8		



Location	Ballmap Name	Function_0	Function_1	Function_2
H5	VCC_AON_1P8	VCC_AON_1P8		
K1	VCC_AVD_OPM_2P6	VCC_AVD_OPM_2P6		
M2	VCC_BATT_ESR1_3P7	VCC_BATT_ESR1_3P7		
K2	VCC_BATT_ESR2_3P7	VCC_BATT_ESR2_3P7		
L2	VCC_BATT_ESR3_3P7	VCC_BATT_ESR3_3P7		
L1	VCC_BATT_OPM_3P7	VCC_BATT_OPM_3P7		
M8	VCC_CMP_3P3	VCC_CMP_3P3		
J7	VCC_HOST_1P8	VCC_HOST_1P8		
K7	VCC_HOST_1P8	VCC_HOST_1P8		
L7	VCC_HOST_1P8	VCC_HOST_1P8		
G5	AON_PWR_GOOD_PAD	VCC_HOST_1P8_PG		
F6	VCC_IO_AON	VCC_IO_AON		
G8	VCC_IO_AON	VCC_IO_AON		
H10	VCC_IO_AON	VCC_IO_AON		
H7	VCC_PLL_1P8	VCC_PLL_1P8		
J4	VCC_RTC_1P8	VCC_RTC_1P8		
J5	VCC_SRAM_1P8	VCC_SRAM_1P8		
L12	VCC_USB_3P3	VCC_USB_3P3		
L5	VCC_VSENSE_ESR1	VCC_VSENSE_ESR1		
L4	VCC_VSENSE_ESR2	VCC_VSENSE_ESR2		
L6	VCC_VSENSE_ESR3	VCC_VSENSE_ESR3		
M3	VCCOUT_AON_1P8	VCCOUT_AON_1P8		
J1	VCCOUT_AVD_OPM_2P6	VCCOUT_AVD_OPM_2P6		
M5	VCCOUT_ESR1_3P3	VCCOUT_ESR1_3P3		
M4	VCCOUT_ESR2_1P8	VCCOUT_ESR2_1P8		
M6	VCCOUT_ESR3_1P8	VCCOUT_ESR3_1P8		
K6	VCCOUT_HOST_1P8	VCCOUT_HOST_1P8		
K5	VCCOUT_QLR1_3P3	VCCOUT_QLR1_3P3		
K4	VCCOUT_QLR2_1P8	VCCOUT_QLR2_1P8		
A1	VSS	VSS		
A12	VSS	VSS		
E7	VSS	VSS		
F7	VSS	VSS		



Location	Ballmap Name	Function_0	Function_1	Function_2
G7	VSS	VSS		
H8	VSS	VSS		
J9	VSS	VSS		
M1	VS	VSS		
M12	VSS	VSS		
L10	VSS_ADC_AGND	VSS_ADC_AGND		
J6	VSS_AVS_ESR1	VSS_AVS_ESR1		
J3	VSS_AVS_ESR2	VSS_AVS_ESR2		
J8	VSS_AVS_ESR3	VSS_AVS_ESR3		
L8	VSS_AVSS_CMP	VSS_AVSS_CMP		
M9	VSS_AVSS_CMP	VSS_AVSS_CMP		
H6	VSS_GNDSSENSE_ESR1	VSS_GNDSSENSE_ESR 1		
J2	VSS_GNDSSENSE_ESR2	VSS_GNDSSENSE_ESR 2		
M7	VSS_GNDSSENSE_ESR3	VSS_GNDSSENSE_ESR 3		
L3	VSS_GNDSSENSE_OPM	VSS_GNDSSENSE_OP M		
G6	VSS_IO_AON	VSS_IO_AON		
J10	VSS_IO_AON	VSS_IO_AON		
J12	VSS_PLL	VSS_PLL		
F8	VSS_RTC	VSS_RTC		
J11	VSS_USB	VSS_USB		



4 Electrical Characteristics

4.1 Voltage and Current Specifications

4.1.1 Absolute Maximum Ratings

Supply voltage ($V_{CC\_BATT\_OPM\_3P7}$).....	-0.3 V to 4.4 V
Analog input voltage (V_{CC_ADC}).....	-0.3 V to 3.63 V
USB input voltage (V_{USB}).....	-0.3 V to 3.63 V
Operating case temperature TC (WLCSP).....	-25°C to + 70°C
Operating case temperature TC (BGA).....	-40°C to + 85°C
Storage temperature range	-40°C to 110°C
T_{jmax}	110°C
ESD	HBM $\pm$ 2000V

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 15. Typical Voltage Range

Symbol	Ratings	Min	Typ	Max	Units
VCC_BATT_OPM_3P7	Battery Supply	1.9	3.7	4.4	V
VCC_BATT_PLAT_3P3_3P7	Battery Supply	1.9	3.7	4.4	V
VCC_BATT_PLAT_1P8_3P7	Battery Supply	1.9	3.7	4.4	V
VCC_BATT_HOST_1P8_3P7	Battery Supply	1.9	3.7	4.4	V
VCC_AVD_OPM_2P6	Overvoltage Protection Supply	1.9	2.6	2.86	V
VCC_AON_1P8	AON Rail	1.63	1.8	1.98	V
VCC_HOST_1P8	AON Rail	1.63	1.8	1.98	V
VCC_VSENSE_PLAT_3P3	Sense voltage	2.97		3.63	V
VCC_VSENSE_PLAT_1P8	Sense voltage	1.63		1.98	V
VCC_VSENSE_HOST_1P8	Sense voltage	VCC_HOST_1P8		VCC_HOST_1P8	V
VCC_SRAM_1P8	SRAM voltage supply	1.63	1.8	1.98	V
VCC_IO_AON	IO voltage supply	1.63		3.63	V
VCC_ADC	ADC voltage supply	1.63		3.63	V



Symbol	Ratings	Min	Typ	Max	Units
VCC_CMP	Comparator voltage supply	2.0		3.63	V
VCC_PLL_1P8	PLL clock voltage	1.63	1.8	1.98	V
VCC_RTC_1P8	RTC clock voltage	1.63	1.8	1.98	V
VCC_USB_3P3	USB IO voltage	2.97	3.3	3.63	V

NOTES:

- VCC_AVD_OPM_2P6 has a range of 1.9V to 2.86V but with the following restrictions:
 - When VCC_BATT_3P7 is less than 2.6V, VCC_AVD_OPM must be equal to VCC_BATT_3P7.
 - When VCC_BATT_3P7 is higher than 2.6V, VCC_AVD_OPM must be equal to 2.6V.
- The Special care must be taken in the event of a hardware power down of V_{sys} followed by a power up sequence. Please ensure that The Intel® Quark™ SE C1000 Microcontroller reference voltage OPM_2P6 is discharged to ground before a power up cycle. Refer to The Intel® Quark™ SE Microcontroller C1000: Platform Design Guide (Document - 334715) for further details.

4.2 Crystal Specifications

Table 16. 32 MHz Crystal Oscillator Specifications

Symbol	Parameter	Min	Typ	Max	Units
Fo	Crystal frequency	32	32	32	MHz
Cesr	Crystal ESR	12.68	14.41	50	Ω
Cm	Crystal Motional Cap	3.34		3.54	pF
Co	Crystal Shunt Cap	0.84		1.5	pF
CL	Crystal Load Cap		10		pF
Ftol	Frequency Tolerance	-30		30	ppm
Dlev	Drive Level (25Ω)			10	uW

Table 17. 32 KHz Crystal Oscillator Specifications

Symbol	Parameter	Min	Typ	Max	Units
Fo	Crystal frequency		32,768		Hz
Cesr	Crystal ESR		50	80	kΩ
Cm	Crystal Motional Cap		3.7		pF
Co	Crystal Shunt Cap		1.2		pF
CL	Crystal Load Cap		7		pF
Ftol	Frequency Tolerance	-20		20	ppm
Dlev	Drive Level			1	uW



4.3 DC Specifications

4.3.1 IO DC Specifications

Table 18. Always On 3.3 Voltage Specifications

Symbol	Parameter	Min	Typ	Max	Units
VIL	Input Low Voltage	-0.3		0.8	V
VIH	Input High Voltage	2		3.6	V
VOL	Output Low Voltage			0.4	V
VOH	Output High Voltage	2.4			V
IOL	2mA @ VOL	2.4	3.8	5.3	mA
	4mA @ VOL	4.7	7.6	10.6	mA
	8mA @ VOL	9.4	15.3	21.2	mA
IOH	2mA @ VOH	3.4	7.0	11.6	mA
	4mA @ VOH	6.9	14.0	23.2	mA
	8mA @ VOH	13.8	27.9	46.4	mA
RPU	Pull-up Resistor	34K	49K	74K	Ω
VT	Threshold Point	1.33	1.4	1.47	V
VT+	L-> H Threshold Point	1.53	1.6	1.66	V
VT-	H-> L Threshold Point	1.13	1.2	1.27	V

Table 19. Always On 1.8 Voltage Specifications

Symbol	Parameter	Min	Typ	Max	Units
VIL	Input Low Voltage	-0.3		0.63	V
VIH	Input High Voltage	1.17		TBC	V
VOL	Output Low Voltage			0.45	V
VOH	Output High Voltage	1.35			V
IOL	2mA @ VOL	1.0	2.0	3.6	mA
	4mA @ VOL	1.9	4.0	7.2	mA
	8mA @ VOL	3.9	8.1	14.4	mA
IOH	2mA @ VOH	0.8	2.0	4.1	mA
	4mA @ VOH	1.6	4.0	8.1	mA
	8mA @ VOH	3.2	8.0	16.2	mA
RPU	Pull-up Resistor	34K	49K	74K	Ω
VT	Threshold Point	0.82	0.89	0.93	V
VT+	L-> H Threshold Point	0.99	1.07	1.12	V



Symbol	Parameter	Min	Typ	Max	Units
VT-	H-> L Threshold Point	0.62	0.69	0.77	V

4.3.2 ADC IO DC Characteristics

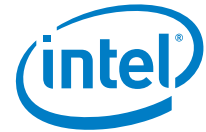
Table 20. ADC IO DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
	Full-scale input range	AGNDREF		3.63	V
VREFP	Positive reference voltage	2	VCC_ADC	VCC_ADC	V
AGNDREF	Negative reference voltage	0	0	0.1	V
ADC_cap	Input sampling capacitance		5		pF
ENOB	Effective number of bits		10		bits
SNR	Signal-to-noise ratio	63	64		dB
SINAD	Signal-to-noise and distortion ratio	63	64		dB
THD	Total harmonic distortion	-64	-65		dB
Gain Error			0.23%	0.3%	

4.3.3 USB IO DC Characteristics

Table 21. USB IO DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
VIL	Input Low Voltage			0.8	V
VIH	Input High Voltage	2.0			V
VOL	Output Low Voltage			0.3	V
VOH	Output High Voltage	2.8			V
VCRS	Differential output signal cross-point voltage	1.3		2.0	V
VCM	Common mode voltage range	0.8		2.5	V
RPU	External pull-up resistor	1.425		1.575	Ω
Vtrm	Termination voltage connected to Rpu	3.0		3.6	V



4.4 AC Specifications

4.4.1 USB IO AC Characteristics

Table 22. USB IO AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
TFR	Rise Time 50pF	4		20	ns
TFF	Fall Time 50pF	4		20	ns
TFRFF	Rise/Fall matching	90		111.11	%

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5 Register Access Methods

5.1 Fixed Memory Mapped Register Access

You can access fixed Memory Mapped IO (MMIO) registers by specifying their 32-bit address in a memory transaction from the CPU core. This allows you to manipulate the registers directly. Fixed MMIO registers are unmovable registers in memory space.

5.2 Register Field Access Types

Table 23. Register Access Types and Definitions

Access Type	Meaning	Description
RO	Read Only	In some cases, if a register is read only, writes to this register location have no effect. In other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the register descriptions for details.
WO	Write Only	In some cases, if a register is write only, reads to this register location have no effect. In other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the register descriptions for details.
R/W	Read/Write	You can read and write the register.
R/WC	Read/Write Clear	You can read and write the register bit. However, a write of 1 clears (that is, sets to 0) the corresponding bit and a write of 0 has no effect.
R/WO	Read/Write-Once	You can write the register bit only once after power up or coming back from reset. After the first write, the bit becomes read only.
R/WLO	Read/Write, Lock-Once	You can write the register bit to the non-locked value multiple times, but to the locked value only once. The bit becomes read-only when the locked value is written.
RW/V	Read/Write, hardware clear	You can read and write the register bit. This is a trigger bit: a write of 1 sets the corresponding bit (that is, sets it to 1), which is then cleared by hardware. A write of 0 has no effect.
RO/V	Read Only, hardware modify	You can only read the register bit. A write has no effect. Hardware can modify this bit type.
RO/C/V	Read Only, Read Clear, hardware modify	You can only read the register bit. A read clears this bit (that is, sets it to 0). Hardware can modify this bit type.
RW/1S	Read/write 1 to set	You can read and write the register bit. A write of 1 sets this bit (that is, sets it to 1). After being set, you can only clear it by a reset.
RW/L	Read/write lock	You can read and write the register bit. You can also lock it so further writes are blocked. Typically, you enable the lock by a RW/1S register bit.



Access Type	Meaning	Description
RW/1C/V	Read/Write	You can read and write the register. Writing 1 clears the register (that is, sets it to 0). Hardware can load the register.
Reserved	Reserved	Do not change the value of reserved bits.
Default	Default	When the processor resets, it sets its registers to predetermined default states. The default state represents the minimum functionality feature set that is required to bring up the system successfully. Hence, it does not represent the optimal system configuration. The system initialization software determines the configuration, operating parameters, and optional system features that are applicable, and programs the processor registers accordingly.
RW/P/L	Read/Write, Lock	You can read and write the register bit. You can also lock it to block further writes. Typically, you enable the lock by a RW/1S register bit. This access type retains its value through a warm reset.
RW/P	Read/Write	You can read and write the register bit. This access type retains its value through a warm reset.
RW/1C/V/P	Read/Write, hardware modify	You can read and write the register bit. Writing 1 clears the register (that is, sets it to 0). Hardware can load the register. This access type retains its value through a warm reset.
RO/V/P	Read Only, hardware modify	You can only read the register bit. A write has no effect. Hardware can modify this bit type. This access type retains its value through a warm reset.

6 Mapping Address Spaces

6.1 Physical Address Spaces

There are 4 GB (32-bits) of physical address space that can be used as the following:

- Memory Mapped I/O (MMIO – I/O fabric)
- Physical Memory (System Flash/System SRAM)

The processor core can access the full physical address space. Other devices within the Intel® Quark™ SE Microcontroller C1000 can only access regions of physical address space that are presented to the device by the multi-layer Intel® Quark™ SE microcontroller fabric.

All Intel® Quark™ SE microcontroller peripherals map their registers and memory to physical address space. This chapter summarizes the possible mappings.

The Sensor Subsystem core maps directly attached peripherals to an auxiliary address space, to which the sensor subsystem core has exclusive access.

6.1.1 Intel® Quark™ SE Microcontroller C1000 Memory Map

The Intel® Quark™ SE Microcontroller C1000 memory map is divided up as follows:

- Processor Local APIC (LAPIC)
- Sensor Subsystem Data CCM (DCCM)
- System Flash (Flash0, Flash1 and ROM)
- System SRAM (Internal)
- Intel® Quark™ SE microcontroller Peripherals
- I/O APIC

The CPU reset vector is located in ROM. The Sensor Subsystem core reset vector is located in Internal SRAM.

Table 24. Intel® Quark™ SE Microcontroller C1000 Memory Map

0xFFFFFFFF		
0xFFFFE000	sys_flash_rom(8KB)	sys_flash_0
0xFEE01000	Reserved	
0xFEE00000	lapic(4KB)	Quark™ SE MCU
0xFED00000	Reserved	
0xFEC00000	ioapic(1MB)	Quark™ SE MCU



0xFFFFFFFF		
0xFFFFE000	sys_flash_rom(8KB)	sys_flash_0
0xB0804000	Reserved	
0xB0800000	scss_(16KB)	scss
0xB0701000	Reserved	
0xB0700000	dma(4KB)	dma
0xB0600400	Reserved	
0xB0540000	Reserved	
0xB0500000	USB(256KB)	usb
0xB0400400	Reserved	
0xB0400000	sram_reg(1KB)	sram
0xB0300400	Reserved	
0xB0300000	extsram_cfg(1KB)	sram
0xB0200400	Reserved	
0xB0200000	sys_flash1_reg(1KB)	sys_flash_1
0xB0100400	Reserved	
0xB0100000	sys_flash0_reg(1KB)	sys_flash_0
0xB0020000	Reserved	
0xB0000000	periph(128KB)	periph
0xA8014000	Reserved	
0xA8000000	sram_mem(80KB)	sram
0xA4000000	Reserved	
0xA0000000	Reserved	
0x80002000	Reserved	
0x80000000	ss_dccm(8KB)	ss_dccm
0x40060000	Reserved	
0x40030000	sys_flash1_flash(192KB)	sys_flash1
0x40000000	sys_flash0_flash(192KB)	sys_flash0
0x00000000	Reserved	

NOTES:

1. The CPU Reset Vector is located in ROM at address 0xFFFF_FFF0.
2. The Sensor Subsystem core Reset Vector is located in internal SRAM at address 0xA800_0000.
3. All memory regions not covered in this memory map are reserved. Reserved regions are unused. The reserved sections allow increased space for memory/peripheral address space in derivative microcontrollers without re-arranging the address map.



6.1.2 IO Fabric (MMIO) Map

The IO fabric routes memory accesses based on fixed memory ranges that map to the Intel® Quark™ SE microcontroller peripherals.

The fixed regions assigned to each peripheral are listed below. See the register maps of all peripheral devices for details.

Table 25. Fixed Memory Ranges for Intel® Quark™ SE Microcontroller C1000 MMIO Peripherals

0xB0003C00	Reserved
0xB0003800	APB_I2S(1KB)
0xB0003400	Reserved
0xB0003000	Reserved
0xB0002C00	APB_I2C_M_1(1KB)
0xB0002800	APB_I2C_M_0(1KB)
0xB0002400	APB_UART_B(1KB)
0xB0002000	APB_UART_A(1KB)
0xB0001C00	Reserved
0xB0001800	APB_SSI_S_0(1KB)
0xB0001400	APB_SSI_M_1(1KB)
0xB0001000	APB_SSI_M_0(1KB)
0xB0000C00	APB_GPIO(1KB)
0xB0000800	APB_TIMER(1KB)
0xB0000400	APB_RTC(1KB)
0xB0000000	APB_WDT(1KB)

6.1.3 Sensor Subsystem Auxiliary Memory Map

The Sensor Subsystem core has access to two physically separate memory spaces. The first space is the main memory space and is shared with the host processor and Intel® Quark™ SE microcontroller peripherals. The second space is an auxiliary memory space that the sensor subsystem core uses to access peripherals that are directly connected to the Sensor Subsystem.

Only the sensor subsystem core can access the auxiliary memory space. All addresses to the auxiliary memory space are DWORD addresses, so this design can support up to 2^{32} 32 bit auxiliary registers.

At a programming level, you use two sets of instructions to access each memory space. To access the main memory space, use LD/ST instructions for load/store operations. To access auxiliary memory space, use LR/SR instructions for load/store operations.



At the C programming level, all addresses map to LD/ST instructions (that is, the main memory map). Therefore, for generic C code the compiler always generates LD/ST instructions.

To get auxiliary address access from C, use the `_sr()` and `_lr()` intrinsics and explicitly specify the auxiliary address. In the case of the Sensor Subsystem peripheral auxiliary registers, the use of the auxiliary address is hidden within the peripheral driver code.

The fixed regions assigned to each sensor subsystem peripheral are listed below. See the register maps of sensor subsystem peripheral devices for details.

Note: The main memory space and the auxiliary memory space are physically separate spaces. This means address 80000000h in main memory is physically separate from address 80000000h in auxiliary memory.

Table 26. Fixed Memory Ranges for Sensor Subsystem Peripherals

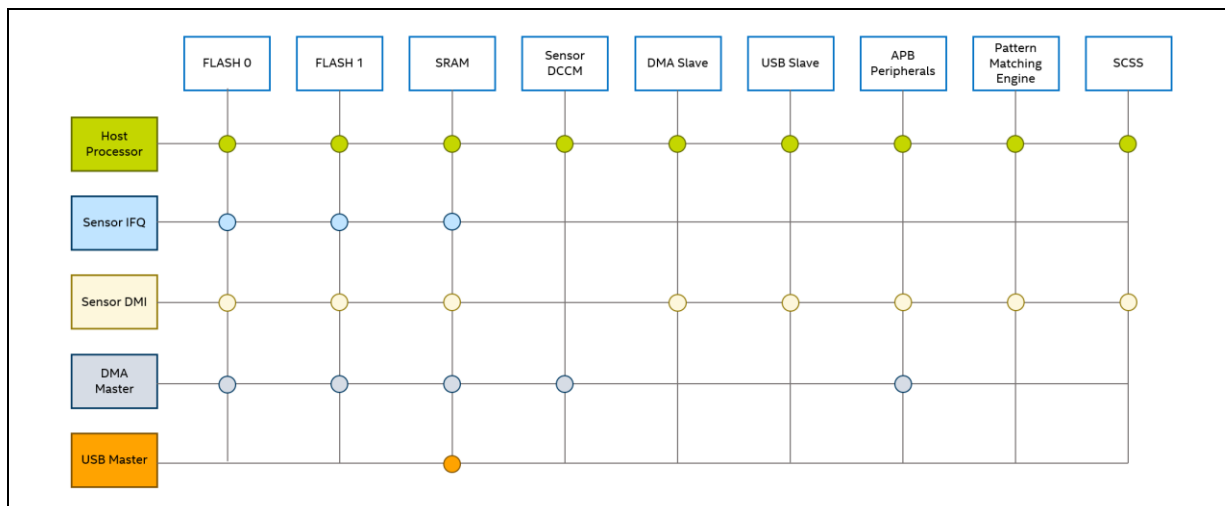
Device	Start Address	End Address
ADC	80015000h	80015005h
CREG_MST0	80018000h	80018000h
CREG_SLV0	80018080h	80018080h
CREG_SLV1	80018180h	80018180h
IO_GPIO0	80017800h	8001780Ah
IO_GPIO1	80017900h	8001790Ah
I2C_MST0	80012000h	80012011h
I2C_MST1	80012100h	80012118h
SPI_MST0	80010000h	8001000dh
SPI_MST1	80010100h	8001010dh

6.2 Intel® Quark™ SE Microcontroller C1000 Fabric

The Intel® Quark™ SE Microcontroller C1000 fabric is a multi-layer AHB fabric that provides an interconnect matrix between 5 Masters and 10 Slaves.

The multi-layer fabric allows multiple masters to access different slaves in parallel. When two or more masters try to access the same slave simultaneously, the slave arbitrates between the masters. With this topology, it is not possible for each master to access every slave connected to the Intel® Quark™ SE Microcontroller C1000 fabric.

Figure 5. Microcontroller Slaves Accessible by Microcontroller Masters



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7 Clocking

The Clock Control Unit (CCU) controls clocking in the Intel® Quark™ SE Microcontroller C1000. There are three primary clocks in the Intel® Quark™ SE Microcontroller C1000: a System clock, a USB clock, and an RTC clock. The sources and frequencies of the primary clocks are described in subsequent sections. For low power operation, the CCU supports Dynamic frequency scaling (DFS) and Dynamic clock gating (DCG).

Figure 6. Clocking

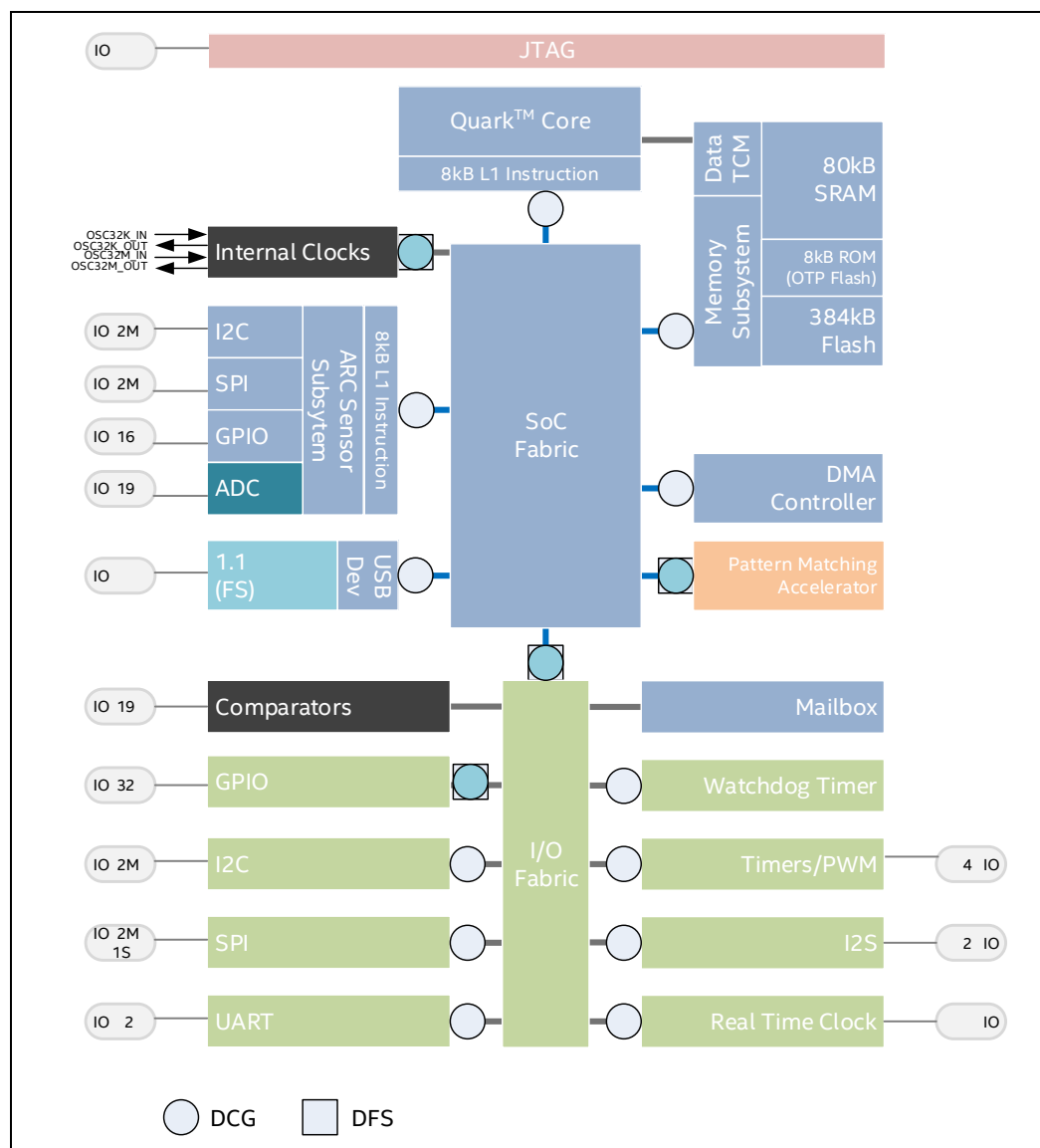


Figure 7. Clocking in Detail (1)

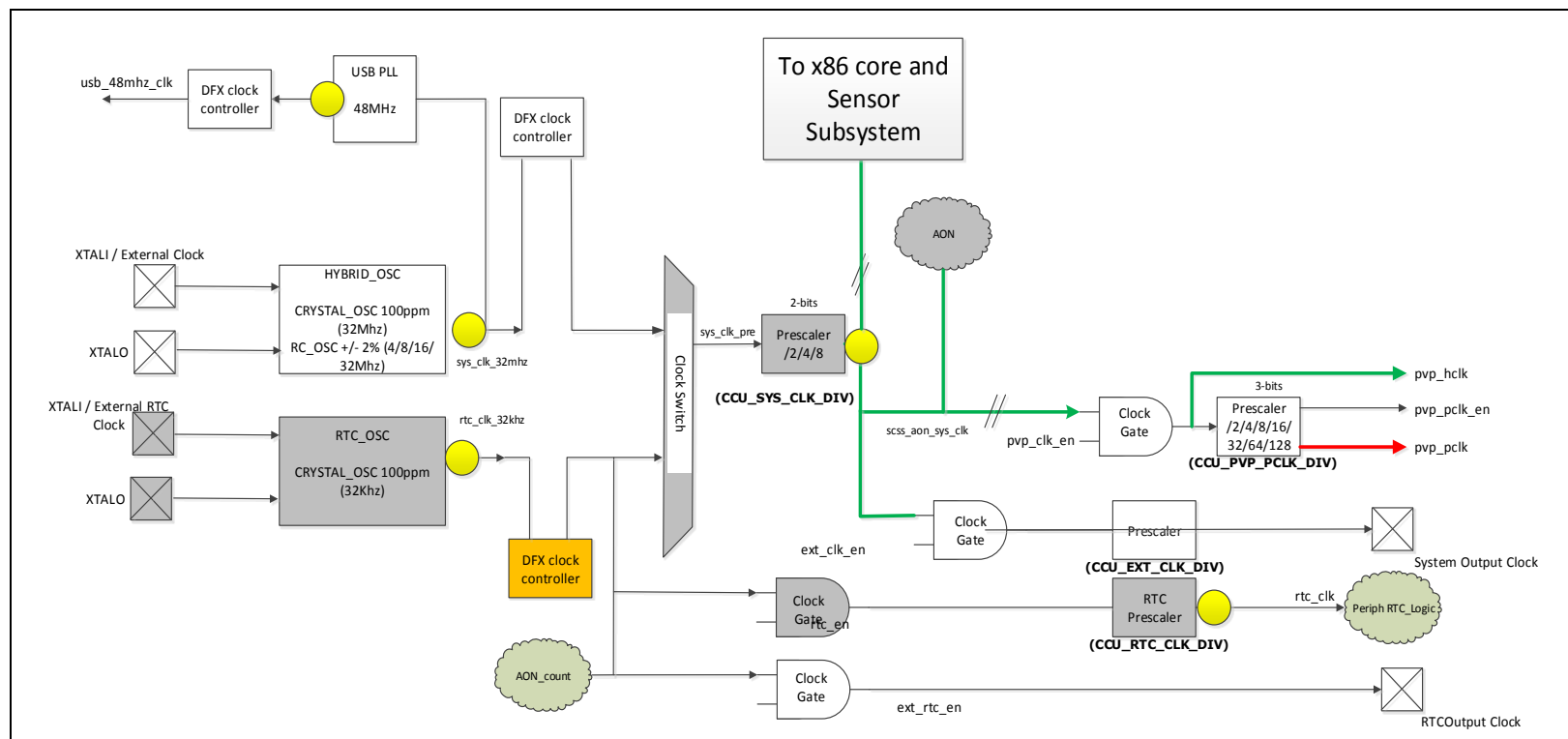
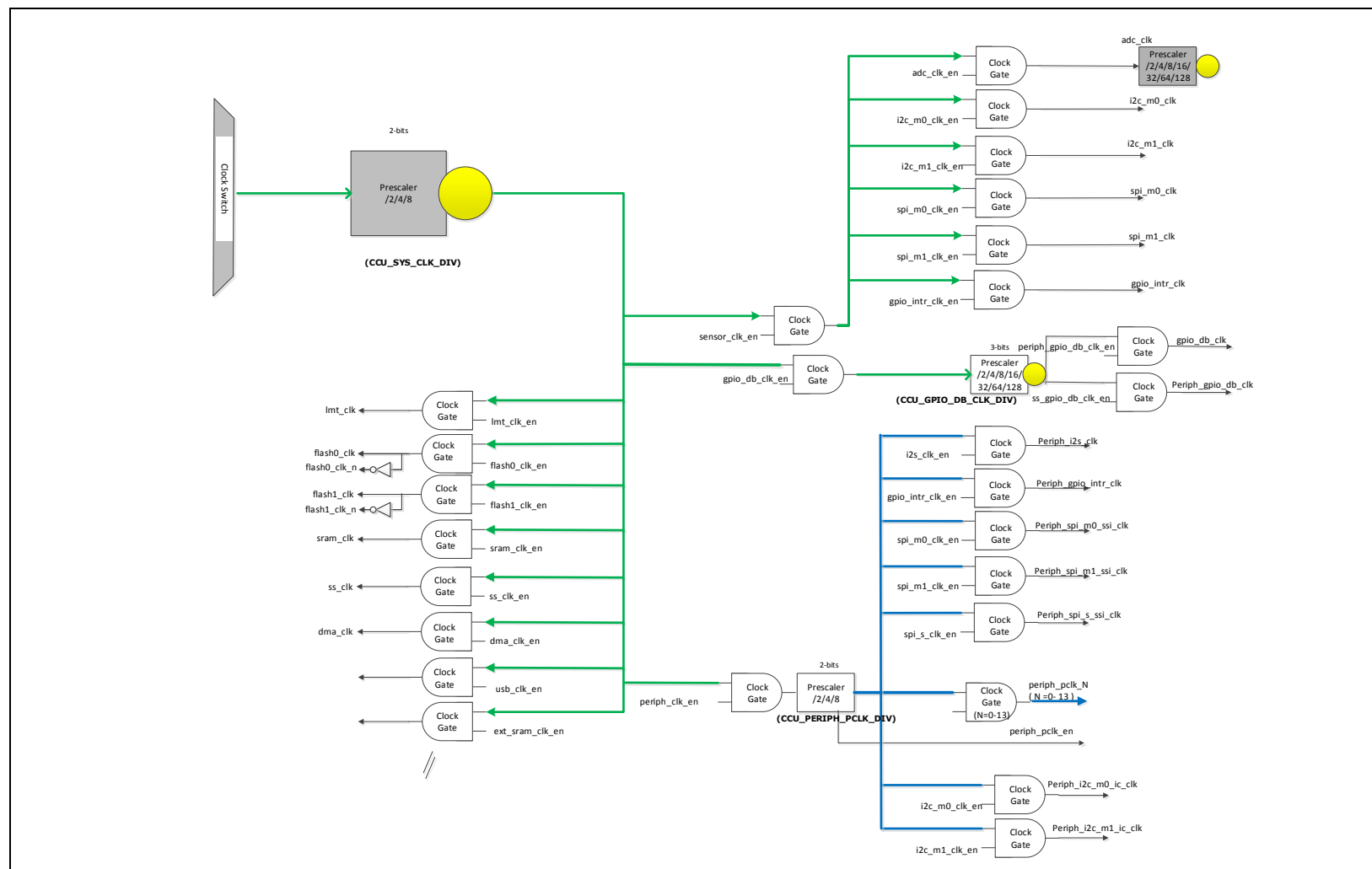


Figure 8. Clocking in Detail (2)



7.1 Signal Descriptions

Table 27. Memory Subsystem Signals

Signal Name	Direction/ Type	Description
External Crystal Interface		
HYB_XTALI	I/O	XTAL input or External system clock
HYB_XTALO	I/O	XTAL input
RTC_XTALI	I/O	RTC XTAL input
RTC_XTALO	I/O	RTC XTAL input
RTC_CLK	O	RTC Clock output
SYS_CLK	O	System Clock

7.2 Features

The CCU supports the following features:

- Dynamic frequency scaling (DFS)
- Dynamic clock gating (DCG)
- Generate a 32.768KHz RTC clock from an internal crystal oscillator
- Generate a 48MHz USB clock from an internal PLL
- Generate a system clock from an internal hybrid oscillator.

7.2.1 System Clock – Hybrid Oscillator

When the system clock is sourced internally, a hybrid oscillator generates the clock. The hybrid oscillator can run in two modes, crystal or silicon, depending on the frequency accuracy and current consumption requirements of the application. The hybrid oscillator contains the follow features:

- Crystal mode
 - Generates 32 MHz clock
 - +/-100ppm (dependent on crystal frequency tolerance)
 - 2ms start-up time to reach +/-100ppm accuracy
- Silicon mode
 - Generates 4/8/16/32 MHz clock
 - One time 10-bit factory trim
 - +/-20,000ppm (after process trim)
 - Temperature compensation block to limit frequency variation
 - 2us start-up time to reach +/-20,000ppm accuracy



- 4mA @ 32MHz in crystal mode
- 450uA @ 32 MHz in silicon mode
- 180uA @ 4 MHz in silicon mode
- 300nA power down leakage current
- Operates with a supply range of 1.62-1.98V
- Outputs a rail-to-rail swing of 1.62-1.98V
- Power down mode to reduce power consumption within the Intel® Quark™ SE Microcontroller C1000
- Glitch free mux for switching between hybrid and crystal oscillator clocks
- Bypass mode allows an external clock to be provided through the hybrid oscillator

7.2.2 RTC Oscillator

Both the internal XTAL and an external Oscillator can be used to generate a 32.768 kHz RTC clock. If an external Oscillator is used, ensure it meets the following specifications:

- Voltage operating range of 1.1-1.98V
- Accuracy of +/-20ppm
- Nominal current consumption of 125nA
- 350mS start-up time to reach +/-20ppm

Note: Refer to section [“28.2.1 Summary of SCSS Registers—0xB0800000”](#) for more details on how to configure the RTC

Note: Bypass mode allows an external clock to be provided through the RTC oscillator. This is done through the XTALI pin while XTALO must be grounded

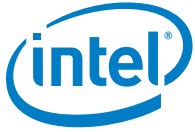
7.2.3 USB PLL

A PLL generates a 48 MHz USB clock from the system clock. The system clock must be running at 32MHz for the PLL to generate the 48MHz clock.

7.2.4 Root Clock Frequency Scaling

The Intel® Quark™ SE Microcontroller C1000 supports a single root clock with multiple supported root clock frequencies:

- 32MHz high accuracy crystal oscillator
Required for high accuracy applications.
- 4/8/16/32MHz silicon oscillator



A lower power operating mode used by applications that do not require a high frequency accuracy.

- 32,768Hz

An ultra-low power “doze” mode which allows quick wakeup times while enabling the powerdown of the hybrid oscillator.

7.2.5 Frequency Scaling

The Intel® Quark™ SE Microcontroller C1000 supports a wide range of frequency scaling options to optimize power:

- You can scale the root system clock frequency to 4/8/16/32MHz.
- You can scale the sensor subsystem peripheral clock independently at 2/4/8 divisions.

To apply a DFS setting, follow this procedure:

1. Apply the clock divider value **CCU_XXX_CLK_DIV**.
2. Apply the clock divider writing '0' **CCU_XXX_CLK_DIV_EN**.
3. Apply the clock divider writing '1' **CCU_XXX_CLK_DIV_EN**.

7.2.5.1 Peripheral DFS requirements

When using DFS, the firmware is responsible for adjusting any settings in peripherals/timers to account for the frequency change. For example, achieving a UART baud rate of 115200 requires a different baud rate divider, depending on the frequency.

7.2.5.2 Flash DFS requirements

When using DFS on the root fabric clock the flash wait states must be adjusted for both Flash instances.

If `sys_clock < 6.7MHz` (32,768Hz or 4MHz) the following settings should be used

1. Write '1' to `CLK_SLOW`
2. Write '0' to `PRE_EN`
3. Write '1' to `PRE_FLUSH` (note this must be done after `PRE_EN` is written to '0')
4. Write '0' to `PRE_FLUSH`
5. Write '0' to `READ_WAIT_STATE_L`

If `sys_clock > 6.7MHz` and `sys_clk < 20MHz` (16MHz) the following settings should be used

1. Write '0' to `CLK_SLOW`
2. Write '1' to `PRE_EN`



3. Write '0' to READ_WAIT_STATE_L

If sys_clock > 20MHz (32MHz) the following settings should be used

1. Write '0' to CLK_SLOW
2. Write '1' to PRE_EN
3. Write '1' to READ_WAIT_STATE_L

Note: The sequencing is important here. If you are changing sys_clk from a slow clock speed to a fast clock speed, you must update the Flash configuration with the configuration for the fast clock before the clock frequency is changed. When changing from a fast clock speed to a slow clock speed, you must change the clock frequency after the Flash configuration is updated with the configuration for the slow clock frequency.

7.2.6 Dynamic Clock Gating

The Intel® Quark™ SE Microcontroller C1000 supports a wide range of clock gating options. Firmware can gate each leaf clock dynamically.

To apply a dynamic clock gate (DCG), write '0' to the clock gate register CCU_XXX_PCLK_EN.

The Intel® Quark™ SE Microcontroller C1000 supports the following hardware clock gating options:

- UART low power autonomous hardware clock gating
- SPI low power autonomous hardware clock gating

7.2.6.1 UART Autonomous Clock Gating (ACG)

Both UART controllers support ACG mode (**CCU_UARTX_PCLK_EN_SW=0**). ACG is asserted when the following occurs:

- The transmit and receive pipeline is clear (no data in the RBR/THR or TX/RX FIFO).
- No activity has occurred on the SIN/SOUT lines.
- The modem input signals have not changed in more than one character time.

7.2.6.2 SPI Autonomous Clock Gating (ACG)

All SPI controllers support ACG mode (**CCU_SPI_XX_PCLK_EN_SW=0**). ACG occurs when the SSIENR register has been written to 0.

7.2.7 USB Clock Operation

For correct USB operation, the root fabric must run at 32MHz and off a high precision Crystal clock.



For USB operation, follow this procedure to ensure the required clock accuracy:

1. Ensure the main system divider is set to divide by 1 (**CCU_SYS_CLK_DIV = 0**).
1. Enable the crystal oscillator by writing '1' to **OSCO_EN_CRYSTAL**.
2. Set the hybrid oscillator to crystal mode by writing '1' to **OSCO_MODE_SEL**.
3. Enable the USB PLL by writing '1' to **USB_PLL_PDLD**.
4. Poll the USB PLL lock by reading **USB_PLL_LOCK** => 1.

When USB is not in use, power down the PLL (**USB_PLL_PDLD=0**) to conserve energy.

7.2.8 Doze Mode

The Intel® Quark™ SE Microcontroller C1000 supports a low power “Doze” mode. Doze mode allows the root system clock to run at a low frequency (32,768KHz). Doze mode offers a fast wakeup low power mode and is an alternative to the Sleep power gating state.

To enable doze mode, follow these steps:

1. Write '0' to **CCU_SYS_CLK_SEL** to switch the system clock to 32,768kHz.
2. Write '1' to **OSCO_PD** to power up the hybrid oscillator.

To disable doze mode, follow these steps:

1. Write '0' to **OSCO_PD** to power down the hybrid oscillator.
2. Write '1' to **CCU_SYS_CLK_SEL** to switch the system clock to hybrid oscillator.

7.2.9 System Clocking Modes

Table 28. System Clocking Modes

Modules	C0S0	C2S0	C0S2	C2S2	Doze	USB
System Clock	4/8/16/32 MHz	4/8/16/32 MHz	4/8/16/32 MHz	4/8/16/32 MHz	32KHz	32MHz
Processors State						
CPU Core	ON	OFF	ON	OFF	Optional	ON
SS	ON	ON	OFF	OFF	Optional	Optional
System Peripheral State						
Peripherals	DCG/DFS	DCG/DFS	DCG/DFS	DCG/DFS	DCG/DFS	DCG/DFS
System Clocks State						
RTC CLK	ON	ON	ON	ON	ON	ON
SYSTEM CLK	Either *	Either *	Either *	Either *	OFF	XO
USB PLL	OFF	OFF	OFF	OFF	OFF	ON
Mode Exit						
Exit	NA	HOST_INTR	SS_INTR	AON_WAKE	PROC	NA



Modules	C0S0	C2S0	C0S2	C2S2	Doze	USB
NOTE: * The system clock can run off 2 sources - a low power silicon oscillator (SI) or high accuracy Crystal Oscillator (XO)						



8 Sensor Subsystem

The Sensor Subsystem is an integrated hardware and software solution for control applications. The sensor subsystem is optimized to process data from analog and digital sensors, offloading the host processor and allowing low power processing of the sensor data.

The Sensor Subsystem contains a 32 bit processor. The Sensor Subsystem contains tightly coupled IP blocks which can be accessed with minimal latency. The IP blocks included in the Sensor Subsystem are as follows:

- 2x SPI Master Interfaces
- 2x I²C Master Interfaces
- ADC controller
- 8Kbyte 1 Way Instruction Cache (Icache)
- 8Kbyte Data Closely Coupled Memory (DCCM)
- 2x 8bit GPIO blocks
- Configuration register control block
- Configuration register observe block
- 2x Timers
- Interrupt Controller

The Sensor Subsystem core supports inclusion of user extension instructions. The Sensor Subsystem contains a range of Intel specific instructions for fractional arithmetic, complex number processing and Sin/Cos generation. The Sensor Subsystem also includes instructions to support floating point.

The Sensor Subsystem contains AHB interfaces to the system fabric and a JTAG debug interface.

The Sensor Subsystem reset vector points to the internal SRAM on the AHB fabric.

8.1 Signal Descriptions

Table 29. Sensor Subsystem Signals

Signal Name	Direction/ Type	Description
I2C 0 Master Interface		
IO_I2C_MST0_IIC_MST_SDA_IN	I	I2C 0 Serial input data
IO_I2C_MST0_IIC_MST_SCL_IN	I	I2C 0 Serial input clock



Signal Name	Direction/ Type	Description
I2C 1 Master Interface		
IO_I2C_MST1_IIC_MST_SDA_IN	I	I2C 1 Serial input data
IO_I2C_MST1_IIC_MST_SCL_IN	I	I2C 1 Serial input clock
SPI 0 Master Interface		
IO_SPI_MST0_SPI_MST_RXD	I	SPI Master 0 receive data.
IO_SPI_MST0_SPI_MST_TXD	O	SPI Master 0 transmit data.
IO_SPI_MST0_SPI_MST_OE_N	O	SPI Master 0 output enable
IO_SPI_MST0_SPI_MST_SS_N[3:0]	O	SPI Master 0 slave select
IO_SPI_MST0_SPI_MST_SCLK_OUT	O	SPI Master 0 clock
SPI 1 Master Interface		
IO_SPI_MST1_SPI_MST_RXD	I	SPI Master 1 receive data.
IO_SPI_MST1_SPI_MST_TXD	O	SPI Master 1 transmit data.
IO_SPI_MST1_SPI_MST_OE_N	O	SPI Master 1 output enable
IO_SPI_MST1_SPI_MST_SS_N[3:0]	O	SPI Master 1 slave select
IO_SPI_MST1_SPI_MST_SCLK_OUT	O	SPI Master 1 clock
GPIO Interface		
IO_GPIO0_GPIO_EXT_PORTA[15:0]	I	GPIO external input data – see

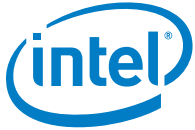
8.2 Features

The following sections describe each block in the sensor subsystem, along with the hard coded configuration for that block.

8.2.1 SPI Master

There are two instances of the SPI Master block in the Sensor subsystem. The features of the SPI Master block are as follows:

- Supports master mode only
- Supports 4 slave select outputs
- Supports SPI clock frequencies up to 16 MHz
 - SPI clock is a divided down version of the 32 MHz system clock
 - Divisor is any even value between 2 and 65534
- Supports configurable clock polarity
- Supports configurable clock phase
- Supports receive sample data delay



- Supports configurable frame size from 4 to 16 bits
- Supports 8 entry transmit FIFO
 - Optionally generates a transmit data required interrupt based on the transmit FIFO depth
 - Supports transmit FIFO status and FIFO error detection
- Supports 8 entry receive FIFO
 - Optionally generates a receive data available interrupt based on the receive FIFO depth
 - Supports receive FIFO status and FIFO error detection

For detailed operation and timing, see [“Chapter 18, SPI”](#).

8.2.2 I²C Master

There are two instances of the I²C Master block in the Sensor subsystem. The features of the I²C Master block are as follows:

- Supports master mode only
- Supports 2 interface speeds
 - Standard Mode (0-100kbps) – min system clock of 2.7MHz required
 - Fast Mode (100-400kbps) – min system clock of 12MHz required
- The I²C clock is a divided down version of the 32MHz system clock
 - The I²C clock high period is a configurable number of system clocks
 - The I²C clock low period is a configurable number of system clocks
- Supports spike suppression
- Supports 7 bit address format
- Supports 10 bit address format
- Supports clock stretching
- Supports 8 entry transmit FIFO
 - Optionally generates a transmit data required interrupt based on the transmit FIFO depth
 - Supports transmit FIFO status and FIFO error detection
- Supports 8 entry receive FIFO
 - Optionally generates a receive data available interrupt based on the receive FIFO depth
 - Supports receive FIFO status and FIFO error detection
- Generates interrupts on the following events:
 - Stop condition is detected on the I²C bus (dedicated stop_det interrupt)
 - Transfer is aborted due to master being unable to complete transmit request (shared error interrupt)
 - Transmit FIFO empty (shared error interrupt)



- Transmit FIFO overflow (shared error interrupt)
- Receive FIFO Full (shared error interrupt)
- Receive FIFO overflow(shared error interrupt)
- Receive FIFO underrun(shared error interrupt)
- Transmit data required – based on configurable threshold (tx_req interrupt)
- Receive data available – based on configurable threshold (rx_avail interrupt)

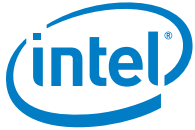
For detailed operation and timing, see [Chapter 15, I2C](#)”.

8.2.3 Sensor Subsystem Core

The core is configured as shown in the following table.

Table 30. Sensor Subsystem Core Configuration

Parameter	Configuration	Comments
Core: Address width	32	-
Core: PC width	32	-
Core: Loop counter width	16	-
Core: Halt on Reset	Yes	Core is taken out of halt state by CPU after the reset vector location has been configured into SRAM
Core: Endianess	Little	-
ISA: Code density option	Yes	Includes following instructions to support higher code density: ENTER_S, LEAVE_S, BI, BIH JLI_S
ISA: Bit Scan Option	Yes	Includes following instructions: NORM, NORMH, NORMW, FFS, FLS
ISA: Shift Option	3	Includes following instructions: ASR16, ASR8, LSR8, LSL8, ROL8, ROR8, ASL, LSR, ASR, ROR, ASL_S, LSR_S, ASR_S, ROR_S
ISA: Swap Option	Yes	Includes following instructions: SWAP, SWAPE, LSL16, LSR16
ISA: DIV/REM Option	radix2	Includes following instructions: DIV, DIVU, REM, REMU
ISA: Multiplier Option	wh3	Includes following instructions: MPYW/U, MPY/U, MPYH/U
ISA: Code protection option	Yes	Allows regions of memory to be protected from load/store accesses.
ISA: Stack checking option	Yes	Enables exception to be raised when there is a stack overflow or underflow
Interrupts/exceptions: Base vector	0xA8000000	
Register file: Implementation	Flip-flops	
Register file: size	32	32 registers, each register is 32 bits



Parameter	Configuration	Comments
Register file: Write ports	1	
Register banks	2	
Fast Interrupt Support	Yes	

The Sensor Subsystem core supports the low power sleep states shown in the following table.

Table 31. Low Power States

State	Core	Timers
Sleep mode 0	Disabled	Enabled
Sleep mode 1	Disabled	Disabled

All peripherals can be active while the Sensor Subsystem core is in sleep state. Note that the RTC will not wake the sensor subsystem if the interrupt is configured as edge Any level triggered interrupt can wake the core from the sleep state.

8.2.4 Extension Instructions

The Sensor Subsystem contains a range of Intel-specific instructions for fractional arithmetic, complex number processing, and Sin/Cos generation.

The Sensor Subsystem also includes instructions to support floating point. The following instructions are included:

- Floating Point Add (single and double precision)
- Floating Point Subtract (single and double precision)
- Floating Point Multiply (single and double precision)
- Floating point compare (single precision – 23 bit significand, 8 bit exponent)
- Integer to floating point (single precision – 23 bit significand, 8 bit exponent)
- Floating point to integer (single precision – 23 bit significand, 8 bit exponent)
- Floating point divide (single precision – 23 bit significand, 8 bit exponent)
- Floating point square root (single precision – 23 bit significand, 8 bit exponent)

8.2.5 Instruction Cache

An instruction cache is included in the Sensor Subsystem. After reset the Sensor Subsystem is held in the halt state while the reset vector location is populated in SRAM – once the reset vector table has been loaded the Sensor Subsystem can be taken out of the halt state via the run interface. The ICache is configured as follows:



- 8kbyte size
- 2 way associativity
- 16 byte cache line size
- Supports cache line locking
- Supports cache invalidate
- Supports cache line invalidate
- Supports cache line access via software

By default, instruction caching is disabled after reset – it must be enabled via configuration register.

In the event of a cache miss, the instruction is fetched via the instruction fetch interface as described in [Chapter 8.2.7, "Instruction Fetch Interface"](#). The Sensor Subsystem stalls while the instruction is fetched. In the event of a cache hit, the Sensor Subsystem core can perform back to back instruction execution, as the instruction is available to the core with zero wait states.

8.2.6 Data Closely Coupled Memory

A data closely coupled memory (DCCM) is included in the Sensor Subsystem. The DCCM is configured as follows:

- 8kbyte size
- Located at address 0x8000000 (in the Intel® Quark™ SE microcontroller address map)
- Accessible to the core with zero wait states
- Accessible to all Intel® Quark™ SE microcontroller fabric masters via a fabric slave interface

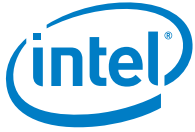
This allows DCCM to be accessed by both the Sensor Subsystem core and any other bus master on the fabric. In the event of contention between Sensor Subsystem core and any other fabric master, the fabric master takes priority.

Data fetches outside of DCCM shall appear on the external Fabric over the data fetch interface as described in [Chapter 8.2.8, "Data Fetch Interface"](#).

8.2.7 Instruction Fetch Interface

An instruction fetch interface is included in the Sensor Subsystem. The instruction fetch interface is a microcontroller fabric master interface that fetches instructions from external memory.

- AHB master interface for fetching instructions



- Full 16byte cache line is fetched at a time
- Burst size of 4 entries performed as an incrementing burst if Instruction caching is enabled
- Single dword accesses performed if instruction caching is disabled

8.2.8 Data Fetch Interface

A data fetch interface is included in the Sensor Subsystem. The data fetch interface is a microcontroller Fabric master interface that fetches instructions.

- AHB master interface for fetching instructions
- All transactions on the data fetch interface are single dword

8.2.9 Timer

Two timers are included in the Sensor Subsystem.

The expected uses for the timers are as follows:

1. U-kernel scheduler
2. Watchdog
3. Time stamping

If time stamping received samples with a granularity finer than 30us is required, one of these timers must be used. Otherwise, the timestamp received on the CREG slave interface is sufficient.

Both timers have optional interrupt generation and watchdog reset generation. The interrupt priority of timer 0 is set at 0 and the interrupt priority of timer 1 is set at 1. If a timer is enabled to have watchdog functionality, it will assert the reset_watchdog output from the Sensor Subsystem when the timer expires. This remains asserted until the sensor subsystem is reset. The timer is enabled to generate a watchdog reset via a software configuration register.

Both timers are 32bits, which with a 32 MHz clock gives a maximum time of 133 seconds before a timeout event.

There are two sleep modes in the Sensor Subsystem. One sleep mode disables the timers and another sleep mode allows the timers to remain active. In the sleep state where the timers remain active and a timer is enabled to generate an interrupt, the interrupt can be used to wake the processor from the sleep state.

When the Sensor Subsystem is in the halt state, the timers can be individually configured via software to increment or stall.



8.2.10 Interrupt Controller

The interrupt controller supports up to two priority levels for interrupts. The following parameters are programmable for each interrupt, with the exception of the timer interrupts which have a fixed priority as described in [Chapter 8.2.9, “Timer”](#):

- Priority level (two levels supported) – Priority 0 is the highest priority interrupt
- Pulse or level sensitivity

The sensor subsystem allows fast processing of priority 0 interrupts. It also has a second register bank which can be used to avoid saving and restoring context when processing a priority 0 interrupt. This removes the need to push context to SRAM when a priority 0 is received.

Note that by default, all interrupts are priority 0 (that is, fast interrupts). This means that by default, an interrupt will cause a register bank swap. This may require that an interrupt stack be created to process the interrupt. If there is no interrupt stack, then all interrupts should be changed to priority 1 interrupts. Also, if fast interrupts are used, the two register banks cannot be used for swapping between kernel and user mode.

Fifty-one interrupts are supported by the Sensor Subsystem. All Sensor Subsystem peripheral interrupts with the exception of the timer interrupts are made visible at the microcontroller level. The list of interrupts is as shown in the following table. If quick retrieval of data from the sensors is a priority, configure the data available interrupts from the SPI/I²C/ADC blocks to the highest priority.

Table 32. Interrupt Mapping

Interrupt Number	Interrupt Name
IRQ_16	TIMER 0
IRQ_17	TIMER 1
IRQ_18	ADC_ERR
IRQ_19	ADC_IRQ
IRQ_20	GPIO0_INTR
IRQ_21	GPIO1_INTR
IRQ_22	I2C 0 ERR
IRQ_23	I2C 0 RX_AVAIL
IRQ_24	I2C 0 TX_REQ
IRQ_25	I2C 0 STOP_DET I2C 1 ERR
IRQ_26	I2C 1 ERR
IRQ_27	I2C 1 RX_AVAIL
IRQ_28	I2C 1 TX_REQ
IRQ_29	I2C 1 STOP_DET



Interrupt Number	Interrupt Name
IRQ_30	SPI 0 ERR_INT
IRQ_31	SPI 0 RX_AVAIL
IRQ_32	SPI 0 TX_REQ
IRQ_33	SPI 1 ERR_INT
IRQ_34	SPI 1 RX_AVAIL
IRQ_35	SPI 1 TX_REQ
IRQ_[67:36]	Defined in top level interrupt routing section

8.2.11 CREG Master

The Sensor Subsystem supports a single 32 bit CREG Master. This allows the Sensor Subsystem to control external blocks via a register: the contents of the master control register are presented on the **IO_CREG_MST0_OP_CREG_CTRL** output from the Sensor Subsystem. The following table shows the usage for each bit in the CREG Master.

For more detailed information, see [Chapter 14.1.10, "CREG Register Detailed Description"](#).

Table 33. CREG Master Bit Assignment

Bit Number	Usage
[2:0]	ADC Power Mode - configures the ADC power mode – settings as follows: "100" – Normal Mode without calibration "011" – Normal Mode with calibration "010" – Standby "001" – Power Down "000" – Deep Power Down
[15:3]	ADC Delay – configures the amount of time the ADC Power Mode FSM stays in each state. Required to meet ADC timing specs.
[16]	ADC Calibration Operation Request
[19:17]	ADC Calibration Command – setting as follows: "100" – Load Calibration "011" – Start calibration "010" – Reset calibration
[26:20]	BVOSI – ADC calibration value to be loaded during a "load calibration" command
[27]	CLK_CTRL – SPI 0 clock gate – this is used to gate the clock to the SPI 0 Master
[28]	CLK_CTRL – SPI 1 clock gate – this is used to gate the clock to the SPI 1 Master
[29]	CLK_CTRL – I2C 0 clock gate – this is used to gate the clock to the I2C 0 Master
[30]	CLK_CTRL – I2C 1 clock gate – this is used to gate the clock to the I2C 1 Master
[31]	CLK_CTRL – ADC clock gate – this is used to gate the clock to the ADC Controller



8.2.12 CREG Slave 0/1

The Sensor Subsystem supports two 32 bit CREG Slave Registers. These are used for general purpose communication with devices outside the Sensor Subsystem. The value on the **IO_CREG_SLV0_IP_CREG_OBSR** and **IO_CREG_SLV1_IP_CREG_OBSR** inputs to the sensor subsystem can be checked on the CREG slave observation registers.

[Table 34](#) and [Table 35](#) show the usage for each bit in the CREG Slave Registers.

Table 34. CREG0 Slave bit assignment

Bit Number	Usage
[2:0]	ADC Power Mode – indicates the Current power mode of the ADC
[3]	ADC Power Mode FSM Status – this is '1' when the requested power state equals the current power state, and is '0' when the requested power state does not equal the current power state.
[4]	ADC Operation Ack – this is '1' when a requested operation has completed, it is cleared when software clears the "ADC Calibration Operation Request" bit of the CREG MASTER FSM.
[11:5]	BVOS – ADC calibration value
[31:12]	Unused

Table 35. CREG1 Slave Bit Assignment

Bit Number	Usage
[31:0]	Timestamp – this is connected to the Always on Counter

8.2.13 GPIO0/GPIO1 Blocks

The GPIO blocks in the sensor subsystem receive interrupts from the off chip sensors. The GPIO ports can be configured as inputs or outputs. When configured as inputs, the GPIO ports are interrupt capable with the following triggering options:

- Active high triggered interrupt
- Active low triggered interrupt
- Rising edge triggered interrupt
- Falling edge triggered interrupt

The interrupts are wake capable interrupts if the interrupts is a level triggered interrupt. Edge triggered interrupts cannot be used to wake the Sensor Subsystem from the sleep state.

The GPIO blocks provide debounce logic, which is required on external interrupts. External interrupts supported by the GPIO blocks are as shown in the following table.

The following table shows the list of inputs expected to be connected to the Sensor Subsystem via GPIO.

8.2.14 ADC Sequence Controller

The Sensor Subsystem contains an ADC controller. The ADC controller is responsible for gathering samples from the ADC block. It generates control to the ADC to acquire the samples and stores the received samples in a FIFO for retrieval by the Sensor Subsystem core. The features of the Sensor Subsystem ADC Controller are as follows:

- Generates an ADC clock by dividing down the system clock by a configurable divider
 - For even values of the divisor, ADC clock high time equals ADC clock low time
 - For odd values of the divisor, ADC clock high time is one clock longer than ADC clock low time
 - The divisor must be configured such that the 45:55 duty cycle on the ADC clock is not violated
 - Maximum supported clock frequency is 32MHz
 - Minimum supported clock frequency is 0.14MHz
- Implements a 32 entry sequencer to control capturing of the samples. Each entry in the sequencer contains the following:
 - Channel select – selects 1 of 19 channels to be sampled
 - Programmable delay to the start of the next conversion
- Sequencer can be run in single capture or repetitive run mode
- Supports a 32 entry receive FIFO for storing the received samples
 - Optionally generates a receive data available interrupt based on the receive FIFO depth
 - Supports receive FIFO status and FIFO error detection
 - In the event of a FIFO overflow, the oldest entries are discarded and are overwritten with the most recent samples
- Generates the following control to the ADC (additional configuration is supplied to the ADC from the CREG Master block):
 - ADC_MUX[4:0] – Channel select – generated by sequencer
 - ADC_DIFF – configures ADC for single ended mode. On Intel® Quark™ SE microcontroller the ADC doesn't support differential inputs.
 - ADC_SOC – Start of conversion – generated by sequencer
 - ADC_RES[1:0] – ADC resolution – configurable to be 12, 10, 8 or 6 bit
 - ADC_CLK – ADC clock
- Generates an error interrupt if the ADC controller takes a sample from the ADC before the ADC is ready – this occurs if the sequencer is misconfigured
- Supports rising edge sampling
- Supports parallel receive mode

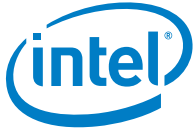


The following programming sequence shows how to configure the ADC controller to capture samples from the ADC:

1. Enable ADC_CLK. By default, after reset, ADC_CLK is internally disabled using a clock gate. ADC_CLK can be internally enabled by programming 1 in ***IO_ADC0_CTRL.CLK_ENA***.
2. Configure ADC_CLK speed via ***IO_ADC0_DIVSEQSTAT.CLK_RATIO***. Note that by default, after reset, ADC_CLK is disabled because ***IO_ADC0_DIVSEQSTAT.CLK_RATIO*** is reset to 0.
3. Enable the AD convertor by setting the ***IO_ADC0_CTRL.ADC_ENA*** register.
4. Make sure that the sequence pointer is 0x0. This is the case after reset or after setting ***IO_ADC0_CTRL.SEQ_PTR_RST***.
5. Fill the sequence table by writing the sequence entries to the ***IO_ADC0_SEQ*** register. After you write to ***IO_ADC0_SEQ*** the register clears itself to 0x0, and the sequence pointer auto-increments by two. To assure the sequencer starts with sequence entry 0, it is best to reset the sequence pointer by setting ***IO_ADC0_CTRL.SEQ_PTR_RST*** after the last sequence entry has been written.
6. Define the modes of operation for the FIFO, sequencer, sampler, and AD converter in the ***IO_ADC0_SET*** register.
7. Start the sequencer by setting ***IO_ADC0_CTRL.SEQ_START***
8. Poll on ***IO_ADC0_INTSTAT.DATA_A*** register or respond on IRQ.
9. THRESHOLD+1 samples are now available in the RX FIFO.
10. ***IO_ADC0_DIVSEQSTAT.SEQ_CUR*** shows the mux setting of the last sample data loaded in the RX FIFO. ***IO_ADC0_DIVSEQSTAT.SEQ_NXT*** register shows the mux setting for the next conversion.
11. Repeat for THRESHOLD+1 samples:
12. Set POP_RX in the ***IO_ADC0_CTRL*** register (maintain other bits if needed) to transfer one sample from RX FIFO into ***IO_ADC0_SAMPLE*** register.
13. Read the ***ADC_SAMPLE*** register.
14. Clear the ***DATA_A*** interrupt, by setting ***IO_ADC0_INTSTAT.CLR_DATA_A***.
15. In case of a single run, the sequencer automatically stops after executing entry ***IO_ADC0_SET.SEQ_ENTRIES***. ***IO_ADC0_CTRL.SEQ_START*** is cleared and the sequence pointer wraps around to 0x0.
16. In case of a repetitive run, the sequencer continuously executes sequences 0 to ***IO_ADC0_SET.SEQ_ENTRIES*** until stopped by clearing ***IO_ADC0_CTRL.START_SEQ***.

8.2.15 ADC Control

The ADC HIP requires specific sequences for calibrating the ADC and controlling power states of the ADC. The Intel® Quark™ SE Microcontroller C1000 provides hardware state machines for performing the calibration and power state control of the ADC. This simplifies the software and minimizes the number of instructions required for



calibration and power state control. Separate state machines are implemented for calibration and power state control.

8.2.15.1 ADC Power Control

The ADC Power Mode FSM sequences between the different power states of the ADC. A new state is requested via the Sensor Subsystem CREG master interface (**IO_CREG_MST0_CTRL.ADC_PWR_MODE**). The FSM takes care of the sequencing between the states. The **IO_CREG_SLV0_OBSR.ADC_PWR_MODE_STS** register bit can be polled to determine when the ADC has reached the requested power state. The following table shows the supported power states of the ADC and the state of the control signals into the ADC in each state.

Table 36. ADC Operating Modes

Operating Mode	Control Signal State				
	dislvl	enldo	Enadc	resetadc	bypasscal
Deep Power Down	3V3	0	0	0	0
Power Down	0	0	0	0	0
Standby	0	1	0	0	0
Normal w/calibration	0	1	1	Toggle	0
Normal wo/calibration	0	1	1	Toggle	1

Note: After waking from Deep Power Down, the ADC requires a dummy conversion to be performed. The ADC Power Mode FSM does not do the dummy conversion; software must perform the dummy conversion via the ADC Sequence Controller in the Sensor Subsystem. The dummy conversion is the same as a normal conversion but the sample returned by the ADC is invalid and must be discarded.

8.2.15.2 ADC Calibration Control

The ADC calibration FSM controls calibration of the ADC. The commands supported by the ADC calibration FSM are as follows:

- Reset calibration
- Start calibration
- Load calibration

The control for requesting a new state is contained in the **IO_CREG_MST0_CTRL** register. An interrupt is generated once the requested calibration command has completed. Alternatively, the **IO_CREG_SLV0_OBSR.ADC_CAL_ACK** register bit can be polled to determine when the ADC Calibration command has completed.

Once the requested command has completed, the **IO_CREG_MST0_CTRL.ADC_CAL_REQ** register bit must be cleared by software. This, in



turn, clears the **IO_CREG_SLV0_OBSR.ADC_CAL_ACK**. After a calibration command completes the calibration values are available in the **IO_CREG_SLV0_OBSR** register.

A start calibration or load calibration command is only required on exiting the Deep Power Down State. If the calibration coefficients are known from a previous calibration cycle then there is no need to re-run calibration; a load calibration command is sufficient.

8.3 Sensor Acquisition Use Case

8.3.1 Low Power Sensor Acquisition

Low power sensor acquisition is achieved via the following flow. The Sensor Subsystem is put into sleep state when possible to reduce power. The overhead with entry to an exit from sleep state is a low number of clock cycles.

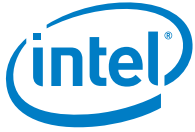
- Sensor Subsystem in Sleep State
- GPIO Interrupt – wake Sensor Subsystem
- I²C ISR
 - GPIO read to determine source of interrupt
- Create Gyro read command – write DATA_CMD Register in I2C
- Return Sensor Subsystem to sleep state
- RX FIFO not empty interrupt (dedicated interrupt line from I2C block) – wake Sensor Subsystem
- I²C control ISR
 - Read Rx FIFO
 - Sample write to DCCM
- Return Sensor Subsystem to sleep state

8.3.2 Time-Stamping

Time-stamping of samples received from sensors is useful to correlate when samples were received from different sensors. The sensor subsystem does not provide any hardware support for time-stamping data received from the sensors. The following analysis shows how samples can be time-stamped via software.

The procedure to timestamp a sample in software is as follows:

1. Sensor Subsystem in Sleep State
2. GPIO Interrupt – wake Sensor Subsystem
3. I²C ISR
 - CREG read of timestamp
 - GPIO read to determine source of interrupt



- Timestamp queue push
 - Read head
 - Read tail
 - Read size
 - ALU instruction - "head – tail"
 - ALU instruction – compare
 - ALU instruction check for overflow
- Timestamp write to DCCM
- 4. Create Gyro read command – write DATA_CMD Register in I²C
- 5. Return Sensor Subsystem to sleep state
- 6. RX FIFO not empty interrupt (dedicated interrupt line from I²C block) – wake Sensor Subsystem
- 7. I²C control ISR
 - Read Rx FIFO
 - Entry queue push
 - Read head
 - Read tail
 - Read size
 - ALU instruction - "head – tail"
 - ALU instruction – compare
 - ALU instruction check for overflow
 - Sample write to DCCM
- 8. Increment entry count
 - Read of DCCM
 - Increment count
 - Write of DCCM
- 9. Return Sensor Subsystem to sleep state

§



9 Pattern Matching Engine

Intel® Pattern Matching Engine (PME) consists of an efficient, highly parallelized hardware-based associative memory. The technology provides advanced pattern matching capabilities for real-time sensor analytics.

The PME is a parallel data indexed look-up table that enables constant recognition time, proportional to the number of features in the trained patterns. The PME uses a network of parallel arithmetic units (feature vectors) to compare new data vectors to data on which it has been trained. It identifies the closest match by performing either a nearest neighbor (k-NN) or radial basis function (RBF) search.

9.1 Features

The pattern matching engine provides the following features:

- Patterns stored in a 2-dimensional array containing up to 128 vectors, each with up to 128x8-bit features
- Up to 128 categories (15-bit each one)
- Two search algorithms: k-Nearest Neighbors (k-NN) and Radial Basis Function (RBF)
- Recognition time proportional to the number of features
- Distance calculation: two distance metrics, Lsup and L1
- Influence field or vicinity of vector for RBF search
- Classification status: category ID, uncertain, or unknown

9.2 Use

The PME interface provides two basic operations:

- Save a trained array
- Classify a new vector

All operations are executed through APB Read/Write commands to registers listed in [Table 37](#). Registers have a starting base address 0xB0600000h.

Table 37. PME Registers

Address	Register	Name	Notes
0x00	NCR	Context for trained array (default 0x0001)	RW



Address	Register	Name	Notes
0x04	COMP	Component Register (default 0x0000)	RW
0x08	LCOMP	Last Component (default 0x0000)	RW
0x0C	DIST	Read distance of classified vector to trained array; write component index	R
0x10	CAT	Category Register	RW
0x14	AIF	Active Influence Field for RBF search	R
0x2C	GCR	Global Context Register (default 0x1) and distance metric	RW [0:6] global context [7] distance metric 0=L1, 1=Lsub
0x30	RSTCHAIN	Reset Chain	W
0x34	NSR	Network Status Register	RW [0:1] reserved [2] uncertain (RBF mode) [3] ID status [4] status [5] k-NN classifier (default RBF)
0x3C	FORGET	Reset register count	W

9.2.1 Save a Trained Array

A trained array can be saved by switching the PME to save mode. All trained vectors must be written in the PME before any pattern matching search can take place. Vectors are written one by one, feature by feature.

```
// prepare array to be overwritten
Write FORGET, 0
Write NSR, 16
Write RSTCHAIN, 0

For (j=0; j<number_of_vectors; j++) {
    For (i = 0; i<vector_length, i++) {
        Write COMP, vector[i];    // save each vector component
    }

    // write associated information for j-th trained vector
    Write NCR, Context
    Write AIF, InfluenceField    // only relevant to RBF
    Write CAT, Category
}
Write NSR, 0    // ends array update
```



Each vector has an associated context, influence field (vicinity), and category. Influence fields are only relevant to RBF search.

9.2.2 Classify a New Vector

The PME compares new data vectors to the array of trained patterns. It broadcasts its components to the patterns in the feature space. The PME then calculates the similarities between the new data vector and all stored patterns. The selected distance metric and search algorithm influences this classification.

When k-NN search is selected, a search across the array will return the k-nearest vectors to the reference one. It is a point-wise comparison with the selected distance metric. RBF search finds whether a new data falls within the vicinity of trained patterns. Each trained vector should have an influence field for RBF search.

A new vector of features (see `new_vector` below) can be classified as follows:

```
For (i = 0; i < vector_length - 1, i++) {  
    Write COMP, new_vector[i]; // take each component  
}  
Write LCOMP, new_vector[vector_length - 1] // mark last component
```

In RBF, when new vectors are found within the vicinity of two or more trained patterns, the search returns the “uncertain” category. Conversely, if the new vector is found outside any trained patterns, the search returns the “unknown” category. For more information, see [Table 37. PME Registers](#).

The response of either search algorithm is calculated after writing the last component (LCOMP) marker. Classification results can be limited to its distance or category, for example:

```
Read DIST      // return distance to best match  
Read CAT       // return category
```

Successive calls to `Read DIST` and `Read CAT` will return the next element with closest distance (k-NN) to the trained patterns, until all vectors are explored or a distance 0xFFFF is read. All Read and Write register operations are 16-bit wide. Notice distance should be read before category.

9.3 Clocking

The PME can be clocked independently of the system clock. It supports synchronous divided clocks of 2/4/8/16/32. Running the PME APB clock at a divided frequency will decrease read and write performance. For more detail, see [Chapter 28.2.1, “Summary of SCSS Registers—0xB0800000”](#).

10 Power Management

This chapter provides information on the following power management topics:

- Intel® Quark™ SE Microcontroller Power Architecture
- Intel® Quark™ SE Microcontroller Power Management
- Intel® Quark™ SE Microcontroller Supported Power Management States

10.1 Power Architecture

The Intel® Quark™ SE Microcontroller C1000 has an integrated power management and power generation solution that provides both the internal – Host and Always On (AON) domain – and external platform supply rails (VCC_PLAT_1P8, VCC_PLAT_3P3).

[Figure 9. Power Delivery Strategy \(Using Internal Regulators\)](#) describes the power delivery strategy using the internal switching regulators to supply the platform rails 3.3V and 1.8V (VCC_PLAT_3P3 and VCC_PLAT_1P8) and the host rail/domain 1.8V (VCC_HOST_1P8). The figure details the available regulators and their interaction with the SoC power domains and main SoC functional blocks.

The Intel® Quark™ SE Microcontroller C1000 has an Over-Voltage Protection Module (OPM) that provides high-voltage protection. The OPM has four LDOs, of which three are configurable (on/off) and one generates 1.8V constantly (“LDO 0” - Always On). The LDOs provide the SoC internal low power voltage supply (up to 300uA).

Along with the OPM, the Intel® Quark™ SE Microcontroller C1000 has three configurable (on/off) switching regulators that can be used to supply the 3.3V (up to 150mA) and 1.8V (up to 100mA) platform and host rails (VCC_PLAT_1P8, VCC_PLAT_3P3 and VCC_HOST_1P8 respectively). If needed, “LDO_3p3”, “LDO_1p8”, and “LDO_Host” (in the OPM module shown in [Figure 9](#)) can be used to back up the switching regulators while using the internal regulators, as long as the current requirements for those rails are <300uA. The Intel® Quark™ SE Microcontroller C1000 manages the transition between “Switching Mode” and “LDO Mode”. The “LDO 0” is constantly ON (Always On domain) and must be used with an external 1.8V LDO to supply the Always On domain as shown in the figure.

To deal with the power state and voltage-level requirements, we require the following regulators:

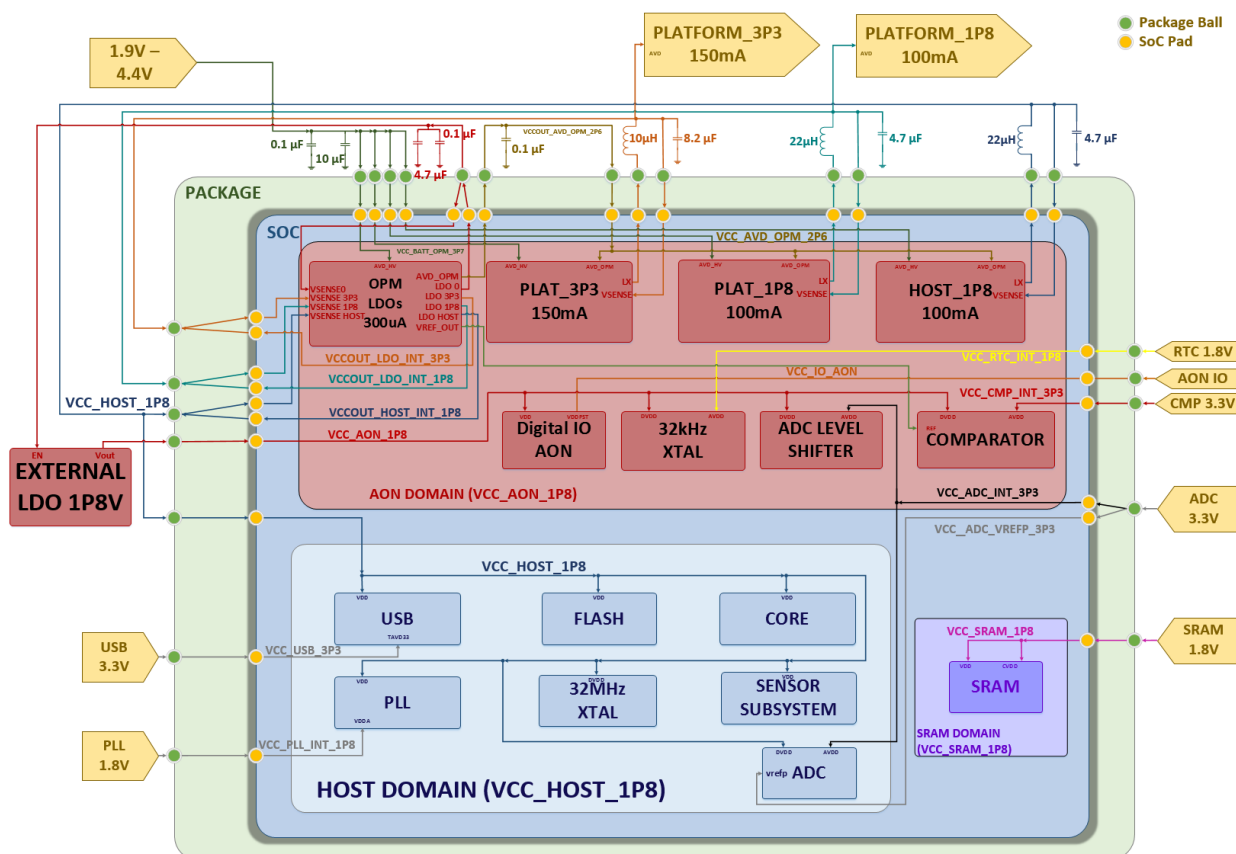
- 3.3V and 1.8V platform regulators (External or Internal VCC_PLAT_3P3 and VCC_PLAT_1P8). The internal regulator can be configured as Switching Regulator or LDO. The transition from Switching to LDO is done by SoC register. The platform regulators can be used to supply VCC_IO_AON, VCC_ADC, and VCC_CMP and VCC_PLL_1P8, VCC_RTC_1P8 and VCC_AON_1P8 through an external package ball.



- A 1.8V platform regulator (External LDO) generating 1.8V to power the Always On domain. You can use this to supply VCC_AON_1P8 and, optionally, VCC_IO_AON, VCC_ADC, VCC_PLL_1P8, and VCC_RTC_1P8.
- A 1.8V host regulator (External or Internal VCC_HOST_1P8). The internal regulator can be configured as Switching Regulator or LDO (the transition from Switching to LDO is done by SoC register) and it can be used to supply all HOST domain digital circuitry.
- An internal 2.6V is generated by the OPM (VCC_AVD_OPM_2P6) and it is used to provide an internal reference voltage for platform regulators.

Note: Special care must be taken in the event of a hardware power down of V_{SYS} followed by a power up sequence. Please ensure that The Intel® Quark™ SE C1000 Microcontroller reference voltage OPM_2P6 is discharged to ground before a power up cycle. Refer to The Intel® Quark™ SE Microcontroller C1000: Platform Design Guide (Document - 334715) for further details.

Figure 9. Power Delivery Strategy (Using Internal Regulators)



The following table shows the typical configuration of the internal regulators.

Table 38. Intel® Quark™ SE Internal Regulators

Regulator	Location	Blocks powered up by this regulator	Function
VCC_HOST_1P8	On-chip	VCC_HOST_1P8	This regulator provides the voltage for the entire HOST domain
VCC_PLAT_1P8	On-chip	VCC_IO_AON, VCC_ADC, VCC_PLL_1P8, VCC_RTC_1P8 and VCC_AON_1P8	This regulator provides the voltage platform 1.8V
VCC_PLAT_3P3	On-chip	VCC_ADC VCC_IO_AON VCC_CMP	This regulator provides the voltage platform 3.3V Note: VCC_CMP must be greater than 2V.

10.1.1 Power Domain Overview

The Intel® Quark™ SE Microcontroller C1000 has three power domains:

- HOST power domain
- Platforms power domain
- AON power domain

Note: Additionally, SRAM can be powered up from a different power rail to ensure retention in SoC Sleep Mode.

10.1.1.1 HOST Power Domain (VCC_HOST_1P8)

Host power domain requires a 1.8V that is supplied by VCC_HOST_1P8 (internal HOST regulator). This domain is only active in SoC Active state and is shut down in SoC Sleep state. For more information on system states, see [Chapter 10.3, “Supported Power Management States”](#).

10.1.1.2 Platforms Power Domain (VCC_PLAT_1P8/VCC_PLAT_3P3)

The SoC includes two optional internal switching regulators that can be used to supply the voltage platforms 1.8V and 3.3V (VCC_PLAT_1P8 and VCC_PLAT_3P3, respectively) that are necessary to supply peripherals such as PLL, RTC or Comparator. For more details, refer to [Table 38. Intel® Quark™ SE Internal Regulators](#).

10.1.1.3 AON Power Domain

The AON power domain requires an external power source to keep it always on. This external power source is required to ramp up within t_{ON_eSR} , as explained in [Chapter 11, “Power Up and Reset Sequence”](#). The on-chip LDO 1.8V can be used to enable the external power supply in order to meet t_{ON_eSR} .



VCC_IO_AON can be powered up independently from either 1.8V or 3.3V. If Analog Inputs AON (GPIO_AON) are expected to be greater than 1.8V, VCC_ADC should be powered from 3.3V.

10.1.1.4 Input Rail Connectivity

The following table shows Intel's recommendations on how to use the internal regulators to supply the different domain voltages.

Table 39. Input Rail Connectivity

Input Rail	Supply Rail			
	VCC_HOST_1P8 (2)	VCC_PLAT_1P8 (2)	VCC_PLAT_3P3 (2)	OTHER (PLATFORM)
VCC_AON_1P8		Yes (4)		
VCC_IO_AON		Yes	Yes	
VCC_USB_3P3				Yes
VCC_ADC		Yes (3)	Yes (3)	
VCC_CMP			Yes (3)	
VCC_PLL_1P8	Yes			
VCC_RTC_1P8		Yes (4)		
VCC_SRAM_1P8	Yes (1)	Yes (1)		

NOTES:

1. If SRAM Retention in Sleep is required, power VCC_SRAM_1P8 by VCC_PLAT_1P8. Otherwise, power VCC_SRAM_1P8 by VCC_HOST_1P8.
2. The VCC_HOST_1P8 rail is automatically powered down in the Sleep power state – the state of the VCC_PLAT_1P8 and VCC_PLAT_3P3 rails in Sleep are individually configurable by firmware.
3. The Analog Inputs pads (AIN[18:0]) are routed to both the ADC and the Comparators, thus appropriate care must be taken that the voltage levels of these inputs do not violate the requirements of either function (described later in this document). If Analog Inputs are expected to be greater than 1.8V then VCC_ADC should be powered from 3.3V.
4. The AON domain supply rails, VCC_AON_1P8 and VCC_RTC_1P8, are supplied from the VCC_PLAT_1P8 platform rail.

10.1.1.5 Internal Regulators: Inductor Selection

The internal regulators are optimized for an inductor value provided in the table below.

Thus, a 120 mA rated inductor should be enough for most applications when using, for example, the 100 mA configuration. For optimal efficiency, choose a low DC-resistance inductor. We recommend ceramic X7R/X5R dielectric type capacitors because of their temperature performance. Capacitors must be placed as close as possible to the pin they are connected to.



Table 40. Optimization of Internal Regulators for Inductor Values

Output current I _{max}	L	Output Capacitor (C _{OUT})	Input Capacitor (C _{IN})
150mA	10μH	8.2 μF	8.2 μF
100mA	22μH	4.7 μF	4.7 μF

NOTES:

1. Tolerances are L = ±30%, C_{OUT} = ±20%, C_{IN} = ±20%.
2. The provided C_{IN} values are recommended generic values. If you need to reduce parasitic serial inductance, set a complementary C_{IN} of 100nF.

10.1.1.6 Internal LDO: Output Capacitor Selection

The external decoupling capacitor for the regulator input supply, C_{OUT}, will range between min 2.2 and max 47μF. The typical value is 4.7 μF. It is assumed a manufacturing tolerance of +/–20%. It is recommended to add a 100μF ceramic capacitor in parallel with C_{OUT} in order to compensate for the lead inductance of C_{OUT}.

10.1.1.7 Battery Supply Connectivity

Table 41. Battery Supply Pins

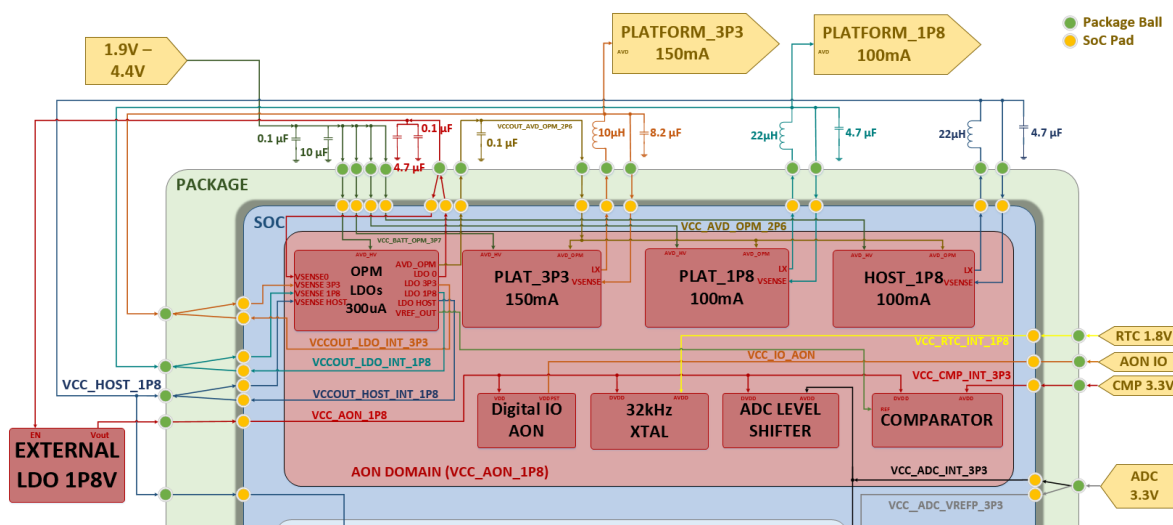
Pin Name	Power Domain	Description / Integration Details
VCC_BATT_OPM_3P7 VCC_BATT_PLAT_3P3_3P7 VCC_BATT_PLAT_1P8_3P7 VCC_BATT_HOST_1P8_3P7	VCC_BATT_3P7	Direct connection to the Battery Supply Rail - 1.9 to 4.4V

10.1.1.8 AON Rail Connectivity

Table 42. AON Rail Pins

Pin Name	Power Domain	Description / Integration Details
VCCOUT_AON_1P8	VCCOUT_AON_1P8	AON Rail Out – 1.8V Nominal Supply (1.62V to 1.98V). NOTE: This output rail is not looped back to supply any AON Domain.
VCC_AON_1P8	VCC_AON_1P8	AON Rail In – 1.8V Nominal Supply (1.62V to 1.98V) for AON Domain. NOTE: AON rail is not looped back to supply any AON Domain. It also requires an output capacitor.
VCC_IO_AON	VCC_IO_AON	AON Rail In – 1.8V Nominal Supply (1.62V to 3.63V). NOTE: To ensure the correct operation of the digital and analog IOs, VCC_IO_AON and VCC_ADC must be at the same voltage level (either 1.8V or 3.3V).

Figure 10. Typical Application Circuit



Note: PLL and USB are not shown in this figure.

10.1.1.9 USB IO Power Sequencing Requirements

The VCC_USB_3P3 rail into the USB 1.1 Transceiver has specific requirements. Some of these requirements relate to requirements from the USB Spec and others are tied to the behavior of the USB 1.1 Transceiver.

The requirements are as follows:

1. Do not power the VCC_USB_3P3 rail when there is no voltage present on the 5V USB VBUS line. Ideally, derive the VCC_USB_3P3 from the 5V VBUS.
2. Do not pull the 1.5kΩ pull-up resistor up to 3.3V when there is no voltage present on the USB VBUS line. On top of this, driving 3.3V onto VCC_USB_3P3 in the absence of a USB connection (VBUS present) will burn approximately 0.3mA on the External 1.5kΩ Pull-Up Resistor.
3. Do not power the VCC_USB_3P3 unless the VCC_HOST_1P8 rail is powered. Powering the VCC_USB_3P3 requires the platform to generate a wake event into the SoC to wake from Sleep when 5V is sensed on the USB VBUS line (VBUS sense). You can communicate this wake event through a Low Power Comparator or an AON GPIO.

You can also use a GPIO to control the enablement of the platform regulator and enforce the sequencing of VCC_USB_3P3 with respect to VCC_HOST_1P8.

10.1.1.10 ADC Supply Rail Connectivity

Table 43. ADC Supply Rail Pins

Pin Name	Power Domain	Description / Integration Details
VCC_ADC	VCC_ADC	Analog Supply Rail into ADC. Power this rail with either the 1P8 Platform Rail or the 3P3 Platform Rail, depending on Platform Requirements. Decouple the power supply according to Figure 9 . Ensure the 10nF capacitors (at least) are good quality ceramic and place them as close to the SoC as possible.
VSS_ADC_AGND	VSS_ADC_AGND	Analog Ground connection for ADC. (Separate pin from VSS to allow segregation of the Ground Plane of the PCB.)

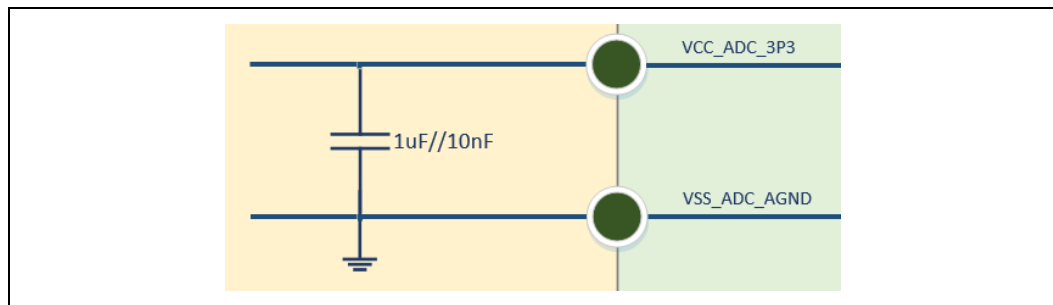
Table 44. ADC Supply Rail Requirements

Parameter	Unit	Min.	Typ.	Max.
VCC_ADC Voltage Range	V	1.62	1.8 / 3.3	3.6
VCC_ADC Decoupling Capacitances (in Parallel)	μF nF	-10% -10%	1 10	+10% +10%

Note: The ADC supports operation at either 1.8V or 3.3V. To have 3.3V scaling range, both VCC_IO and VCC_ADC must be 3.3V, otherwise the analog input pins will be clamped to IO voltage.

Note: To ensure the correct operation of the digital and analog IOs, VCC_IO_AON and VCC_ADC must be at the same voltage level (either 1.8V or 3.3V).

Figure 11. ADC Supply Rail External Component Connectivity





10.1.1.11 Comparator Supply Rail Connectivity

Table 45. Comparator Supply Rail Pins

Pin Name	Power Domain	Description / Integration Details
VCC_CMP	VCC_CMP	Analog Supply Rail into Comparators. Power this rail with the 3.3V Platform Rail. Note: If VCC_CMP is connected to PLAT_3P3V but VCC_AON_IO is 1P8V, the analog signal inputs to the comparator must be less than 1P8V otherwise they will be clamped to VCC_AON_IO.
VSS_AVSS_CMP	VSS_AVSS_CMP	Analog Ground connection for Comparators. (Separate pin from VSS to allow segregation of the Ground Plane of the PCB.)
COMP_AREF	COMP_AREF	External Comparator Reference Voltage. The default configuration uses the Internal 1.09V Reference Voltage.

10.2 Power Management Features

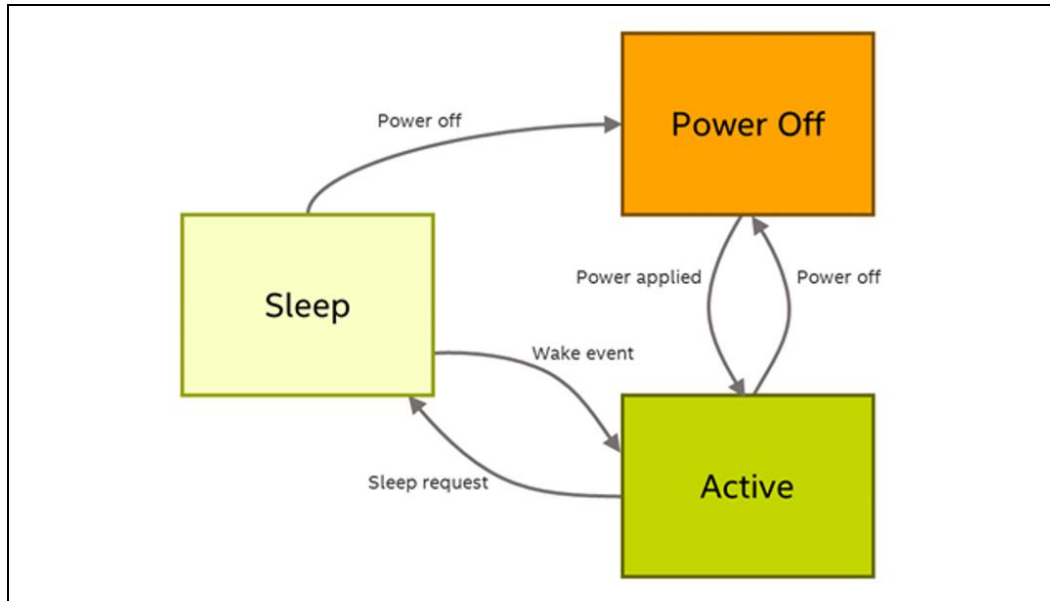
- Intel® Quark™ SE microcontroller System States support (Off, Sleep, Active)
- Host Processor States support (C0, C1, C2, C2 LP, LPSS)
- Sensor Subsystem States (SS0, SS1, SS2, LPSS)
- Low Power Sensing
- Peripheral Clock Gating

10.3 Supported Power Management States

This section describes the power management states supported by the Intel® Quark™ SE Microcontroller C1000.

10.3.1 Intel® Quark™ SE Microcontroller C1000 System State Definition

Figure 12. Intel® Quark™ SE Microcontroller C1000 System States



The Intel® Quark™ SE Microcontroller C1000 supports a number of power management system states that determine the behavior of the system clocks and the on-die voltage regulators.

10.3.2 Intel® Quark™ SE Microcontroller C1000 System States

The system clocks consist of the main core clock (up to 32 MHz) and the RTC clock (32.768 kHz).

The on-die voltage regulators provide the following voltage rails:

- Core Voltage Rail (1.8V)
- Always On (AON) Voltage Rail (1.8V)
- Platform 1P8 Voltage Rail (1.8V)
- Platform 3P3 Voltage Rail (3.3V)

10.3.2.1 Active State

The Active state is the normal operating state of the Intel® Quark™ SE Microcontroller C1000. In the Active state, the core clock and RTC clock are running and the Core and AON voltage rails are enabled. You can optionally enable the Platform 1P8 and 3P3 voltage rails. If the Platform 1P8 rail is used to supply the AON domain, this rail then is required to be ON for AON operation.



In the Active state, the Host processor can transition into and out of various C-states and the Sensor Subsystem can transition into and out of various sensing states. You can disable or clock gate Intel® Quark™ SE microcontroller peripherals for additional power savings.

10.3.2.2 Sleep State

Sleep is a suspend state in which the host voltage rail and core clock are turned off and the Always On voltage rail remains powered. You can individually configure the platform 3P3 and 1P8 voltage rails to be turned on or off in this state. You can also configure the platform rails in linear mode to reduce the power consumption. If the 3P3 or 1P8 rails are used to power the AON domain then it must remain on.

You can choose to retain the contents of SRAM during the Sleep state. If the SRAM contents do not need to be retained during the Sleep state, you can connect the SRAM voltage supply rail (VCC_SRAM_1P8) to the same supply as the host domain. However, if the SRAM contents must be preserved, you must connect VCC_SRAM_1P8 to an AON supply.

The Intel® Quark™ SE Microcontroller C1000 supports the following wake events:

- Low Power comparator Interrupt
- AON GPIO Interrupt
- AON Timer Interrupt
- RTC Interrupt

10.3.2.3 Off State

In the Off state, all voltage rails are disabled and no clocks run. The Intel® Quark™ SE Microcontroller C1000 enters the Off state if the power supply is less than 1.9v.

When power is applied, the Intel® Quark™ SE Microcontroller C1000 exits the Off state and transitions to Active.

Table 46. General Power States for System

State	Description
Active	Host domain is on. Always On domain is on. System Clock is on. RTC Clock is on
Sleep	Host domain is off. Always On domain is on. System Clock is off. RTC Clock is on
Off	Host domain is off. Always On domain is off. System Clock is off. RTC Clock is off

The following table shows the transition rules among the various states. Note that transitions among the various states may appear to temporarily transition through intermediate states. These intermediate transitions and states are not listed in the table.



Table 47. State Transition Rules

Present State	Transition Trigger	Next State
Active	Host SW requests Sleep Entry by writing to PM1C.SLPEN register field	Sleep
	Power Removed	Off
Sleep	Wake Event	Active
	Power Removed	Off
Off	Power Applied	Active

A SoC Wake event is a transition from SoC LPSS or SoC Sleep to a state where one CPU is in active state. A CPU Wake event is a transition from a CPU low power state to a CPU active state.

Table 48. Wake Events

SoC Wake Events	CPU Wake Events
Low Power comparator Interrupt	All interrupts from peripherals or internal CPU interrupt
AON GPIO Interrupt	
AON Timer Interrupt	
RTC Interrupt	

10.4 Processor Core Power States

Table 49. Processor Core Power States

State	Name	Description
C0	Normal State	Processor executing instructions.
C1	Halt State	CPU is not executing instructions. Internal Processor Clock gated.
C2	Stop Grant State	CPU is not executing instructions. Internal Processor Clock gated. The only difference with C1 is the way the SoC enters in the power state.
C2 LP	Low Power Stop Grant State	CPU is not executing instructions. Processor Complex Clock Gated (LAPIC gated)
LPSS	Low Power Sensing Standby State	Combination Processor Core/Sensor Subsystem State Intel® Quark™ SE microcontroller System Clock is gated

There are two classes of interrupt source for the Host Processor – Host Interrupts and Local APIC Interrupts. Host Interrupts can come from any event that can be routed to the Host Processor via the Host Processor Interrupt Routing Mask registers. The Host Processor Interrupt Routing Mask registers steer the enabled Host events to the I/O APIC. Local APIC Interrupts are generated in response to MSIs received from the I/O APIC or from local interrupts within the Local APIC (for example, the LVT Timer).



The delivery of Local APIC interrupts to the Host Processor require the clock to Processor Complex to be running. As a result, Local APIC interrupts cannot be delivered in C2 LP.

For details on Wake Events and the Low Power Sensing state, see [Chapter 10.6, “Low Power Sensing Standby State”](#).

Table 50. Processor Core Power State Transition Rules

Present State	Transition Trigger	Next State
C0	Host SW executes HLT instruction	C1
	Host SW reads P_LVL2 register and CCU_LP_CLK_CTL.CCU_C2_LP_EN set to 0b	C2
	Host SW reads P_LVL2 register and CCU_LP_CLK_CTL.CCU_C2_LP_EN set to 1b	C2 LP
C1	Host Interrupt Local APIC Interrupt	C0
C2	Host Interrupt Local APIC Interrupt	C0
	Sensor Subsystem enters SS2 with: CCU_LP_CLK_CTL.CCU_SS_LPS_EN set to 1b	LPSS
C2 LP	Host Interrupt Local APIC Interrupts are not compatible with C2 LP	C0
	Sensor Subsystem enters SS2 or is already in SS2 with CCU_LP_CLK_CTL.CCU_SS_LPS_EN set to 1b. (Refer to Table 51. Sensor Subsystem Power State Transition Rules)	LPSS
LPSS	Wake Event routed to Host Processor	C0
	Wake Event routed to Sensor Subsystem with CCU_LP_CLK_CTL.CCU_C2_LP_EN set to 0b	C2
	Wake Event routed to Sensor Subsystem with CCU_LP_CLK_CTL.CCU_C2_LP_EN set to 1b	C2 LP

10.5 Sensor Subsystem Power States

Table 51. Sensor Subsystem Power States

State	Name	Description
SS0	Sensing Active State	Sensor Subsystem running
SS1	Sensing Wait State	SS Core Clock Gated. See Table 53. Sensor Subsystem Internal Clocks during Sleep Mode .
SS2	Sensing Standby State	SS Complex Clock Gated SS Peripheral Clock Gated
LPSS	Low Power Sensing Standby State	Combination Processor Core/Sensor Subsystem State Intel® Quark™ SE microcontroller System Clock is gated



There are two classes of interrupt source for the Sensor Subsystem – SS Interrupts and SS Peripheral Interrupts. SS Interrupts can come from any event that can be routed to the Sensor Subsystem via the Sensor Subsystem Interrupt Routing Mask registers. SS Peripheral Interrupts come from events within the Sensor Subsystem that are not observable by the Host Processor.

Table 52. Sensor Subsystem Power State Transition Rules

Present State	Transition Trigger	Next State
SS0	Sensor SW executes SLEEP instruction with Sleep Operand set to 000b, 001b or 010b	SS1
	Sensor Subsystem SPI, I2C and ADC Clocks are gated. IO_CREG_MST0_CTRL (Bits 27 to 31). Refer to Chapter 8.2.11, “CREG Master” and Sensor Subsystem executes SLEEP instruction with Sleep Operand set to 011b, 100b, 101b, 110b or 111b.	SS2
SS1	SS Interrupt SS Peripheral Interrupt	SS0
SS2	SS Interrupt	SS0
	Processor Core enters C2/C2 LP or is already in C2/C2 LP with CCU_LP_CLK_CTL.CCU_SS_LPS_EN set to 1b.	LPSS
LPSS	Wake Event routed to Host Processor	SS2
	Wake Event routed to Sensor Subsystem	SS0

The clock gating of the SS Peripherals is controlled by the SS CREG IO_CREG_MST0_CTRL. Bits in this register are set to 1b to clock gate SPI, I2C and ADC. The relevant registers are IO_CREG_MST0_CTRL Bits 27 to 31. Refer to [Chapter 8.2.11, “CREG Master”](#). **This is required to enter into LPSS.**

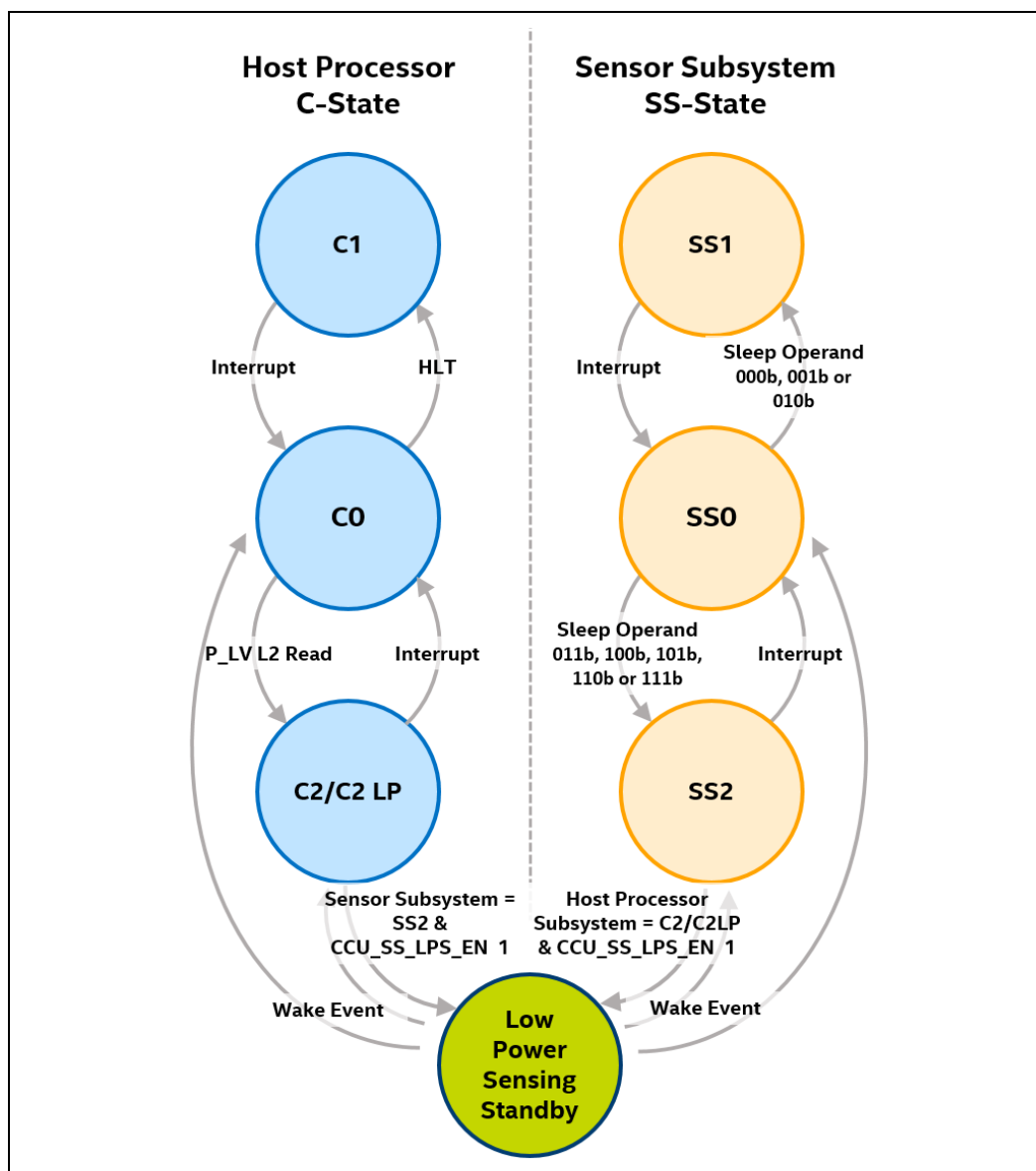
For details on Wake Events and the Low Power Sensing state, see [Chapter 10.6, “Low Power Sensing Standby State”](#).

Table 53. Sensor Subsystem Internal Clocks during Sleep Mode

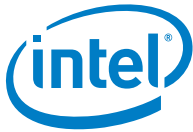
Sleep Operand	SS Core Clock	SS Internal Timers	SS Real Time Clock
000b	Clock Gated	Enabled	Enabled
001b	Clock Gated	Clock Gated	Enabled
010b	Clock Gated	Enabled	Clock Gated
011b	Clock Gated	Clock Gated	Clock Gated
100b	Clock Gated	Clock Gated	Clock Gated
101b	Clock Gated	Clock Gated	Clock Gated
110b	Clock Gated	Clock Gated	Clock Gated
111b	Clock Gated	Clock Gated	Clock Gated

10.6 Low Power Sensing Standby State

Figure 13. Low Power Sensing Standby Entry



The Low Power Sensing Standby state is the lowest power state possible while the Intel® Quark™ SE Microcontroller C1000 is in the Active state. To enter the Low Power Sensing State, the Host Processor must be in the C2 or C2 LP state and the Sensor Subsystem must be in the SS2 state. If you enabled Low Power Sensing (by setting CCU_LP_CLK_CTL.CCU_SS_LPS_EN to 1b) and both the Host Processor and Sensor Subsystem enter the required states, power management logic gates the System Clock and the Intel® Quark™ SE Microcontroller C1000 enters the Low Power Sensing state.



Please note that if either the host processor or the sensor subsystem wakes up from LPSS, to enter LPSS again the CCU_LP_CLK_CTL.CCU_SS_LPS_EN bit should be toggled before going to C2/C2LP.

The following clock gates **must** also be set to get to the LPSS state:

SS SPI Master 0	IO_CREG_MST0_CTRL.CTRL[27]
SS SPI Master 1	IO_CREG_MST0_CTRL.CTRL[28]
SS I2C Master 0	IO_CREG_MST0_CTRL.CTRL[29]
SS I2C Master 1	IO_CREG_MST0_CTRL.CTRL[30]
SS ADC	IO_CREG_MST0_CTRL.CTRL[31]

Refer to [Chapter 8.2.11, “CREG Master”](#).

In the Low Power Sensing State, only the RTC clock runs. The gating of the System Clock gates all other clocks in the Host domain of the Intel® Quark™ SE Microcontroller C1000. The clocks in the Always On domay stay running.

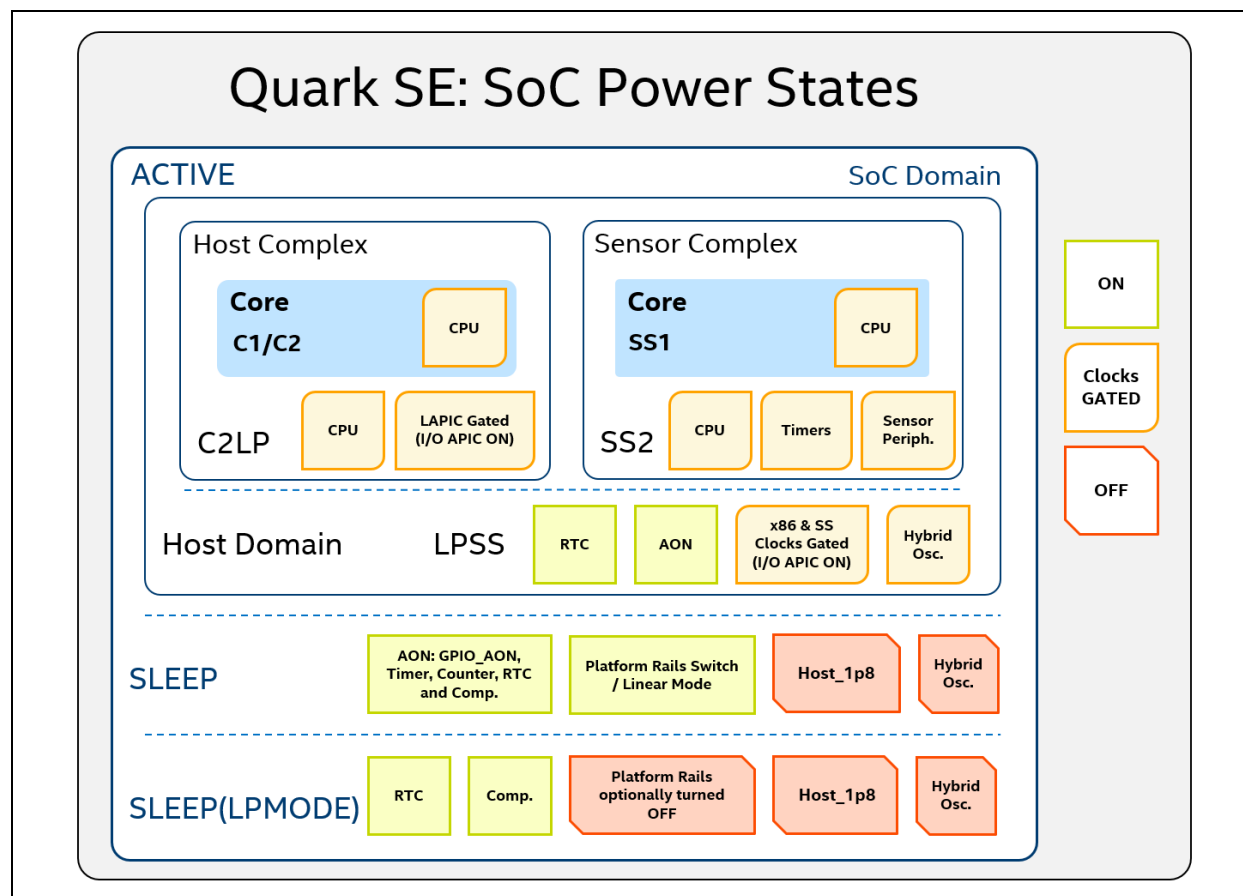
The Intel® Quark™ SE Microcontroller C1000 remains in the Low Power Sensing state until a Wake Event occurs. When a Wake Event occurs, the System Clock restarts and the interrupt that triggered the Wake Event is routed to either the Host Processor or the Sensor Subsystem. The Host Processor Interrupt Routing Mask registers and the Sensor Subsystem Interrupt Routing Mask registers determine the destination of the Wake Event.

Note: Do not enable the Low Power Sensing state while USB is active.

Note: Software must ensure that there are no DMA transactions in flight before enabling Low Power Sensing state.



Figure 14. SoC Power States



11 Power Up and Reset Sequence

This chapter provides information on the following topics:

- Power Up Sequences
- Power Down Sequences
- Reset Behavior
- Internal Regulator Inductor Selection

11.1 Power Up Sequences

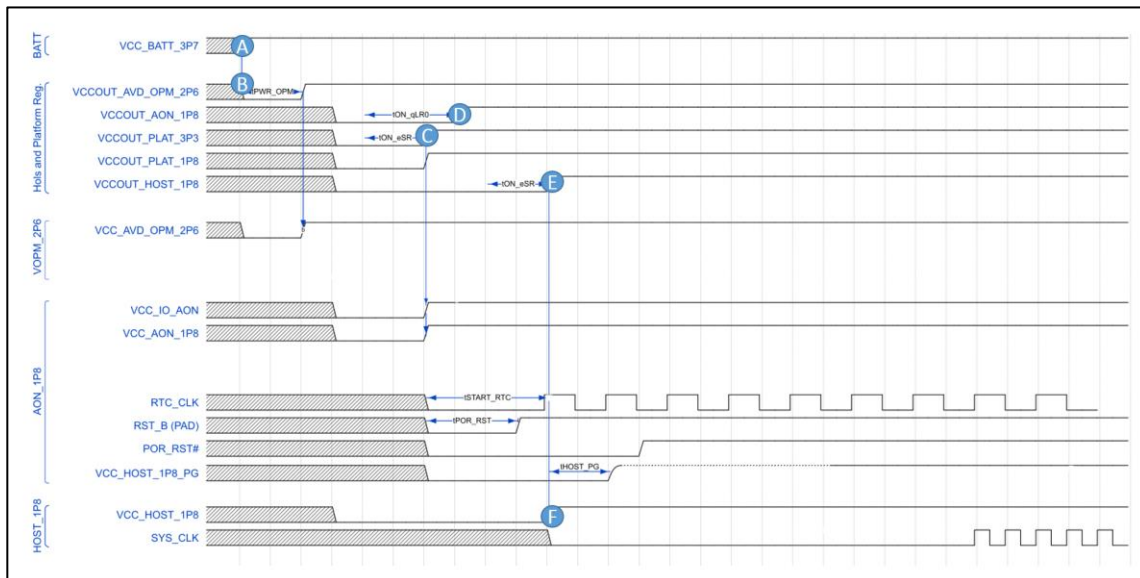
11.1.1 Off to Active

When an external battery or other power source applies VCC_BATT_V3P7, the SoC powers up automatically. There are two possible power up sequences: one sequence uses internal regulators only, and the other allows the use of external regulators. The value of the hardware strap PLT_REG_EN governs the selection of power up sequence.

11.1.1.1 Power Up Sequence using Internal Regulators

The following power up sequence occurs when VCC_BATT_V3P7 is applied and PLT_REG_EN is tied to VSS. This sequence is illustrated below.

Figure 15. Power Up Sequence Using Internal Regulators





- A.** Main power is applied.
- When main power rises above 1.9V, OPM iLR starts ramping VCCOUT_AVD_OPM_2P6.

Note: Special care must be taken in the event of a hardware power down of V_{SYS} followed by a power up sequence. Please ensure that The Intel® Quark™ SE C1000 Microcontroller reference voltage OPM_2P6 is discharged to ground before a power up cycle. Refer to The Intel® Quark™ SE Microcontroller C1000: Platform Design Guide (Document - 334715) for further details.

- B.** VCCOUT_AVD_OPM_2P6 crosses OPMBOR_{threshold}.

This places ACU into Reset State. ACU then initializes LDOs and Regulators based on PLT_REG_EN (REG_PLAT) value.

- PLT_REG_EN is tied to VSS.
 - VCCOUT_AVD_OPM_2P6 crosses OPMPON_{threshold} and PON_VOPM is asserted.
- C.** VCCOUT_PLAT_3P3 and VCCOUT_PLAT_1P8 ramp to 3.3V and 1.8V respectively over t_{ON_eSR} .

Note: When EN_ACU[0] is asserted, VCCOUT_AON_1P8 ramps to 1.8V over t_{ON_qLR} .

- VCCOUT_AON_1P8 is not looped back on platform to supply any SoC voltage rails.

- D.** VCCOUT_AON_1P8 crosses REGPON_{threshold} and PON_QLR0 is asserted.

- E.** When EN_ACU[6] is asserted, VCCOUT_PLAT_1P8 ramps to 1.8V over t_{ON_eSR} .

- F.** VCCOUT_HOST_1P8 crosses REGPON_{threshold}. This completes the start-up sequence performed by the ACU for PLT_REG_EN = 0.

Power On is complete. PMU transitions to ACTIVE state.

Note: When VCC_AON_1P8 has ramped, RST_B is released for t_{POR_RST} .

- RST_B level depends on the chosen VCC_IO_AON voltage level.

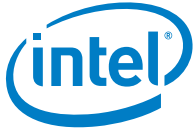
Note: After t_{START_RTC} , RTC oscillator starts generating a 32.768 kHz clock.

- The RTC oscillator is enabled once VCC_AON_1P8 is supplied and POR_RST# is asserted.
- This clock source is used as the SoC System clock during power on.

Note: PMU releases COLD_RST#, which takes the AON domain out of reset.

Note: VCC_HOST_1P8_PG must be asserted at least t_{HOST_PG} after VCC_HOST_1P8 has ramped.

PMU releases Host Isolation signals to disable isolation between AON and Host domains.



Note: PMU releases Hybrid Oscillator Power Down signal to enable the generation of a 4 MHz clock via the silicon oscillator.

Note: When released from Power Down, the silicon oscillator starts generating a 4 MHz clock at $t_{\text{START\_SI\_OSC}}$.

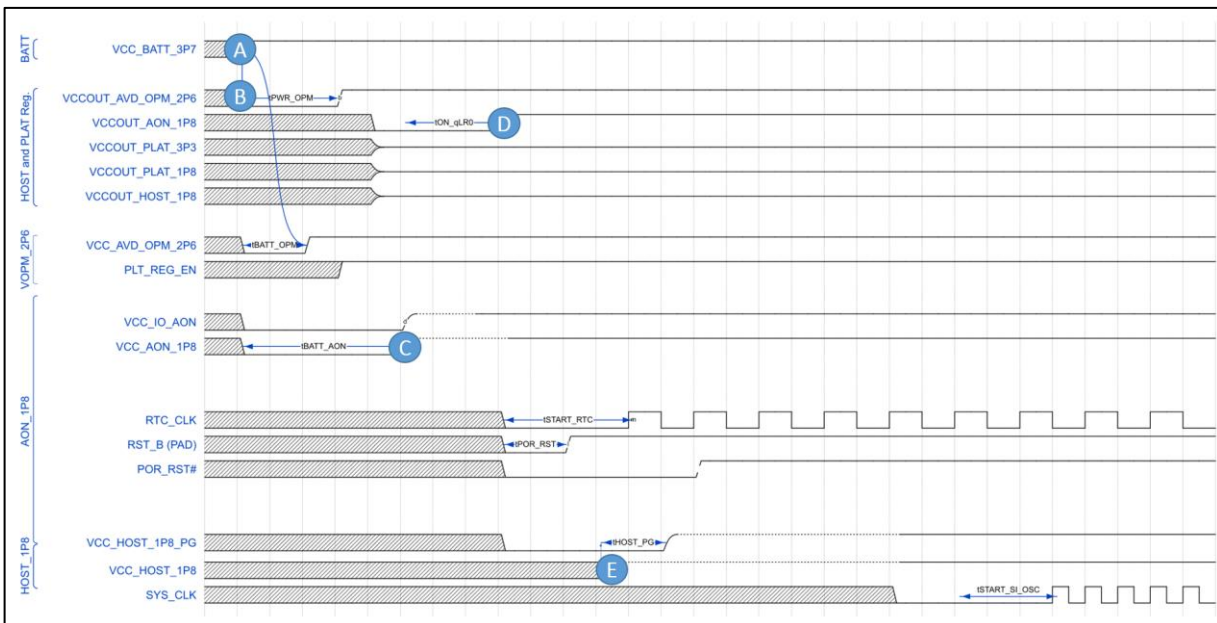
Note: PMU Host VR FSM switches System Clock Mux from RTC oscillator (32.768 kHz) to silicon oscillator (4MHz) Hybrid Oscillator Power Down signal, to enable the generation of a 4 MHz clock through the silicon oscillator.

- The silicon oscillator clock source is now used as the SoC System clock.

11.1.1.2 Power Up Sequence Using External Regulators

The following power up sequence occurs when VCC_BATT_V3P7 is applied and PLT_REG_EN is tied to VCC_AVD_OPM_V2P6. This sequence is illustrated in [Figure 16. Power Up Sequence Using External Regulators](#) (the letters of the sequence below correspond to those in the figure).

Figure 16. Power Up Sequence Using External Regulators



A. Main power is applied. We recommend to use the internal OPM regulator to supply the OPM rail.

- When main power rises above 1.9V, OPM iLR starts ramping VCCOUT_AVD_OPM_2P6.

Note: Special care must be taken in the event of a hardware power down of VSYS followed by a power up sequence. Please ensure that The Intel® Quark™ SE C1000 Microcontroller reference voltage OPM_2P6 is discharged to ground before a power up cycle. Refer to The Intel® Quark™ SE Microcontroller C1000: Platform Design Guide (Document -



334715) for further details.

- B. Special care must be taken in the event of a hardware power down of V_{SYS} followed by a power up sequence. Please ensure that The Intel® Quark™ SE C1000 Microcontroller reference voltage OPM_2P6 is discharged to ground before a power up cycle. Refer to The Intel® Quark™ SE Microcontroller C1000: Platform Design Guide (Document - 334715) for further details.
- C. VCCOUT_AVD_OPM_2P6 crosses $OPMBOR_{threshold}$ and ACU enables LDO_0. Refer to ["Figure 10. Typical Application Circuit"](#) for further details on LDO_0.
- D. An External Regulator ramps and supplies VCC_IO_AON at either 3.3V or 1.8V. An External Regulator ramps and supplies VCC_AON_1P8.
- E. VCCOUT_AON_1P8 crosses $REGPON_{threshold}$ and PON_QLR0 is asserted.
 - **This completes the start-up sequence performed by the ACU for $PLT\_REG\_EN = 1$.**
- F. When VCC_AON_1P8 is supplied and in regulation, and RST_B has been asserted, an external regulator can ramp and supply VCC_HOST_1P8. If you allow VCC_AON_1P8 to be supplied and RST_B to be applied before ramping VCC_HOST_1P8, you can reset all AON flops to valid values before supplying power to the Host domain. You can also enable isolation between AON and Host domains before supplying power to the Host domain.

Note: When VCC_AON_1P8 has ramped, RST_B is released for t_{POR_RST} . The RST_B level depends on the chosen VCC_IO_AON voltage.

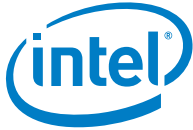
Note: RTC oscillator starts generating a 32.768 kHz clock. The RTC oscillator is enabled once VCC_AON_1P8 is supplied and POR_RST# is asserted. This clock source is used as the SoC System clock during power on.

Note: The internal, reset synchronized POR_RST# is released, which takes the PMU out of reset. PMU Host domain FSM waits for the following conditions to be met before beginning the sequence to release the Host domain from reset: VCC_HOST_1P8_PG pad must be asserted to indicate that the External Regulator supplying VCC_HOST_1P8 is in regulation at least t_{HOST_PG} after VCC_HOST_1P8 has ramped.

Note: This is also the opportunity to use a top-level pin to stall the power on sequence and break in with JTAG to observe, override, and re-program internal signals within the SoC.

Note: PMU releases Hybrid Oscillator Power Down signal to enable the generation of a 4 MHz clock through the silicon oscillator. The silicon oscillator starts generating a 4 MHz clock through the silicon oscillator, the PMU Host switches System Clock Mux from RTC oscillator (32.768 kHz) to silicon oscillator (4MHz) Hybrid Oscillator Power Down signal. The silicon oscillator clock source is now used as the SoC System clock.

Note: Once the Power on is complete, PMU transitions to ACTIVE state.



11.1.1.2.1 Supplying VCC_BATT_3P7 and VCC_AON_1P8 from External Regulators

This section details the requirements for supplying VCC_BATT_3P7 and VCC_AON_1P8 from external regulators.

Sources supplying VCC_BATT_3P7 and VCC_AVD_OPM_2P6 must meet the following requirements:

- When VCC_BATT_3P7 < 2.6V, VCC_AVD_OPM_2P6 must be equal to VCC_BATT_3P7
- When VCC_BATT_3P7 > 2.6V, VCC_AVD_OPM_2P6 must be equal to 2.6V

Note: Special care must be taken in the event of a hardware power down of V_{SYS} followed by a power up sequence. Please ensure that The Intel® Quark™ SE C1000 Microcontroller reference voltage OPM_2P6 is discharged to ground before a power up cycle. Refer to The Intel® Quark™ SE Microcontroller C1000: Platform Design Guide (Document - 334715) for further details.

- Delays between VCC_BATT_3P7 and VCC_AVD_OPM_2P6:
 - Minimum: 0us
 - Maximum: 100us
 - t_{BATT_OPM} is the time between VCC_BATT_3P7 reaching 90% and VCC_AVD_OPM_2P6 reaching 90%
 - $0 \leq t_{BATT\_OPM} < 100us$
- VCC_AVD_OPM_2P6 must reach 90% before PON_AVD_OPM rises to 1.

Sources supplying VCC_BATT_3P7 and VCC_AON_1P8 must meet the following requirements:

- VCC_AON_1P8 must be in the range 1.62-1.98V.

Note: An external capacitor, C_OPM, must be connected to VCCOUT_AVD_OPM_2P6 even when an external regulator is used to supply VCC_AVD_OPM_2P6. Failure to provide C_OPM will result in unreliable operation. For more information about C_OPM, see the SoC Integration guide.

Note: An external capacitor, C_AON, must be connected to VCCOUT_AON_1P8 even when qLRO is not used to supply any SoC voltage rails. Failure to provide C_AON will result in unreliable operation. For more information about C_AON, see the SoC Integration guide.

11.1.1.3 SRAM Power Up Sequence

Power is supplied to the 80kB on-die SRAM through VCC_SRAM_1P8. This dedicated supply allows you to place the SRAM in either the AON domain or the Host domain. If you place the SRAM in the AON domain, the contents of SRAM are retained when the SoC enters the Sleep state and preserved when the SoC re-enters the Active state. If you place the SRAM in the Host domain, the contents of SRAM are lost when the SoC enters the Sleep state and the SRAM will be empty when the SoC re-enters the Active state. The SRAM power domain location is dependent on the target use case.



If you place the SRAM in the AON domain, you must supply VCC_SRAM_1P8 with the same timing as VCC_AON_1P8.

If you place the SRAM in the Host domain, you must supply VCC_SRAM_1P8 with the same timing as VCC_HOST_1P8.

Note: If you supply VCC_SRAM_1P8 after VCC_HOST_1P8 has been supplied, the behavior will be unreliable. You must supply VCC_SRAM_1P8 either before or at the same time as VCC_HOST_1P8.

11.1.1.4 Power Up Sequence Timings and Thresholds

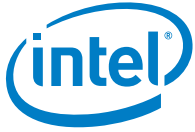
Table 54. Power Up Sequence Timing Parameters

Parameter	Description	Min.	Typical	Max.	Units
t _{PWR_OPM}	Time for regulator to properly regulate the output (AVD_VOPM_2P6 > 90%) when VCC_BATT_3P7 is applied	-	50	1000	us
t _{ON_QLR0}	Time interval for qLR0 to properly regulate the output when EN is asserted	-	40	-	ms
t _{ON_eSR}	Time interval for rail to properly regulate the output when EN is asserted	-	0.15	-	ms
t _{BATT_OPM}	Time between VCC_BATT_3P7 reaching 90% and VCC_AVD_OPM_2P6 reaching 90%	0	-	100	us
t _{BATT_AON}	Time between VCC_BATT_3P7 reaching 90% and VCC_AON_1P8 reaching 90%	0.2	-	2	ms
t _{POR_RST}	Time between VCC_AON_1P8 reaching 90% and RST_B (PAD) being released	-	40	-	ms
t _{START_RTC}	RTC Oscillator Start Up Time	0.2	0.35	1.0	s
t _{START_SI_OSC}	Silicon Oscillator Start Up Time	-	2	-	us
t _{START_XTAL_OSC}	Crystal Oscillator Start Up Time	-	2000	-	us
t _{HOST_PG}	Time between VCC_HOST_1P8 reaching 90% and PWRGOOD being released	6.5	-	-	ns

11.1.2 Sleep to Active

When the SoC is in the Sleep state and a wake event triggers, the following sequence occurs:

1. An enabled wake event is triggered and latched within the SoC.
2. If LPMODE_OPM is been enabled by software, then the PMU de-asserts LPMODE_OPM to take the OPM out of low power mode.
3. The PMU sets HOST_VR_EN to restart HOST_1P8.
 - This causes VCC_HOST_1P8 to ramp.
 - HOST_VR_ROK is asserted to indicate that HOST_1P8 has completed startup and is regulating properly. The regulator is said to be regulating properly once



the regulated supply is above 87% of its programmed value. Therefore, HOST_VR_OK indicates that VCC_HOST_1P8 is above 1.566V.

Note: It is recommended to program HOST_VR_ROK in a way that it is not masked.

- The PMU also requires that the VCC_HOST_1P8_PG SoC input is asserted to continue the wake up sequence.
- 4. The PMU releases WARM_RST# once the Host domain is ready to exit reset. Once WARM_RST# is released, it is synchronously de-asserted.

11.2 Power Down Sequences

The only power down sequence supported by the SoC is the sequence to enter the Sleep state.

Entry to the Sleep state is initiated as follows:

- Program SLP_CFG.LPMODE_EN to determine if OPM low power mode is entered in Sleep state.
- Write '1' to PM1C.SLPEN to initiate the transition.

The only mechanism to fully power down the SoC is to remove main power.

11.2.1 Active to Sleep

When the SoC is in the Active state and a sleep request is received, the following sequence occurs:

1. A request to enter the Sleep state is initiated by software writing '1' to PM1C.SLPEN.
2. The PMU asserts WARM_RST# to prepare for removing power from the Host domain.
3. The PMU clears HOST_VR_EN to put HOST_1P8 into Shutdown mode and pull VCC_HOST_1P8 to 0V.
4. VCC_HOST_1P8 drops to 0V, causing the Host domain to lose power.
 - The PMU waits for the deassertion of HOST_VR_ROK.
5. If SLP_CFG.LPMODE_EN is set to 1, the PMU asserts LPMODE_OPM to enable the OPM low power mode.
 - OPM low power mode requires all the switching regulators to be disabled with the LDOs enabled..

11.3 Reset Behavior

The SoC supports the following reset types:

- Power on reset



- Cold reset
- Warm reset

11.3.1 Power On Reset

The SoC provides a Power On Reset input, RST_B, that allows you to reset all logic within the SoC.

You must assert RST_B until VCC_AON_1P8 is stable to reliably reset the AON domain.

The assertion of RST_B resets all non-sticky, sticky and power-on reset sensitive logic.

Table 55. Power On Reset Triggers

Trigger	Description
RST_B pin asserted	External reset pin asserted
VCC_BATT_3P7 removed	Main power removed/cycled

11.3.2 Cold Reset

A cold reset triggers a reset of all host domain logic as well as all sticky logic within the AON domain.

If PLT_REG_EN is set to 0b, cold reset also triggers a power cycle of the Host domain by shutting down and subsequently restarting HOST_1P8.

You can configure the cold reset behavior of PLAT_3P3 and PLAT_1P8 through the PLAT3P3_VR and PLAT1P8_VR registers. This allows you to specify whether each rail is shutdown, reset, or unaffected by a cold reset.

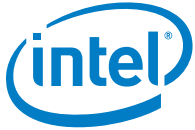
Note: If a platform rail is used to supply VCC_IO_AON, the rail must be configured to remain powered during cold reset. Otherwise, power to the IOs will be lost during cold reset leading to unreliable operation.

Note: If PLAT_1P8 is used to supply VCC_AON_1P8, the rail must be configured to remain powered during cold reset. Otherwise, power to the AON will be lost during cold reset, leading to unreliable operation.

Table 56. Cold Reset Triggers

Trigger	Description
Software writes 1 to RSTC.COLD	Software initiated through reset control register
BOR_VOPM asserted and PMNETCS.BOR_VOPM_RST_EN is set to 1	Cold reset triggered by on-die switching regulator BOR_VOPM condition

When a cold reset is triggered, the following sequence occurs:



1. A valid cold reset event is detected.
2. The PMU accepts the cold reset request and asserts both COLD_RST# and WARM_RST#.
3. The PMU de-asserts LPMODE_OPM to ensure the OPM is out of low power mode.
 - This ensures that if the cold reset was triggered while in a Sleep state with the LPMODE_OPM set to 1, it is cleared ahead of enabling any of the on-die platform rails.
4. The PMU clears HOST_VR_EN to put HOST_1P8 into Shutdown mode and pull VCC_HOST_1P8 to 0V. The on-die platform regulators are reset to defaults based on PLT_REG_EN strapping.
 - The PMU waits for the de-assertion of HOST_VR_ROK.
5. The PMU waits in cold reset for a configurable number of cycles. The number of cycles is controlled by the PM_WAIT.COLD_RST_WAIT register.
6. The PMU releases COLD_RST# and it is synchronously de-asserted.
7. The PMU sets HOST_VR_EN to re-start HOST_1P8.
 - This causes VCC_HOST_1P8 to ramp.
 - HOST_VR_ROK is asserted to indicate that HOST_1P8 has completed startup and is regulating properly. The regulator is said to be regulating properly once the regulated supply is above 87% of its programmed value. Therefore, HOST_VR_OK indicates that VCC_HOST_1P8 is above 1.566V.
 - The PMU also requires that the VCC_HOST_1P8_PG SoC input is asserted to continue the wake up sequence.
8. The PMU releases WARM_RST# once the Host domain is ready to exit reset. Once WARM_RST# is released, it is synchronously de-asserted.

11.3.3 Warm Reset

A warm reset triggers a reset of all Host logic and all non-sticky registers in the AON domain.

There is no power cycling of the Host or AON domains due to a warm reset.

Table 57. Warm Reset Triggers

Trigger	Description
Software writes 1 to RSTC.WARM	Software initiated through reset control register
Host watchdog expiration	Reset triggered by watchdog expiring
Sensor Subsystem Watchdog Expiration	Reset triggered by watchdog expiring
Host halt interrupt configured as warm reset	Reset triggered by an event routed to Host using Host Processor Interrupt Routing Mask registers with P_STS.HALT_INTR_REDIR set to 0b



Trigger	Description
Sensor subsystem halt interrupt configured as warm reset	Reset triggered by an event routed to sensor subsystem using Sensor Subsystem Interrupt Routing Mask registers with SS_CFG.HALT_INTR_REDIR set to 0b

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12 Thermal Management

12.1 Overview

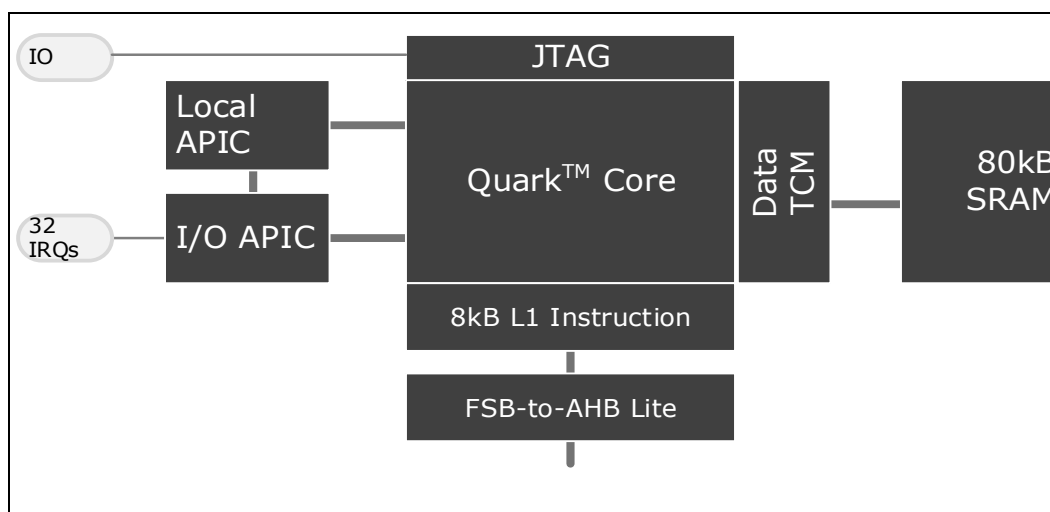
The Intel® Quark™ SE Microcontroller C1000 does not contain an integrated thermal sensor.

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13 Processor Core

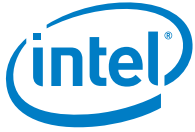
The Intel® Quark™ SE Microcontroller C1000 provides a single core x86 processor with an 8kB Instruction Cache and Data Tightly Coupled Memory (TCM) Interface.

Figure 17. Processor Core



13.1 Features

- Single Processor Core
- Single Instruction 5-stage pipeline
- 32-bit Processor with 32-bit Data Bus
- 8 kB, 2- way Instruction L1 Cache
- AHB-Lite FSB Interface
- Data TCM Interface to Internal System SRAM
 - Data Transfers for addresses matching the Internal System SRAM range will appear on the Data TCM Interface and transfers to address outside this range will appear on the AHB-Lite FSB Interface
- Support for IA 32-bit with Pentium x86 ISA compatibility
- Support for CPUID Instruction
- Support for long NOP Instruction
- Time Stamp Counter (TSC) accessed with the RDTSC instruction
- Integrated Local APIC
- Integrated IO APIC with support for 32 IRQs



- Supports C0, C1 and C2 Processor Power States
 - Supports Interrupt as Wake Events from C1 and C2
 - Time Stamp Counter runs in C1 and C2 States
 - Local APIC Timer runs in C1 and C2 States
- Support for PAE.XD and SMEP

Note: The processor does not provide an x87 Floating Point Unit (FPU) and does not support x87 FPU instructions.

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14 Memory Subsystem

The memory subsystem contains the following volatile and non-volatile memories:

- System Flash 0 (Quark SE) – 192Kbytes
- System Flash 1 (Sensor Subsystem) – 192Kbytes
- System ROM – 8Kbytes
(OTP implemented using Information Memory of Flash 0)
- Internal System SRAM – 80Kbytes

The Sensor Subsystem also has an 8Kbyte DCCM. These blocks are covered in [Chapter 8, “Sensor Subsystem”](#).

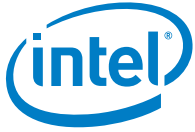
14.1 Features

14.1.1 System Flash Controller Features

- A Flash controller is instantiated per 192Kbyte Flash instance
- Supports 32 bit wide Instruction reads via an AHB Lite interface
The 32 bit reads can be performed as single read, incrementing burst or wrapping burst.
- Supports prefetching of 4 cache lines (1 cache line = 16 bytes) from Flash
Prefetching can be enabled/disabled via a configuration register
- Supports page erase via configuration registers in the System Control Module
- Each page is 2kbytes
- Supports 32 bit wide writes via configuration registers in the System Control Module

The procedure for updating Flash is as follows:

- Copy Flash Page with location to be modified to SRAM
- Erase the Flash page
- Update the relevant bytes in the SRAM copy
- Copy the modified page in SRAM into Flash
- Each write operation takes 40us (refer to Flash datasheet – $T_{nvs}(5us) + T_{pgs}(10us) + T_{prog}(20us) + T_{nvh}(5us)$), so total time to program Flash is 2.7 seconds.
- Supports mass erase via configuration registers in the System Control module
- Supports erase reference cell via configuration in the System Control Module



This is required to allow reads to work. You only need do this once in the device's lifetime.

- Generates accesses to Flash which adhere to the timing requirements of the Flash interface as specified in [1].
- Support configurable wait states to allow Flash to run with different frequency clocks

The number of wait states on Flash Read Access is as follows:

- Clk = 4MHz => 0 wait states supported on first access, 1 wait state on a subsequent access if the second access is on the next clock, 0 wait states on a subsequent access if there is at least a single clock cycle gap after the first access
- Clk = 8MHz => 1 wait state on all accesses
- Clk = 16MHz => 1 wait state on all accesses
- Clk = 32MHz => 2 wait states on all accesses
- Supports the following test features in test mode:
 - Provides direct access to Flash control signals
 - Provides direct access to Flash address signals
 - Provides access to either the upper 32 bits or the lower 32 bits of the 64 bit flash data bus, selectable via bit [2] of the address bus
- Supports a lock-out feature where Flash writes/erases are disabled via a register write

Once Flash writes have been disabled a soft reset is required to re-enable write access.

- Supports a memory protection read disable feature where memory can be partitioned in up to 4 regions with read control per region

An interrupt is generated if an access is attempted to a region of Flash which has reads disabled.

- Default protection is that all agents have access to full Flash memory
- Generates an interrupt when a Flash read or write access violation is detected
- Supports address re-mapping to allow multiple 192kbyte Flash instance appear as contiguous in the Intel® Quark™ SE Microcontroller C1000 level memory map.
- Support a scan mode where all the Flash control signals are gated during scan

14.1.2 System ROM Features

- System ROM is implemented using the information memory region of Flash0.
System Flash contains 192 kB of main memory which is used for instruction code and 8 kB of information memory.
- The 8 kB of System ROM is presented in the memory map as a single contiguous region.



- Supports 32 bit wide reads via an AHB Lite Interface.
- Write, page erase and erase reference cell supported as per [Chapter 14.1.1, “System Flash Controller Features”](#).
- Wait state behavior as per [Chapter 14.1.1, “System Flash Controller Features”](#).
- Supports a hardware lock mechanism to prevent writes to and erases of ROM. If byte 0 of the information memory region of Flash is 0x0, then hardware blocks all writes/erases of information memory.
- Supports a read disable feature where ROM reads can optionally be disabled on a 4kbyte granularity. An interrupt is generated if an access is attempted to ROM when information ROM reads are disabled.

14.1.3 Internal SRAM Features

- The internal SRAM controller presents 80kB of SRAM.
- Supports 64 bit wide reads via a dedicated Host Processor DTCM Interface.
- Supports 64 bit wide writes via a dedicated Host Processor Interface.
- Supports 32 bit wide reads via an AHB Lite Interface.
- Supports 32 bit wide writes via an AHB Lite Interface.
- A Rotated Priority access scheme is used to arbitrate between the DTCM Interface and the AHB Lite Interface. The arbitration scheme will result in 0 wait states being applied to the respective interface for arbitration win scenario and 1 wait state being applied to the respective interface for arbitration loss scenario.
- 4 Isolated Memory Regions (IMRs) with Agent based Memory Access Control. Agents are as follows:
 - Host Processor (over DTCM)
 - Sensor Processor (over AHB)
 - All other AHB masters are considered a single Agent (for example, DMA/USB)
- An interrupt is generated if an Agent without sufficient privileges attempts to access an IMR. The following violation details are also captured:
 - Agent ID
 - Access Type
 - Access Address

14.1.4 Flash Controller 0 Register Summary

MEM BaseAddress: 0xB0200000

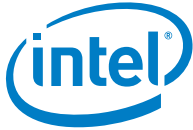


Table 58. Summary of Flash Controller 0 Register

MEM Address	Default	Name	Description
0x0	0000_0060h	TMG_CTRL	TMG_CTRL
0x4	0000_0000h	ROM_WR_CTRL	ROM_WR_CTRL
0x8	0000_0000h	ROM_WR_DATA	ROM_WR_DATA
0xC	0000_0000h	FLASH_WR_CTRL	FLASH_WR_CTRL
0x10	0000_0000h	FLASH_WR_DATA	FLASH_WR_DATA
0x14	0000_0000h	FLASH_STTS	FLASH_STTS
0x18	0000_0000h	CTRL	CTRL
0x1C	0000_0000h	FPR0_RD_CFG	FPR0_RD_CFG
0x20	0000_0000h	FPR1_RD_CFG	FPR1_RD_CFG
0x24	0000_0000h	FPR2_RD_CFG	FPR2_RD_CFG
0x28	0000_0000h	FPR3_RD_CFG	FPR3_RD_CFG
0x2C	0000_0000h	MPR_WR_CFG	MPR_WR_CFG
0x30	0000_0000h	MPR_VSTS	MPR_VSTS

14.1.5 Flash Controller 0 Register Detailed Description

TMG_CTRL (TMG_CTRL)

Flash Timing Control Register

MEM Offset (B0200000)	0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0060h

Table 59. Detailed Description of TMG_CTRL (TMG_CTRL)

Bits	Access Type	Default	Description
31:15	RO	17'h0	RSV (RSV) Reserved
14	RW	1'h0	CLK_SLOW (CLK_SLOW) Slow clock - when 1, zero wait state flash access is possible. When 0, flash accesses will always have one or more wait states. This bit must be set to zero when clock frequencies are above 6.7 MHz.
13:10	RW	4'h0	READ_WAIT_STATE_H (READ_WAIT_STATE_H) Flash SE high pulse width in system clocks plus one. Set to 0 for clock frequencies below 66MHz.



Bits	Access Type	Default	Description
9:6	RW	4'h1	READ_WAIT_STATE_L (READ_WAIT_STATE_L) Flash SE low pulse width in system clocks plus one. This must be set to one when the system clock frequency is above 20 MHz. This determines when the Flash controller generates a read data valid indication and is based on the Flash data access time. Please note that applying 1 to this register actually applies 2 wait states as READ_WAIT_STATE_L has an integrated +1
5:0	RW	6'h20	MICRO_SEC_CNT (MICRO_SEC_CNT) Number of clocks in a micro second.

Table 60. Typical values for TMG_CTRL (TMG_CTRL)

	CLK_SLOW	READ_WAIT_STATE_H	READ_WAIT_STATE_L
32kHz	1	0	0
4MHz	1	0	0
8MHz	0	0	0
16MHz	0	0	0
32MHz	0	0	1

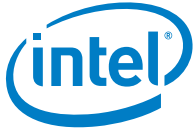
ROM_WR_CTRL (ROM_WR_CTRL)

ROM Write Control Register

MEM Offset (B0100000)	4h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 61. Detailed Description of ROM_WR_CTRL (ROM_WR_CTRL)

Bits	Access Type	Default	Description
31:20	RO	12'h0	RSV (RSV) Reserved
19:2	RW	18'b0	WR_ADDR (WR_ADDR) Write Address <i>On the Intel® Quark™ SE Microcontroller C1000, the information memory in the Flash 1 does not appear in the system memory map, so this register bit is unused.</i>



Bits	Access Type	Default	Description
1	RW/V	1'b0	ER_REQ (ER_REQ) Erase request - set to '1' to trigger a ROM Page Erase. Check the FLASH_STTS.ER_DONE bit to determine when the erase completes. ER_REQ is self clearing. ER_REQ has no effect after CTRL.FL_WR_DIS has been written to 1'b1. Hardware blocks all erases after ROM has been programmed. <i>On the Intel® Quark™ SE Microcontroller C1000, the information memory in the Flash 1 does not appear in the system memory map, so this register bit is unused</i>
0	RW/V	1'b0	WR_REQ (WR_REQ) Write request - set WR_REQ to '1' to trigger a ROM write. Check the FLASH_STTS.WR_DONE bit to determine when the write completes. WR_REQ is self clearing. WR_REQ has no effect after CTRL.FL_WR_DIS has been written to 1'b1. Hardware blocks all ROM writes after ROM has been programmed. <i>On the Intel® Quark™ SE Microcontroller C1000, the information memory in the Flash 1 does not appear in the system memory map, so this register bit is unused</i>

ROM_WR_DATA (ROM_WR_DATA)

ROM Write Data

MEM Offset (B0100000)	8h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 62. Detailed Description of ROM_WR_DATA (ROM_WR_DATA)

Bits	Access Type	Default	Description
31:0	RW	32'h0	DATA (DATA) ROM Write Data

FLASH_WR_CTRL (FLASH_WR_CTRL)

DCCM Base Address Register

MEM Offset (B0100000)	0Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 63. Detailed Description of FLASH_WR_CTRL (FLASH_WR_CTRL)

Bits	Access Type	Default	Description																				
31:20	RO	12'h0	RSV (RSV) Reserved																				
19:2	RW	18'b0	WR_ADDR (WR_ADDR) Write Address. WR_ADDR is a byte address. The write granularity to flash is a dword so for writes the 2 LSBs are unused. The following table shows the WR_ADDR to system address mapping: <table><tr><th>WR_ADDR[17:0]</th><th>System Address</th></tr><tr><td>18'h0</td><td>0x4000_0000</td></tr><tr><td>18'h4</td><td>0x4000_0004</td></tr><tr><td>...</td><td>...</td></tr><tr><td>18'h2_FFFC</td><td>0x4002_FFFC</td></tr></table> The page erase granularity to Flash is 2kbytes. The following table shows the WR_ADDR address setting required to erase each of the Flash pages. <table><tr><th>WR_ADDR[17:0]</th><th>System Address</th></tr><tr><td>18'h0</td><td>0x4000_0000 - 0x4000_07FF</td></tr><tr><td>18'h800</td><td>0x4000_0800 - 0x4000_0FFF</td></tr><tr><td>...</td><td>...</td></tr><tr><td>18'h2_F800</td><td>0x4002_F800 - 0x4002_FFFF</td></tr></table>	WR_ADDR[17:0]	System Address	18'h0	0x4000_0000	18'h4	0x4000_0004	...	...	18'h2_FFFC	0x4002_FFFC	WR_ADDR[17:0]	System Address	18'h0	0x4000_0000 - 0x4000_07FF	18'h800	0x4000_0800 - 0x4000_0FFF	...	...	18'h2_F800	0x4002_F800 - 0x4002_FFFF
WR_ADDR[17:0]	System Address																						
18'h0	0x4000_0000																						
18'h4	0x4000_0004																						
...	...																						
18'h2_FFFC	0x4002_FFFC																						
WR_ADDR[17:0]	System Address																						
18'h0	0x4000_0000 - 0x4000_07FF																						
18'h800	0x4000_0800 - 0x4000_0FFF																						
...	...																						
18'h2_F800	0x4002_F800 - 0x4002_FFFF																						
1	RW/V	1'b0	ER_REQ (ER_REQ) Erase request - set to '1' to trigger a Flash Page Erase. The page number is specified by WR_ADDR[17:11]. ER_REQ is self clearing. ER_REQ has no effect after CTRL.FL_WR_DIS has been written to '1'.																				
0	RW/V	1'b0	WR_REQ (WR_REQ) Write request - set WR_REQ to '1' to trigger a Flash write. Check the FLASH_STTS.WR_DONE bit to determine when the write completes. WR_REQ is self clearing. WR_REQ has no effect after CTRL.FL_WR_DIS has been written to '1'.																				

FLASH_WR_DATA (FLASH_WR_DATA)

Flash Write Data

MEM Offset (B0100000)	10h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 64. Detailed Description of FLASH_WR_DATA (FLASH_WR_DATA)

Bits	Access Type	Default	Description
31:0	RW	32'h0	DATA (DATA) Flash Write Data

FLASH_STTS (FLASH_STTS)

Flash Status

MEM Offset (B0100000)	14h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 65. Detailed Description of FLASH_STTS (FLASH_STTS)

Bits	Access Type	Default	Description
31:3	RO	29'h0	RSV (RSV) Reserved
2	RO/V	1'h0	ROM_PROG (ROM_PROG) ROM programmed - when set this indicates that ROM has been programmed and any further attempt to write ROM is blocked.
1	RO/C/V	1'b0	WR_DONE (WR_DONE) Write done - when set this indicates that a write operation has completed. WR_DONE is cleared on read.
0	RO/C/V	1'h0	ER_DONE (ER_DONE) Erase done - when set this indicates that an erase has completed. ER_DONE is cleared on read.

**CTRL (CTRL)**

Control Register

MEM Offset (B0100000)

18h

Security_PolicyGroup**IntelRsvd**

False

Size

32 bits

Default

0000_0000h

Table 66. Detailed Description of CTRL (CTRL)

Bits	Access Type	Default	Description	PowerWell
31:9	RO	23'h0	RSV (RSV) Reserved	
8	RW/V	1'h0	ERC (ERC) Erase reference	
7	RW/V	1'h0	MASS_ERASE (MASS_ERASE) Mass Erase - set to '1' to trigger an erase of Flash. This has no effect after FL_WR_DIS has been written to '1'.	
6	RW	1'h0	MASS_ERASE_INFO (MASS_ERASE_INFO) Mass Erase Info - Valid when MASS_ERASE is '1'. When MASS_ERASE_INFO = '1' then the ROM portion of Flash is erased during a Mass Erase. When MASS_ERASE_INFO = '0' then the ROM portion of Flash is not erased during a Mass Erase. If the ROM portion of Flash is detected as programmed by the Flash Controller then hardware will block a ROM erase. This has no effect after FL_WR_DIS has been written to '1'.	
5	RW	1'h0	LVE_MODE (LVE_MODE) Low Voltage mode	
4	RW/1S	1'h0	FL_WR_DIS (FL_WR_DIS) Flash Write Disable	
3	RW/1S	1'h0	ROM_RD_DIS_U (ROM_RD_DIS_U) Rom read disable for upper 4k region of ROM	
2	RW/1S	1'h0	ROM_RD_DIS_L (ROM_RD_DIS_L) Rom read disable for lower 4k region of ROM	
1	RW	1'h0	PRE_FLUSH (PRE_FLUSH) Prefetch buffer Flush	



0	RW	1'h0	PRE_EN (PRE_EN) Prefetch Enable. When '1' cache line prefetching is enabled. When '0' cacheline prefetching is disabled.	

FPRO_RD_CFG (FPRO_RD_CFG)

Flash Protection Region Read Control Register 0

MEM Offset (B0100000) 1Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 67. Detailed Description of FPRO_RD_CFG (FPRO_RD_CFG)

Bits	Access Type	Default	Description
31	RW/1S	1'h0	LOCK (LOCK) Lock the Memory Protection Region Configuration
30	RW/L	1'h0	ENABLE (ENABLE) Enable the Memory Protection Region
29:24	RO	6'h0	RSV2 (RSV2) Reserved
23:20	RW/L	4'h0	RD_ALLOW (RD_ALLOW) Enable Read Access on an Agent by Agent basis: [0] : Enables Read Access for the Host Processor [1] : Enables Read Access for the Sensor Subsystem [2] : Enables Read Access for DMA [3] : Enables Access for all other Agents
19:18	RO	2'h0	RSV1 (RSV1) Reserved
17:10	RW/L	8'h0	UPR_BOUND (UPR_BOUND) The Upper Address Bound is compared with 17:10 of the incoming address determine the upper 1kB aligned value of the Protected Region.
9:8	RO	2'h0	RSV (RSV) Reserved
7:0	RW/L	8'h0	LWR_BOUND (LWR_BOUND) The Lower Address Bound is compared with 17:10 of the incoming address determine the lower 1kB aligned value of the Protected Region.

FPR1_RD_CFG (FPR1_RD_CFG)

Flash Protection Region Read Control Register 1



MEM Offset (B0100000) 20h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 68. Detailed Description of FPR1_RD_CFG (FPR1_RD_CFG)

Bits	Access Type	Default	Description
31	RW/1S	1'h0	LOCK (LOCK) Lock the Memory Protection Region Configuration
30	RW/L	1'h0	ENABLE (ENABLE) Enable the Memory Protection Region
29:24	RO	6'h0	RSV2 (RSV2) Reserved
23:20	RW/L	4'h0	RD_ALLOW (RD_ALLOW) Enable Read Access on an Agent by Agent basis: [0] : Enables Read Access for the Host Processor [1] : Enables Read Access for the Sensor Subsystem [2] : Enables Read Access for DMA [3] : Enables Access for all other Agents
19:18	RO	2'h0	RSV1 (RSV1) Reserved
17:10	RW/L	8'h0	UPR_BOUND (UPR_BOUND) The Upper Address Bound is compared with 17:10 of the incoming address determine the upper 1kB aligned value of the Protected Region.
9:8	RO	2'h0	RSV (RSV) Reserved
7:0	RW/L	8'h0	LWR_BOUND (LWR_BOUND) The Lower Address Bound is compared with 17:10 of the incoming address determine the lower 1kB aligned value of the Protected Region.

FPR2_RD_CFG (FPR2_RD_CFG)

Flash Protection Region Read Control Register 2

MEM Offset (B0100000) 24h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h



Table 69. Detailed Description of FPR2_RD_CFG (FPR2_RD_CFG)

Bits	Access Type	Default	Description
31	RW/1S	1'h0	LOCK (LOCK) Lock the Memory Protection Region Configuration
30	RW/L	1'h0	ENABLE (ENABLE) Enable the Memory Protection Region
29:24	RO	6'h0	RSV2 (RSV2) Reserved
23:20	RW/L	4'h0	RD_ALLOW (RD_ALLOW) Enable Read Access on an Agent by Agent basis: [0] : Enables Read Access for the Host Processor [1] : Enables Read Access for the Sensor Subsystem [2] : Enables Read Access for DMA [3] : Enables Access for all other Agents
19:18	RO	2'h0	RSV1 (RSV1) Reserved
17:10	RW/L	8'h0	UPR_BOUND (UPR_BOUND) The Upper Address Bound is compared with 17:10 of the incoming address determine the upper 1kB aligned value of the Protected Region.
9:8	RO	2'h0	RSV (RSV) Reserved

FPR3_RD_CFG (FPR3_RD_CFG)

Flash Protection Region Read Control Register 3

MEM Offset (B0100000) 28h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 70. Detailed Description of FPR3_RD_CFG (FPR3_RD_CFG)

Bits	Access Type	Default	Description
31	RW/1S	1'h0	LOCK (LOCK) Lock the Memory Protection Region Configuration
30	RW/L	1'h0	ENABLE (ENABLE) Enable the Memory Protection Region
29:24	RO	6'h0	RSV2 (RSV2) Reserved



Bits	Access Type	Default	Description
23:20	RW/L	4'h0	RD_ALLOW (RD_ALLOW) Enable Read Access on an Agent by Agent basis: [0] : Enables Read Access for the Host Processor [1] : Enables Read Access for the Sensor Subsystem [2] : Enables Read Access for DMA [3] : Enables Access for all other Agents
19:18	RO	2'h0	RSV1 (RSV1) Reserved
17:10	RW/L	8'h0	UPR_BOUND (UPR_BOUND) The Upper Address Bound is compared with 17:10 of the incoming address determine the upper 1kB aligned value of the Protected Region.
9:8	RO	2'h0	RSV (RSV) Reserved
7:0	RW/L	8'h0	LWR_BOUND (LWR_BOUND) The Lower Address Bound is compared with 17:10 of the incoming address determine the lower 1kB aligned value of the Protected Region.

MPR_WR_CFG (MPR_WR_CFG)

Flash Write Protection Control Register

MEM Offset (B0100000)	2Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 71. Detailed Description of MPR_WR_CFG (MPR_WR_CFG)

Bits	Access Type	Default	Description
31	RW/1S	1'h0	Valid (Valid) Lock out further writes to Flash
30:0	RO	31'h0	RSV (RSV) Reserved

MPR_VSTS (MPR_VSTS)

Protection Status Register

MEM Offset (B0100000)	30h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 72. Detailed Description of MPR_VSTS (MPR_VSTS)

Bits	Access Type	Default	Description
31	RW/1C/V	1'h0	VALID (VALID) This field is asserted when a Violation Event Occurs. No further Violation Events will be captured in this register until this bit is cleared by SW.
30:23	RO	8'h0	RSV (RSV) Reserved
22:21	RO/V	2'h0	AGENT (AGENT) This field captures the Agent ID for an Access Violation - this field is valid for AHB violations only. 0: Host Processor 1: Sensor Subsystem 2: DMA Engine 3: Other Agents
20:18	RO/V	3'h0	TYPE (TYPE) This field captures the Transfer Type for an Access Violation: 0: ROM Read (via AHB) 1: ROM Write (via AHB) 2: Flash Read (via AHB) 3: Flash Write (via AHB) 4: Flash Write/erase (via CREG) 5: ROM Write/erase (via CREG)
17:0	RO/V	18'h0	ADDR (ADDR) This field captures the invalid address that was detected during a violation.

14.1.6 Flash Controller 1 Register Summary

MEM BaseAddress: 0xB0200000

Table 73. Summary of Flash Controller 1 Register

MEM Address	Default	Name	Description
0x0	0000_0060h	TMG_CTRL	TMG_CTRL
0x4	0000_0000h	ROM_WR_CTRL	ROM_WR_CTRL
0x8	0000_0000h	ROM_WR_DATA	ROM_WR_DATA
0xC	0000_0000h	FLASH_WR_CTRL	FLASH_WR_CTRL
0x10	0000_0000h	FLASH_WR_DATA	FLASH_WR_DATA
0x14	0000_0000h	FLASH_STTS	FLASH_STTS
0x18	0000_0000h	CTRL	CTRL



MEM Address	Default	Name	Description
0x1C	0000_0000h	FPR0_RD_CFG	FPR0_RD_CFG
0x20	0000_0000h	FPR1_RD_CFG	FPR1_RD_CFG
0x24	0000_0000h	FPR2_RD_CFG	FPR2_RD_CFG
0x28	0000_0000h	FPR3_RD_CFG	FPR3_RD_CFG
0x2C	0000_0000h	MPR_WR_CFG	MPR_WR_CFG
0x30	0000_0000h	MPR_VSTS	MPR_VSTS

14.1.7 Flash Controller 1 Register Detailed Description

TMG_CTRL (TMG_CTRL)

Flash Timing Control Register

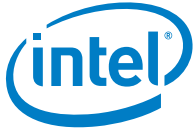
MEM Offset (B0200000)	0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0060h

Table 74. Detailed Description of TMG_CTRL (TMG_CTRL)

Bits	Access Type	Default	Description
31:15	RO	17'h0	RSV (RSV) Reserved
14	RW	1'h0	CLK_SLOW (CLK_SLOW) Slow clock - when 1, zero wait state flash access is possible. When 0, flash accesses will always have one or more wait states. This bit must be set to zero when clock frequencies are above 6.7 MHz.
13:10	RW	4'h0	READ_WAIT_STATE_H (READ_WAIT_STATE_H) Flash SE high pulse width in system clocks plus one. Set to 0 for clock frequencies below 66MHz.
9:6	RW	4'h1	READ_WAIT_STATE_L (READ_WAIT_STATE_L) Flash SE low pulse width in system clocks plus one. This must be set to one when the system clock frequency is above 20 MHz. This determines when the Flash controller generates a read data valid indication and is based on the Flash data access time.
5:0	RW	6'h20	MICRO_SEC_CNT (MICRO_SEC_CNT) Number of clocks in a micro second.

ROM_WR_CTRL (ROM_WR_CTRL)

ROM Write Control Register



MEM Offset (B0200000) 4h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 75. Detailed Description of ROM_WR_CTRL (ROM_WR_CTRL)

Bits	Access Type	Default	Description
31:20	RO	12'h0	RSV (RSV) Reserved
19:2	RW	18'b0	WR_ADDR (WR_ADDR) Write Address <i>On Intel® Quark™ SE Microcontroller C1000, the information memory in the Flash 1 does not appear in the system memory map, so this register bit is unused.</i>
1	RW/V	1'b0	ER_REQ (ER_REQ) Erase request - set to '1' to trigger a ROM Page Erase. Check the FLASH_STTS.ER_DONE bit to determine when the erase completes. ER_REQ is self clearing. ER_REQ has no effect after CTRL.FL_WR_DIS has been written to 1'b1. Hardware blocks all erases after ROM has been programmed. <i>On Intel® Quark™ SE Microcontroller C1000, the information memory in the Flash 1 does not appear in the system memory map, so this register bit is unused</i>
0	RW/V	1'b0	WR_REQ (WR_REQ) Write request - set WR_REQ to '1' to trigger a ROM write. Check the FLASH_STTS.WR_DONE bit to determine when the write completes. WR_REQ is self clearing. WR_REQ has no effect after CTRL.FL_WR_DIS has been written to 1'b1. Hardware blocks all ROM writes after ROM has been programmed. <i>On Intel® Quark™ SE Microcontroller C1000, the information memory in the Flash 1 does not appear in the system memory map, so this register bit is unused</i>

ROM_WR_DATA (ROM_WR_DATA)

ROM Write Data

MEM Offset (B0200000) 8h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h



Table 76. Detailed Description of ROM_WR_DATA (ROM_WR_DATA)

Bits	Access Type	Default	Description
31:0	RW	32'h0	DATA (DATA) ROM Write Data <i>On Intel® Quark™ SE Microcontroller C1000, the information memory in the Flash 1 does not appear in the system memory map, so this register bit is unused</i>

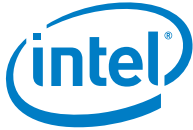
FLASH_WR_CTRL (FLASH_WR_CTRL)

DCCM Base Address Register

MEM Offset (B0200000)	0Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 77. Detailed Description of FLASH_WR_CTRL (FLASH_WR_CTRL)

Bits	Access Type	Default	Description																				
31:20	RO	12'h0	RSV (RSV) Reserved																				
19:2	RW	18'b0	WR_ADDR (WR_ADDR) Write Address. WR_ADDR is a byte address. The write granularity to flash is a dword so for writes the 2 LSBs are unused. The following table shows the WR_ADDR to system address mapping: <table><tr><th>WR_ADDR[17:0]</th><th>System Address</th></tr><tr><td>18'h0</td><td>0x4003_0000</td></tr><tr><td>18'h4</td><td>0x4003_0004</td></tr><tr><td>...</td><td>...</td></tr><tr><td>18'h2_FFFC</td><td>0x4005_FFFC</td></tr></table> The page erase granularity to Flash is 2kbytes. The following table shows the WR_ADDR address setting required to erase each of the Flash pages. <table><tr><th>WR_ADDR[17:0]</th><th>System Address</th></tr><tr><td>18'h0</td><td>0x4003_0000 - 0x4003_07FF</td></tr><tr><td>18'h800</td><td>0x4003_0800 - 0x4003_0FFF</td></tr><tr><td>...</td><td>...</td></tr><tr><td>18'h2_F800</td><td>0x4005_F800 - 0x4005_FFFF</td></tr></table>	WR_ADDR[17:0]	System Address	18'h0	0x4003_0000	18'h4	0x4003_0004	...	...	18'h2_FFFC	0x4005_FFFC	WR_ADDR[17:0]	System Address	18'h0	0x4003_0000 - 0x4003_07FF	18'h800	0x4003_0800 - 0x4003_0FFF	...	...	18'h2_F800	0x4005_F800 - 0x4005_FFFF
WR_ADDR[17:0]	System Address																						
18'h0	0x4003_0000																						
18'h4	0x4003_0004																						
...	...																						
18'h2_FFFC	0x4005_FFFC																						
WR_ADDR[17:0]	System Address																						
18'h0	0x4003_0000 - 0x4003_07FF																						
18'h800	0x4003_0800 - 0x4003_0FFF																						
...	...																						
18'h2_F800	0x4005_F800 - 0x4005_FFFF																						



Bits	Access Type	Default	Description
1	RW/V	1'b0	ER_REQ (ER_REQ) Erase request - set to '1' to trigger a Flash Page Erase. The page number is specified by WR_ADDR[17:11]. ER_REQ is self clearing. ER_REQ has no effect after CTRL.FL_WR_DIS has been written to '1'. Note: Hardware blocks all ROM writes the OTP bit in ROM is programmed. The OTP bit in ROM is programmed by writing '0' to bit 0 of address 0 in the ROM. Once this is done all further writes to ROM are blocked by hardware. The OTP bit should not be programmed in a debug environment.
0	RW/V	1'b0	WR_REQ (WR_REQ) Write request - set WR_REQ to '1' to trigger a Flash write. Check the FLASH_STTS.WR_DONE bit to determine when the write completes. WR_REQ is self clearing. WR_REQ has no effect after CTRL.FL_WR_DIS has been written to '1'.

FLASH_WR_DATA (FLASH_WR_DATA)

Flash Write Data

MEM Offset (B0200000)	10h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 78. Detailed Description of FLASH_WR_DATA (FLASH_WR_DATA)

Bits	Access Type	Default	Description
31:0	RW	32'h0	DATA (DATA) Flash Write Data

FLASH_STTS (FLASH_STTS)

Flash Status

MEM Offset (B0200000)	14h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 79. Detailed Description of FLASH_STTS (FLASH_STTS)

Bits	Access Type	Default	Description
31:3	RO	29'h0	RSV (RSV) Reserved



Bits	Access Type	Default	Description
2	RO/V	1'h0	ROM_PROG (ROM_PROG) ROM programmed - when set this indicates that ROM has been programmed and any further attempt to write ROM is blocked.
1	RO/C/V	1'b0	WR_DONE (WR_DONE) Write done - when set this indicates that a write operation has completed. WR_DONE is cleared on read.
0	RO/C/V	1'h0	ER_DONE (ER_DONE) Erase done - when set this indicates that an erase has completed. ER_DONE is cleared on read.

CTRL (CTRL)

Control Register

MEM Offset (B0200000)	18h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 80. Detailed Description of CTRL (CTRL)

Bits	Access Type	Default	Description
31:9	RO	23'h0	RSV (RSV) Reserved
8	RW/V	1'h0	ERC (ERC) Erase reference
7	RW/V	1'h0	MASS_ERASE (MASS_ERASE) Mass Erase - set to '1' to trigger an erase of Flash. This has no effect after FL_WR_DIS has been written to '1'.
6	RW	1'h0	MASS_ERASE_INFO (MASS_ERASE_INFO) Mass Erase Info - Valid when MASS_ERASE is '1'. When MASS_ERASE_INFO = '1' then the ROM portion of Flash is erased during a Mass Erase. When MASS_ERASE_INFO = '0' then the ROM portion of Flash is not erased during a Mass Erase. If the ROM portion of Flash is detected as programmed by the Flash Controller then hardware will block a ROM erase. This has no effect after FL_WR_DIS has been written to '1'.
5	RW	1'h0	LVE_MODE (LVE_MODE) Low Voltage mode
4	RW/1S	1'h0	FL_WR_DIS (FL_WR_DIS) Flash Write Disable
3	RW/1S	1'h0	ROM_RD_DIS_U (ROM_RD_DIS_U) Rom read disable for upper 4k region of ROM



Bits	Access Type	Default	Description
2	RW/1S	1'h0	ROM_RD_DIS_L (ROM_RD_DIS_L) Rom read disable for lower 4k region of ROM
1	RW	1'h0	PRE_FLUSH (PRE_FLUSH) Prefetch buffer Flush
0	RW	1'h0	PRE_EN (PRE_EN) Prefetch Enable. When '1' cache line prefetching is enabled. When '0' cacheline prefetching is disabled.

FPRO_RD_CFG (FPRO_RD_CFG)

Flash Protection Region Read Control Register 0

MEM Offset (B0200000)	1Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 81. Detailed Description of FPRO_RD_CFG (FPRO_RD_CFG)

Bits	Access Type	Default	Description
31	RW/1S	1'h0	LOCK (LOCK) Lock the Memory Protection Region Configuration
30	RW/L	1'h0	ENABLE (ENABLE) Enable the Memory Protection Region
29:24	RO	6'h0	RSV2 (RSV2) Reserved
23:20	RW/L	4'h0	RD_ALLOW (RD_ALLOW) Enable Read Access on an Agent by Agent basis: [0] : Enables Read Access for the Host Processor [1] : Enables Read Access for the Sensor Subsystem [2] : Enables Read Access for DMA [3] : Enables Access for all other Agents
19:18	RO	2'h0	RSV1 (RSV1) Reserved
17:10	RW/L	8'h0	UPR_BOUND (UPR_BOUND) The Upper Address Bound is compared with 17:10 of the incoming address determine the upper 1kB aligned value of the Protected Region.
9:8	RO	2'h0	RSV (RSV) Reserved



Bits	Access Type	Default	Description
7:0	RW/L	8'h0	LWR_BOUND (LWR_BOUND) The Lower Address Bound is compared with 17:10 of the incoming address determine the lower 1kB aligned value of the Protected Region.

FPR1_RD_CFG (FPR1_RD_CFG)

Flash Protection Region Read Control Register 1

MEM Offset (B0200000)	20h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 82. Detailed Description of FPR1_RD_CFG (FPR1_RD_CFG)

Bits	Access Type	Default	Description
31	RW/1S	1'h0	LOCK (LOCK) Lock the Memory Protection Region Configuration
30	RW/L	1'h0	ENABLE (ENABLE) Enable the Memory Protection Region
29:24	RO	6'h0	RSV2 (RSV2) Reserved
23:20	RW/L	4'h0	RD_ALLOW (RD_ALLOW) Enable Read Access on an Agent by Agent basis: [0] : Enables Read Access for the Host Processor [1] : Enables Read Access for the Sensor Subsystem [2] : Enables Read Access for DMA [3] : Enables Access for all other Agents
19:18	RO	2'h0	RSV1 (RSV1) Reserved
17:10	RW/L	8'h0	UPR_BOUND (UPR_BOUND) The Upper Address Bound is compared with 17:10 of the incoming address determine the upper 1kB aligned value of the Protected Region.
9:8	RO	2'h0	RSV (RSV) Reserved
7:0	RW/L	8'h0	LWR_BOUND (LWR_BOUND) The Lower Address Bound is compared with 17:10 of the incoming address determine the lower 1kB aligned value of the Protected Region.

FPR2_RD_CFG (FPR2_RD_CFG)

Flash Protection Region Read Control Register 2



MEM Offset (B0200000) 24h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 83. Detailed Description of FPR2_RD_CFG (FPR2_RD_CFG)

Bits	Access Type	Default	Description
31	RW/1S	1'h0	LOCK (LOCK) Lock the Memory Protection Region Configuration
30	RW/L	1'h0	ENABLE (ENABLE) Enable the Memory Protection Region
29:24	RO	6'h0	RSV2 (RSV2) Reserved
23:20	RW/L	4'h0	RD_ALLOW (RD_ALLOW) Enable Read Access on an Agent by Agent basis: [0] : Enables Read Access for the Host Processor [1] : Enables Read Access for the Sensor Subsystem [2] : Enables Read Access for DMA [3] : Enables Access for all other Agents
19:18	RO	2'h0	RSV1 (RSV1) Reserved
17:10	RW/L	8'h0	UPR_BOUND (UPR_BOUND) The Upper Address Bound is compared with 17:10 of the incoming address determine the upper 1kB aligned value of the Protected Region.
9:8	RO	2'h0	RSV (RSV) Reserved
7:0	RW/L	8'h0	LWR_BOUND (LWR_BOUND) The Lower Address Bound is compared with 17:10 of the incoming address determine the lower 1kB aligned value of the Protected Region.

FPR3_RD_CFG (FPR3_RD_CFG)

Flash Protection Region Read Control Register 3

MEM Offset (B0200000) 28h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h



Table 84. Detailed Description of FPR3_RD_CFG (FPR3_RD_CFG)

Bits	Access Type	Default	Description
31	RW/1S	1'h0	LOCK (LOCK) Lock the Memory Protection Region Configuration
30	RW/L	1'h0	ENABLE (ENABLE) Enable the Memory Protection Region
29:24	RO	6'h0	RSV2 (RSV2) Reserved
23:20	RW/L	4'h0	RD_ALLOW (RD_ALLOW) Enable Read Access on an Agent by Agent basis: [0] : Enables Read Access for the Host Processor [1] : Enables Read Access for the Sensor Subsystem [2] : Enables Read Access for DMA [3] : Enables Access for all other Agents
19:18	RO	2'h0	RSV1 (RSV1) Reserved
17:10	RW/L	8'h0	UPR_BOUND (UPR_BOUND) The Upper Address Bound is compared with 17:10 of the incoming address determine the upper 1kB aligned value of the Protected Region.
9:8	RO	2'h0	RSV (RSV) Reserved
7:0	RW/L	8'h0	LWR_BOUND (LWR_BOUND) The Lower Address Bound is compared with 17:10 of the incoming address determine the lower 1kB aligned value of the Protected Region.

MPR_WR_CFG (MPR_WR_CFG)

Flash Write Protection Control Register

MEM Offset (B0200000)	2Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 85. Detailed Description of MPR_WR_CFG (MPR_WR_CFG)

Bits	Access Type	Default	Description
31	RW/1S	1'h0	Valid (Valid) Lock out further writes to Flash
30:0	RO	31'h0	RSV (RSV) Reserved

**MPR_VSTS (MPR_VSTS)**

Protection Status Register

MEM Offset (B0200000) 30h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 86. Detailed Description of MPR_VSTS (MPR_VSTS)

Bits	Access Type	Default	Description
31	RW/1C/V	1'h0	VALID (VALID) This field is asserted when a Violation Event Occurs. No further Violation Events will be captured in this register until this bit is cleared by SW.
30:23	RO	8'h0	RSV (RSV) Reserved
22:21	RO/V	2'h0	AGENT (AGENT) This field captures the Agent ID for an Access Violation - this field is valid for AHB violations only. 0: Host Processor 1: Sensor Subsystem 2: DMA Engine 3: Other Agents
20:18	RO/V	3'h0	TYPE (TYPE) This field captures the Transfer Type for an Access Violation: 0: ROM Read (via AHB) 1: ROM Write (via AHB) 2: Flash Read (via AHB) 3: Flash Write (via AHB) 4: Flash Write/erase (via CREG) 5: ROM Write/erase (via CREG)
17:0	RO/V	18'h0	ADDR (ADDR) This field captures the invalid address that was detected during a violation.

14.1.8 Internal SRAM Register Summary

MEM BaseAddress: 0xB0400000



Table 87. Summary of Internal SRAM Registry

MEM Address	Default	Name	Description
0x0	0000_0000h	MPR0_CFG	MPR_CFG
0x4	0000_0000h	MPR1_CFG	MPR_CFG
0x8	0000_0000h	MPR2_CFG	MPR_CFG
0xC	0000_0000h	MPR3_CFG	MPR_CFG
0x10	FFFF_FFFFh	MPR_VDATA	MPR_VDATA
0x14	0000_0000h	MPR_VSTS	MPR_VSTS

14.1.9 Internal SRAM Register Detailed Description

MPR_CFG (MPR0_CFG)

Memory Protection Region Configuration Register

MEM Offset (B0400000)	0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 88. Detailed Description of MPR_CFG (MPR0_CFG)

Bits	Access Type	Default	Description
31	RW/1S	1'b0	MPR Lock (LOCK) Lock the Memory Protection Region Configuration
30	RW/L	1'b0	MPR Enable (ENABLE) Enable the Memory Protection Region
29:27	RO	3'b0	RSV4 (RSV4) Reserved
26:24	RW/L	3'b0	MPR Read Access Allow (RD_ALLOW) Enable Read Access on an Agent by Agent basis: [0] : Enables Read Access for the Host Processor [1] : Enables Read Access for the Sensor SubSystem Processor [2] : Enables Read Access for all Other Agents
23	RO	1'b0	RSV3 (RSV3) Reserved
22:20	RW/L	3'b0	MPR Write Access Allow (WR_ALLOW) Enable Write Access on an Agent by Agent basis: Bit [0] : Enables Write Access for the Host Processor Bit [1] : Enables Write Access for the Sensor SubSystem Processor Bit [2] : Enables Write Access for all Other Agents



Bits	Access Type	Default	Description
19:17	RO	3'b0	RSV2 (RSV2) Reserved
16:10	RW/L	7'b0	MPR Upper Bound (UPR_BOUND) The Upper Address Bound is compared with 16:10 of the incoming address determine the upper 1kB aligned value of the Protected Region.
9:7	RO	3'b0	RSV1 (RSV1) Reserved
6:0	RW/L	7'b0	MPR Lower Bound (LWR_BOUND) The Lower Address Bound is compared with 16:10 of the incoming address determine the lower 1kB aligned value of the Protected Region.

MPR_CFG (MPR1_CFG)

Memory Protection Region Configuration Register

MEM Offset (B0400000)	4h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 89. Detailed Description of MPR_CFG (MPR1_CFG)

Bits	Access Type	Default	Description
31	RW/1S	1'b0	MPR Lock (LOCK) Lock the Memory Protection Region Configuration
30	RW/L	1'b0	MPR Enable (ENABLE) Enable the Memory Protection Region
29:27	RO	3'b0	RSV4 (RSV4) Reserved
26:24	RW/L	3'b0	MPR Read Access Allow (RD_ALLOW) Enable Read Access on an Agent by Agent basis: [0] : Enables Read Access for the Host Processor [1] : Enables Read Access for the Sensor SubSystem Processor [2] : Enables Read Access for all Other Agents
23	RO	1'b0	RSV3 (RSV3) Reserved
22:20	RW/L	3'b0	MPR Write Access Allow (WR_ALLOW) Enable Write Access on an Agent by Agent basis: Bit [0] : Enables Write Access for the Host Processor Bit [1] : Enables Write Access for the Sensor SubSystem Processor Bit [2] : Enables Write Access for all Other Agents



Bits	Access Type	Default	Description
19:17	RO	3'b0	RSV2 (RSV2) Reserved
16:10	RW/L	7'b0	MPR Upper Bound (UPR_BOUND) The Upper Address Bound is compared with 16:10 of the incoming address determine the upper 1kB aligned value of the Protected Region.
9:7	RO	3'b0	RSV1 (RSV1) Reserved
6:0	RW/L	7'b0	MPR Lower Bound (LWR_BOUND) The Lower Address Bound is compared with 16:10 of the incoming address determine the lower 1kB aligned value of the Protected Region.

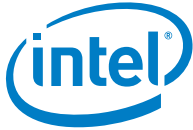
MPR_CFG (MPR2_CFG)

Memory Protection Region Configuration Register

MEM Offset (B0400000)	8h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 90. Detailed Description of MPR_CFG (MPR2_CFG)

Bits	Access Type	Default	Description
31	RW/1S	1'b0	MPR Lock (LOCK) Lock the Memory Protection Region Configuration
30	RW/L	1'b0	MPR Enable (ENABLE) Enable the Memory Protection Region
29:27	RO	3'b0	RSV4 (RSV4) Reserved
26:24	RW/L	3'b0	MPR Read Access Allow (RD_ALLOW) Enable Read Access on an Agent by Agent basis: [0] : Enables Read Access for the Host Processor [1] : Enables Read Access for the Sensor SubSystem Processor [2] : Enables Read Access for all Other Agents
23	RO	1'b0	RSV3 (RSV3) Reserved
22:20	RW/L	3'b0	MPR Write Access Allow (WR_ALLOW) Enable Write Access on an Agent by Agent basis: Bit [0] : Enables Write Access for the Host Processor Bit [1] : Enables Write Access for the Sensor SubSystem Processor Bit [2] : Enables Write Access for all Other Agents



Bits	Access Type	Default	Description
19:17	RO	3'b0	RSV2 (RSV2) Reserved
16:10	RW/L	7'b0	MPR Upper Bound (UPR_BOUND) The Upper Address Bound is compared with 16:10 of the incoming address determine the upper 1kB aligned value of the Protected Region.
9:7	RO	3'b0	RSV1 (RSV1) Reserved
6:0	RW/L	7'b0	MPR Lower Bound (LWR_BOUND) The Lower Address Bound is compared with 16:10 of the incoming address determine the lower 1kB aligned value of the Protected Region.

MPR_CFG (MPR3_CFG)

Memory Protection Region Configuration Register

MEM Offset (B0400000)	0Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 91. Detailed Description of MPR_CFG (MPR3_CFG)

Bits	Access Type	Default	Description
31	RW/1S	1'b0	MPR Lock (LOCK) Lock the Memory Protection Region Configuration
30	RW/L	1'b0	MPR Enable (ENABLE) Enable the Memory Protection Region
29:27	RO	3'b0	RSV4 (RSV4) Reserved
26:24	RW/L	3'b0	MPR Read Access Allow (RD_ALLOW) Enable Read Access on an Agent by Agent basis: [0] : Enables Read Access for the Host Processor [1] : Enables Read Access for the Sensor SubSystem Processor [2] : Enables Read Access for all Other Agents
23	RO	1'b0	RSV3 (RSV3) Reserved
22:20	RW/L	3'b0	MPR Write Access Allow (WR_ALLOW) Enable Write Access on an Agent by Agent basis: Bit [0] : Enables Write Access for the Host Processor Bit [1] : Enables Write Access for the Sensor SubSystem Processor Bit [2] : Enables Write Access for all Other Agents



Bits	Access Type	Default	Description
19:17	RO	3'b0	RSV2 (RSV2) Reserved
16:10	RW/L	7'b0	MPR Upper Bound (UPR_BOUND) The Upper Address Bound is compared with 16:10 of the incoming address determine the upper 1kB aligned value of the Protected Region.
9:7	RO	3'b0	RSV1 (RSV1) Reserved
6:0	RW/L	7'b0	MPR Lower Bound (LWR_BOUND) The Lower Address Bound is compared with 16:10 of the incoming address determine the lower 1kB aligned value of the Protected Region.

MPR_VDATA (MPR_VDATA)

Memory Protection Region Violation Data Value

MEM Offset (B0400000)	10h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	FFFF_FFFFh

Table 92. Detailed Description of MPR_VDATA (MPR_VDATA)

Bits	Access Type	Default	Description
31:0	RW/O	32'hFFFFFFFF	MPR Violation Data (VDATA) This field controls the data returned to Agents that violate the MPR Access rules

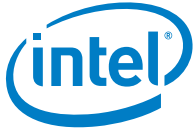
MPR_VSTS (MPR_VSTS)

Memory Protection Region Violation Details

MEM Offset (B0400000)	14h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 93. Detailed Description of MPR_VSTS (MPR_VSTS)

Bits	Access Type	Default	Description
31	RW/1C/V	1'b0	MPR Violation Details Valid (VALID) This field is asserted when a Violation Event Occurs. No further Violation Events will be captured in this register until this bit is cleared by SW.



Bits	Access Type	Default	Description
30:20	RO	11'b0	RSV (RSV) Reserved
19:18	RO/V	2'b0	MPR Violation Agent ID (AGENT) This field captures the Agent ID for an Access Violation: 0: Host Processor 1: Sensor SubSystem Processor 2: Other Agents
17	RO/V	1'b0	MPR Violation Agent ID (TYPE) This field captures the Transfer Type for an Access Violation: 0: Read 1: Write
16:0	RO/V	17'b0	MPR Violation Address (ADDR) This field captures the Address for an Access Violation.

14.1.10 CREG Register Detailed Description

IO_CREG_MST0_CTRL (IO_CREG_MST0_CTRL)

CREG control register

MEM Offset (80018000)	0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 94. Detailed Description of IO_CREG_MST0_CTRL (IO_CREG_MST0_CTRL)

Bits	Access Type	Default	Description
31	RW	32'h0	ADC_CLK_GATE (ADC_CLK_GATE) When ADC_CLK_GATE is 1 it indicates that the ADC peripheral is inactive and its clock can be gated.
30	RW	32'h0	I2C1_CLK_GATE (I2C1_CLK_GATE) When I2C1_CLK_GATE is 1 it indicates that the I2C 1 peripheral is inactive and its clock can be gated.
29	RW	32'h0	I2C0_CLK_GATE (I2C0_CLK_GATE) When I2C0_CLK_GATE is 1 it indicates that the I2C 0 peripheral is inactive and its clock can be gated.
28	RW	32'h0	SPI1_CLK_GATE (SPI0_CLK_GATE) When SPI1_CLK_GATE is 1 it indicates that the SPI 1 peripheral is inactive and its clock can be gated.



Bits	Access Type	Default	Description
27	RW	32'h0	SPIO_CLK_GATE (SPIO_CLK_GATE) When SPIO_CLK_GATE is 1 it indicates that the SPI 0 peripheral is inactive and its clock can be gated.
26:20	RW	32'h0	ADC CALIBRATION VALUE (ADC_CAL_VAL) ADC calibration value to be loaded during a "load calibration" command
19:17	RW	32'h0	ADC CALIBRATION COMMAND (ADC_CAL_CMD) ADC Calibration Command – setting as follows: "010" – Reset calibration "011" – Start calibration "100" – Load Calibration
16	RW	1'h0	ADC CALIBRATION REQUEST (ADC_CAL_REQ) Write to 1 to initiate a calibration command. Write to 0 once the calibration command is complete.
15:3	RW	13'h0	ADC DELAY (ADC_DELAY) Configures the amount of time the ADC Power Mode FSM stays in each state. Required to meet ADC HIP timing specs. ADC_DELAY should be configured as follows based on the system clock frequency: 4 MHz -> 20 8 MHz -> 40 16 MHz -> 80 32 MHz -> 160
2:0	RW	3'h0	ADC Power Mode (ADC_PWR_MODE) Selects the ADC power mode – settings as follows: "000" – Deep Power Down "001" – Power Down "010" – Standby "011" – Normal Mode with calibration "100" – Normal Mode without calibration A transition to a new state is initiated by writing the requested state to ADC_PWR_MODE. Hardware takes care of the sequencing between the states. Notes: After exiting the deep power down mode a dummy conversion is required – this must be done by software via the Sensor Subsystem ADC interface. If offset is a critical parameter, then after exiting the deep power down state, either a load calibration or a start calibration command must be performed.

IO_CREG_SLV0_OBSR (IO_CREG_SLV0_OBSR)

This register is used to control the CREG Slave Interface

MEM Offset (80018000)

80h

Security_PolicyGroup



IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 95. CREG1 Slave Bit Assignment

Bits	Access Type	Default	Description
11:5	RO	1'h0	ADC CALIBRATION VALUE (ADC_CAL_VAL) This contains the ADC calibration value returned after a calibration cycle.
4	RO	1'h0	ADC CALIBRATION ACKNOWLEDGE (ADC_CAL_ACK) ADC_CAL_ACK is '1' when a requested calibration operation has completed, it is cleared when software clears IO_CREG_MST0_CTRL.ADC_CAL_REQ
3:1	RO	3'h0	ADC POWER MODE (ADC_PWR_MODE) Indicates the current power mode of the ADC. "000" – Deep Power Down "001" – Power Down "010" – Standby "011" – Normal Mode with calibration "100" – Normal Mode without calibration
0	RO	1'h0	ADC POWER MODE STATUS (ADC_PWR_MODE_STS) This is '1' when the requested power state equals the current power state, and is '0' when the requested power state does not equal the current power state.

IO_CREG_SLV1_OBSR (IO_CREG_SLV1_OBSR)

This register is used to control the CREG Slave Interface

MEM Offset (80018000) 180h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 96. Detailed Description of IO_CREG_SLV1_OBSR (IO_CREG_SLV1_OBSR)

Bits	Access Type	Default	Description
31:0	RO	32'h0	TIMESTAMP (TSTMP) This is connected to the always on counter – it can be used for time stamping samples received from sensors.



15 USB

15.1 Signal Descriptions

Table 97. USB Controller Signals

Signal Name	Direction/ Type	Description
USB_PADP	IO	USB Positive differential signal
USB_PADN	IO	USB Negative differential signal
USB_VCC3P3	I	USB 3.3V
USB_VSS	I	USB Ground

15.2 Features

- Supports USB 1.1 Full speed only (12Mbps)
- Supports internal DMA
 - Buffer mode DMA supported (scatter gather mode is *not* supported)
 - DMA control per endpoint per direction supported
 - Generates DMA interrupt after a configurable number of bytes/packets have been transmitted
- Supports 1 control endpoint
- Supports 3 bidirectional endpoints (in addition to control end point)
- Supports 2 IN endpoints
- Supports control, interrupt and bulk transfers (does not support isochronous transfers)
- Supports a maximum packet size of 64 bytes
- Supports dedicated FIFOs per IN endpoint
 - Each Transmit FIFO is sized at 2 maximum sized packets
 - Each Transmit FIFO can be filled with minimum sized packets
- Supports a single FIFO for all OUT end points
 - The receive FIFO is sized at 2 maximum sized packets
 - The receive FIFO can be filled with minimum sized packets



15.3 Memory Mapped IO Registers

15.3.1 USB Controller Register Summary

MEM BaseAddress: 0xB0500000

Table 98. USB Controller Register Summary

MEM Address	Default	Instance Name	Name
0x000	0019_0000h	GOTGCTL	GOTGCTL
0x004	0000_0000h	GOTGIN	GOTGIN
0x008	0000_0000h	GAHBCFG	GAHBCFG
0x00C	0000_1440h	GUSBCFG	GUSBCFG
0x010	0000_0000h	GRSTCTL	GRSTCTL
0x014	0000_0000h	GINTSTS	GINTSTS
0x018	0000_0000h	GINTMSK	GINTMSK
0x01C	0000_0000h	GRXSTSR	GRXSTSR
0x020	0000_0000h	GRXSTSP	GRXSTSP
0x024	0000_003Ah	GRXFSIZ	GRXFSIZ
0x028	0022_0022h	GNPTXFSIZ	GNPTXFSIZ
0x040	4F54_310Ah	GSNPSID	GSNPSID
0x044	0000_0500h	GHWCFG1	GHWCFG1
0x048	2280_D514h	GHWCFG2	GHWCFG2
0x04C	0124_0468h	GHWCFG3	GHWCFG3
0x050	1600_8020h	GHWCFG4	GHWCFG4
0x054	0124_012Eh	GDFIFOCFG	GDFIFOCFG
0x104	0022_005Ch	DIEPTXF1	DIEPTXF1
0x108	0022_007Eh	DIEPTXF2	DIEPTXF2
0x10C	0022_00A0h	DIEPTXF3	DIEPTXF3
0x110	0022_00C2h	DIEPTXF4	DIEPTXF4
0x114	0022_00E4h	DIEPTXF5	DIEPTXF5
0x800	0800_0000h	DCFG	DCFG
0x804	0000_0002h	DCTL	DCTL
0x808	0000_0002h	DSTS	DSTS
0x810	0000_0000h	DIEPMSK	DIEPMSK
0x814	0000_0000h	DOEPMSK	DOEPMSK
0x818	0000_0000h	DAINT	DAINT



MEM Address	Default	Instance Name	Name
0x81C	0000_0000h	DAINTMSK	DAINTMSK
0x828	0000_17D7h	DVBUSDIS	DVBUSDIS
0x82C	0000_05B8h	DVBUSPULSE	DVBUSPULSE
0x830	0810_0010h	DTHRCTL	DTHRCTL
0x834	0000_0000h	DIEPEMPMSK	DIEPEMPMSK
0x900	0000_8000h	DIEPCTL0	DIEPCTL0
0x908	0000_0080h	DIEPINT0	DIEPINT0
0x910	0000_0000h	DIEPTSIZE0	DIEPTSIZE0
0x914	0000_0000h	DIEPDMA0	DIEPDMA0
0x918	0000_0022h	DTXFSTS0	DTXFSTS0
0x928	0000_0080h	DIEPINT1	DIEPINT1
0x920	0000_8000h	DIEPCTL1	DIEPCTL1
0x930	0000_0000h	DIEPTSIZE1	DIEPTSIZE1
0x934	0000_0000h	DIEPDMA1	DIEPDMA1
0x938	0000_0022h	DTXFSTS1	DTXFSTS1
0x940	0000_8000h	DIEPCTL2	DIEPCTL2
0x948	0000_0080h	DIEPINT2	DIEPINT2
0x950	0000_0000h	DIEPTSIZE2	DIEPTSIZE2
0x954	0000_0000h	DIEPDMA2	DIEPDMA2
0x958	0000_0022h	DTXFSTS2	DTXFSTS2
0x960	0000_8000h	DIEPCTL3	DIEPCTL3
0x968	0000_0080h	DIEPINT3	DIEPINT3
0x970	0000_0000h	DIEPTSIZE3	DIEPTSIZE3
0x974	0000_0000h	DIEPDMA3	DIEPDMA3
0x978	0000_0022h	DTXFSTS3	DTXFSTS2
0x994	0000_0000h	DIEPDMA4	DIEPDMA4
0x988	0000_0080h	DIEPINT4	DIEPINT4
0x980	0000_8000h	DIEPCTL4	DIEPCTL4
0x990	0000_0000h	DIEPTSIZE4	DIEPTSIZE4
0x998	0000_0022h	DTXFSTS4	DTXFSTS4
0x9A0	0000_8000h	DIEPCTL5	DIEPCTL5
0x9A8	0000_0080h	DIEPINT5	DIEPINT5
0x9B4	0000_0000h	DIEPDMA5	DIEPDMA5
0x9B0	0000_0000h	DIEPTSIZE5	DIEPTSIZE5



MEM Address	Default	Instance Name	Name
0x9B8	0000_0022h	DTXFSTS5	DTXFSTS5
0xB00	0000_8000h	DOEPCTL0	DOEPCTL0
0xB08	0000_0000h	DOEPINT0	DOEPINT0
0xB10	0000_0000h	DOEPTSIZE0	DOEPTSIZE0
0xB14	0000_0000h	DOEPDMA0	DOEPDMA0
0xB28	0000_0000h	DOEPINT1	DOEPINT1
0xB20	0000_0000h	DOEPCTL1	DOEPCTL1
0xB30	0000_0000h	DOEPTSIZE1	DOEPTSIZE1
0xB34	0000_0000h	DOEPDMA1	DOEPDMA1
0xB40	0000_0000h	DOEPCTL2	DOEPCTL2
0xB48	0000_0000h	DOEPINT2	DOEPINT2
0xB50	0000_0000h	DOEPTSIZE2	DOEPTSIZE2
0xB54	0000_0000h	DOEPDMA2	DOEPDMA2
0xB60	0000_0000h	DOEPCTL3	DOEPCTL3
0xB68	0000_0000h	DOEPINT3	DOEPINT3
0xB74	0000_0000h	DOEPDMA3	DOEPDMA3
0xB70	0000_0000h	DOEPTSIZE3	DOEPTSIZE3
0xE00	0000_0000h	PCGCCTL	PCGCCTL

15.3.2 USB Controller Register Detailed Description

GOTGCTL

OTG Control register

MEM Offset (B0050000)	000h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0019_0000h

Table 99. Detailed Description of GOTGCTL

Bits	Access Type	Default	Description
31:22	RO	10'h0	RSV_3 (RSV_3) Reserved



Bits	Access Type	Default	Description
21	RO	1'h0	Current Mode of Operation (CUR_MOD) Mode: Host and Device Indicates the current mode. 1'b0: Device mode 1'b1: Host mode
20	RW	1'h1	OTG Version (OTG_VER) OTG Version Indicates the OTG revision. 1'b0: OTG Version 1.3. In this version the core supports Data line pulsing and VBus pulsing for SRP. 1'b1: OTG Version 2.0. In this version the core supports only Data line pulsing for SRP.
19	RO	1'h1	B-Session Valid (BSESVALD) Mode: Device only B-Session Valid Indicates the Device mode transceiver status. 1'b0: B-session is not valid. 1'b1: B-session is valid. In OTG mode, you can use this bit to determine IF the device is connected or disconnected. Note: If you do not enabled OTG features (such as SRP and HNP), the read reset value will be 1. The vbus assigns the values internally for non- SRP or non-HNP configurations.
18:17	RO	2'h0	RSV_2 (RSV_2) Reserved
16	RO	1'h1	Connector ID Status (CON_ID_STS) Mode: Host and Device Indicates the connector ID status on a connect event. 1'b0: The DWC_otg core is in A-Device mode 1'b1: The DWC_otg core is in B-Device mode
15:8	RO	8'h0	RSV_1 (RSV_1) Reserved
7	RW	1'h0	B-Peripheral Session Valid OverrideValue (BVAL_OV_VAL) B-Peripheral Session Valid OverrideValue This bit is used to set Override value for Bvalid signal when GOTGCTL.BvalidOvEn is set. 1'b0 : Bvalid value is 1'b0 when GOTGCTL.BvalidOvEn =1 1'b1 : Bvalid value is 1'b1 when GOTGCTL.BvalidOvEn =1



Bits	Access Type	Default	Description
6	RW	1'h0	B-Peripheral Session Valid Override Enable (BVALID_OV_EN) B-Peripheral Session Valid Override Enable This bit is used to enable/disable the software to override the Bvalid signal using the GOTGCTL.BVALID_OV_VAL. 1'b1 : Internally Bvalid received from the PHY is overridden with GOTGCTL.BVALID_OV_VAL. 1'b0 : Override is disabled and bvalid signal from the respective PHY selected is used internally by the force
5:0	RO	6'h0	RSV (RSV) Reserved

GOTGINT

OTG Interrupt Register

MEM Offset (B0050000)	004h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 100. Detailed Description of GOTGINT

Bits	Access Type	Default	Description
31:19	RO	13'h0	RSV_3 (RSV_3) Reserved
18	RW/1C	1'h0	A-Device Timeout Change (ADEV_TOUT_CHG) Mode: Host and Device The core sets this bit to indicate that the A-device has timed out WHILE waiting FOR the B-device to connect. This bit can be set only by the core and the application should write 1 to clear it.
17	RW/1C	1'h0	Host Negotiation Detected (HST_NEG_DET) Mode: Host and Device The core sets this bit when it detects a host negotiation request on the USB. This bit can be set only by the core and the application should write 1 to clear it.
16:10	RO	7'h0	RSV_2 (RSV_2) Reserved



Bits	Access Type	Default	Description
9	RW/1C	1'h0	Host Negotiation Success Status Change (HST_NEG_SUC_STS_CHNG) The core sets this bit on the success or failure of a USB host negotiation request. The application must read the Host Negotiation Success bit of the OTG Control and Status register (GOTGCTL.HST_NEG_SCS) to check for success or failure. This bit can be set only by the core and the application should write 1 to clear it.
8	RW/1C	1'h0	Session Request Success Status Change (SES_REQ_SUC_STS_CHNG) The core sets this bit on the success or failure of a session request. The application must read the Session Request Success bit in the OTG Control and Status register (GOTGCTL.SES_REQ_SCS) to check For success or failure. This bit can be set only by the core and the application should write 1 to clear it. The core sets this bit when the utmiotg_bvalid signal is deasserted. This bit can be set only by the core and the application should write 1 to clear it.
7:3	RO	5'h0	RSV_1 (RSV_1) Reserved
2	RW/1C	1'h0	Session End Detected (SES_END_DET) The core sets this bit when the utmiotg_bvalid signal is deasserted. This bit can be set only by the core and the application should write 1 to clear it.
1:0	RO	2'h0	RSV (RSV) Reserved

GAHBCFG

AHB Configuration Register

MEM Offset (B0050000)	008h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 101. Detailed Description of GAHBCFG

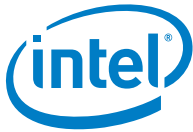
Bits	Access Type	Default	Description
31:24	RW	8'h0	RSV_3 (RSV_3) Reserved



Bits	Access Type	Default	Description
23	RW	1'h0	AHB Single Support (AHB_SINGLE) AHB Single Support This bit when programmed supports Single transfers for the remaining data in a transfer when the DWC_otg core is operating in DMA mode. 1'b0: This is the default mode. When this bit is set to 1'b0, the remaining data in the transfer is sent using INCR burst size. 1'b1: When set to 1'b1, the remaining data in a transfer is sent using Single burst size. Note: if this feature is enabled, the AHB RETRY and SPLIT transfers still have INCR burst type. Enable this feature when the AHB Slave connected to the DWC_otg core does not support INCR burst (and when Split, and Retry transactions are not being used in the bus).
22	RW	1'h0	Notify All Dma Write Transactions (NOTI_ALL_DMA_WRIT) Notify All Dma Write Transactions This bit is programmed to enable the System DMA Done functionality for all the DMA write Transactions corresponding to the Channel/Endpoint. This bit is valid only when GAHBCFG.REM_MEM_SUPP is set to 1. GAHBCFG.NOTI_ALL_DMA_WRIT = 1 - HSOTG core asserts int_dma_req for all the DMA write transactions on the AHB interface along with int_dma_done, chep_last_transact and chep_number signal information. The core waits for sys_dma_done signal for all the DMA write transactions in order to complete the transfer of a particular Channel/Endpoint. GAHBCFG.NOTIALLDMAWRIT = 0 - HSOTG core asserts int_dma_req signal only for the last transaction of DMA write transfer corresponding to a particular Channel/Endpoint. Similarly, the core waits for sys_dma_done signal only for that transaction of DMA write to complete the transfer of a particular Channel/Endpoint.
21	RW	1'h0	Remote Memory Support (REM_MEM_SUPP) This bit is programmed to enable the functionality to wait for the system DMA Done Signal for the DMA Write Transfers. GAHBCFG.REM_MEM_SUPP=1 - The int_dma_req output signal is asserted when HSOTG DMA starts write transfer to the external memory. When the core is done with the Transfers it asserts int_dma_done signal to flag the completion of DMA writes from HSOTG. The core then waits for sys_dma_done signal from the system to proceed further and complete the Data Transfer corresponding to a particular Channel/Endpoint. GAHBCFG.REM_MEM_SUPP=0 - The int_dma_req and int_dma_done signals are not asserted and the core proceeds with the assertion of the XferComp interrupt as soon as the DMA write transfer is done at the HSOTG Core Boundary and it doesn't wait for the sys_dma_done signal to complete the DATA transfers
20:8	RO	13'h0	RSV_2 (RSV_2) Reserved



Bits	Access Type	Default	Description
7	RW	1'h0	Non-Periodic TxFIFO Empty Level (NPTXFE_EMP_LVL) Mode: Host and device Non-Periodic TxFIFO Empty Level This bit is used only in Slave mode. In host mode and with Shared FIFO with device mode, this bit indicates when the Non-Periodic TxFIFO Empty Interrupt bit in the Core Interrupt register (GINTSTS.NP_TX_FEMP) is triggered. With dedicated FIFO in device mode, this bit indicates when IN endpoint Transmit FIFO empty interrupt (DIEPINTn.TX_FEMP) is triggered. Host mode and with Shared FIFO with device mode:- 1'b0: GINTSTS.NP_TX_FEMP interrupt indicates that the Non- Periodic TxFIFO is half empty 1'b1: GINTSTS.NP_TX_FEMP interrupt indicates that the Non- Periodic TxFIFO is completely empty Dedicated FIFO in device mode :- 1'b0: DIEPINTn.TX_FEMP interrupt indicates that the IN Endpoint TxFIFO is half empty 1'b1: DIEPINTn.TX_FEMP interrupt indicates that the IN Endpoint TxFIFO is completely empty
6	RO	1'h0	RSV_1 (RSV_1) Reserved
5	RW	1'h0	DMA Enable (DMA_EN) Mode: Host and device DMA Enable 1'b0: Core operates in Slave mode 1'b1: Core operates in a DMA mode This bit is always 0 when Slave-Only mode has been selected
4:3	RO	2'h0	RSV (RSV) Reserved
2	RO	1'h0	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
1	RW	1'h0	Burst Length/Type (HBST_LEN) Mode: Host and device Burst Length/Type This field is used in both External and Internal DMA modes. In External DMA mode, these bits appear on dma_burst[3:0] ports, which can be used by an external wrapper to interface the External DMA Controller interface to DW_ahb_dmac or ARM PrimeCell. External DMA Mode defines the DMA burst length in terms of 32-bit words: 4'b0000: 1 word 4'b0001: 4 words 4'b0010: 8 words 4'b0011: 16 words 4'b0100: 32 words 4'b0101: 64 words 4'b0110: 128 words 4'b0111: 256 words Others: Reserved Internal DMA ModeAHB Master burst type: 4'b0000 Single 4'b0001 INCR 4'b0011 INCR4 4'b0101 INCR8 4'b0111 INCR16 Others: Reserved
0	RW	1'h0	Global Interrupt Mask (GLB_INTR_MASK) Mode: Host and device Global Interrupt Mask The application uses this bit to mask or unmask the interrupt line assertion to itself. Irrespective of this bit's setting, the interrupt status registers are updated by the core. 1'b0: Mask the interrupt assertion to the application. 1'b1: Unmask the interrupt assertion to the application.

GUSBCFG

USB Configuration Register

MEM Offset (B0050000)	00Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_1440h



Table 102 Detailed Description of GUSB_CFG

Bits	Access Type	Default	Description
31	WO	1'h0	Corrupt Tx packet (CORRUPT_TX_PKT) Mode: Host and device Corrupt Tx packet This bit is for debug purposes only. Never Set this bit to 1. The application should always write 1'b0 to this bit.
30:29	RO	2'h0	RSV_5 (RSV_5) Reserved
28	RW	1'h0	Tx End Delay (TX_END_DELAY) Mode: Device only Tx End Delay Writing 1'b1 to this bit enables the core to follow the TxEndDelay timings as per UTMI+ specification 1.05 section 4.1.5 for opmode signal during remote wakeup. 1'b0 : Normal Mode. 1'b1 : Tx End delay.
27	RO	1'h0	RSV_4 (RSV_4) Reserved
26	RO	1'h0	IC_USB-Capable (IC_USB_CAP) The application uses this bit to control the DWC_otg core's Interchip USB capabilities. 1'b0: IC_USB PHY Interface is not selected. 1'b1: IC_USB PHY Interface is selected. This bit is writeable only if IC_USB is selected
25:23	RO	3'h0	RSV_3 (RSV_3) Reserved
22	RW	1'h0	TermSel DLine Pulsing Selection (TERM_SEL_DL_PULSE) Mode: Device only TermSel DLine Pulsing Selection This bit selects utmi_termselect to drive data line pulse during SRP. 1'b0: Data line pulsing using utmi_txvalid (Default). 1'b1: Data line pulsing using utmi_termsel.
21:14	RO	8'h0	RSV_2 (RSV_2) Reserved



Bits	Access Type	Default	Description
13:10	RW	4'h5	USB Turnaround Time (USB_TRD_TRIM) Mode: Device only USB Turnaround Time Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIFO (SPRAM). This must be programmed to 4'h5: When the MAC interface is 16-bit UTMI+. 4'h9: When the MAC interface is 8-bit UTMI+. Note: The values above are calculated for the minimum AHB frequency of 30 MHz. USB turnaround time is critical for certification where long cables and 5-Hubs are used, so If you need the AHB to run at less than 30 MHz, and If USB turnaround time is not critical, these bits can be programmed to a larger value.
9:7	RO	3'h0	RSV_1 (RSV_1) Reserved
6	RO	1'h1	USB 1.1 Full-Speed Serial Transceiver Select (PHYSEL) Mode: Host and Device USB 2.0 High-Speed PHY or USB 1.1 Full-Speed Serial Transceiver Select The application uses this bit to select either a high-speed UTMI+ or ULPI PHY, or a full-speed transceiver. 1'b0: USB 2.0 high-speed UTMI+ or ULPI PHY 1'b1: USB 1.1 full-speed serial transceiver If a USB 1.1 Full-Speed Serial Transceiver interface was not selected in, this bit is always 0, with Write Only access. If a high-speed PHY interface was not selected in, this bit is always 1, with Write Only access. If both interface types were selected (parameters have non-zero values), the application uses this bit to select which interface is active, and access is Read and Write.
5	RW	1'h0	Full-Speed Serial Interface Select (FS_INTF) Mode: Host and Device Full-Speed Serial Interface Select The application uses this bit to select either a unidirectional or bidirectional USB 1.1 full-speed serial transceiver interface. 1'b0: 6-pin unidirectional full-speed serial interface 1'b1: 3-pin bidirectional full-speed serial interface If a USB 1.1 Full-Speed Serial Transceiver interface was not selected, this bit is always 0, with Write Only access. If a USB 1.1 FS interface was selected, Then the application can Set this bit to select between the 3- and 6-pin interfaces, and access is Read and Write.
4	RO	1'h0	RSV (RSV) Reserved



Bits	Access Type	Default	Description
3	RW	1'h0	PHY Interface (PHY_IF) Mode: Host and Device PHY Interface The application uses this bit to configure the core To support a UTMI+ PHY with an 8- or 16-bit interface. When a ULPI PHY is chosen, this must be Set to 8-bit mode. 1'b0: 8 bits 1'b1: 16 bits This bit is writable only If UTMI+ and ULPI were selected.
2:0	RW	3'h0	HS/FS Timeout Calibration (TOUT_CAL) Mode: Host and Device HS/FS Timeout Calibration The number of PHY clocks that the application programs in this field is added to the high-speed/full-speed interpacket timeout duration in the core to account for any additional delays introduced by the PHY. This can be required, because the delay introduced by the PHY in generating the linestate condition can vary from one PHY to another. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value for full-speed operation is 16 to 18 (inclusive) bit times. The application must program this field based on the speed of enumeration. The number of bit times added per PHY clock are: High-speed operation: One 30-MHz PHY clock = 16 bit times One 60-MHz PHY clock = 8 bit times Full-speed operation: One 30-MHz PHY clock = 0.4 bit times One 60-MHz PHY clock = 0.2 bit times One 48-MHz PHY clock = 0.25 bit times

GRSTCTL

Reset Register

MEM Offset (B0050000)	010h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 103. Detailed Description of GRSTCTL

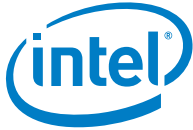
Bits	Access Type	Default	Description
31	RO	1'h0	AHB Master Idle (AHB_IDLE) Indicates that the AHB Master State Machine is in the IDLE condition.



Bits	Access Type	Default	Description
30	RO	1'h0	DMA Request Signal (DMA_REQ) Indicates that the DMA request is in progress. Used For debug.
29:11	RO	19'h0	RSV_1 (RSV_1) Reserved
10:6	RW	5'h0	TxFIFO Flush (TX_FNUM) Mode: Host and Device This is the FIFO number that must be flushed using the TxFIFO Flush bit. This field must not be changed until the core clears the TxFIFO Flush bit. 5'h0: - Non-periodic TxFIFO flush in Host mode - Non-periodic TxFIFO flush in device mode when in shared FIFO operation - Tx FIFO 0 flush in device mode when in dedicated FIFO mode 5'h1: - Periodic TxFIFO flush in Host mode - Periodic TxFIFO 1 flush in Device mode when in shared FIFO operation - TxFIFO 1 flush in device mode when in dedicated FIFO mode 5'h2: - Periodic TxFIFO 2 flush in Device mode when in shared FIFO operation - TxFIFO 2 flush in device mode when in dedicated FIFO mode ... 5'hF: - Periodic TxFIFO 15 flush in Device mode when in shared FIFO operation - TxFIFO 15 flush in device mode when in dedicated FIFO mode 5'h10: Flush all the transmit FIFOs in device or host mode..
5	RW/1S/V	1'h0	TxFIFO Flush (TX_FFLSH) Mode: Host and Device This bit selectively flushes a single or all transmit FIFOs, but cannot do so If the core is in the midst of a transaction. The application must write this bit only after checking that the core is neither writing to the TxFIFO nor reading from the TxFIFO. Verify using these registers: Read - NAK Effective Interrupt ensures the core is not reading from the FIFO Write - GRSTCTL.AHB_IDLE ensures the core is not writing anything to the FIFO. Flushing is normally recommended when FIFOs are reconfigured or when switching between Shared FIFO and Dedicated Transmit FIFO operation. FIFO flushing is also recommended during device endpoint disable. The application must wait until the core clears this bit before performing any operations. This bit takes eight clocks to clear, using the slower clock of phy_clk or hclk.



Bits	Access Type	Default	Description
4	RW/1S/V	1'h0	RxFIFO Flush (RX_FFLSH) Mode: Host and Device The application can flush the entire RxFIFO using this bit, but must first ensure that the core is not in the middle of a transaction. The application must only write to this bit after checking that the core is neither reading from the RxFIFO nor writing to the RxFIFO. The application must wait until the bit is cleared before performing any other operations. This bit requires 8 clocks (slowest of PHY or AHB clock) to clear.
3:2	RO	2'h0	RSV (RSV) Reserved
1	RW/1S/V	1'h0	PIU FS Dedicated Controller Soft Reset (PIU_FS_SFT_RST) Mode: Host and Device Resets the PIU FS Dedicated ControllerAll module state machines in FS Dedicated Controller of PIU are reset to the IDLE state. Used to reset the FS Dedicated controller in PIU in case of any PHY Errors like Loss of activity or Babble Error resulting in the PHY remaining in RX state for more than one frame boundary.



0	RW/1S/V	1'h0	Core Soft Reset (C_SFT_RST) Mode: Host and device Resets the hclk and phy_clock domains as follows: Clears the interrupts and all the CSR registers except the following register bits: - PCGCCTL.RSTPDWNMODULE - PCGCCTL.GATEHCLK - PCGCCTL.PWRCLMP - PCGCCTL.STOPPPHYLPWRCLKSELCLK - GUSBCFG.PHYLPWRCLKSEL - GUSBCFG.DDRSEL - GUSBCFG.PHYSEL - GUSBCFG.FSINTF - GUSBCFG.ULPI_UTMI_SEL - GUSBCFG.PHYIF - GUSBCFG.TXENDDELAY - GUSBCFG.TERMSELDLPULSE - GUSBCFG.ULPICKSUSM - GUSBCFG.ULPIAUTORES - GUSBCFG.ULPIFSL - GGPI0 - GPWRDN - GADPCTL - DCFG.DEVS_PD - DCTL.SFT_DIS_CON - All module state machines All module state machines (except the AHB Slave Unit) are reset to the IDLE state, and all the transmit FIFOs and the receive FIFO are flushed. Any transactions on the AHB Master are terminated as soon as possible, after gracefully completing the last data phase of an AHB transfer. Any transactions on the USB are terminated immediately. When Hibernation or ADP feature is enabled, the PMU module is not reset by the Core Soft Reset. The application can write to this bit any time it wants to reset the core. This is a self-clearing bit and the core clears this bit after all the necessary logic is reset in the core, which can take several clocks, depending on the current state of the core. Once this bit is cleared software must wait at least 3 PHY clocks before doing any access to the PHY domain (synchronization delay). Software must also must check that bit 31 of this register is 1 (AHB Master is IDLE) before starting any operation. Typically software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock For the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain has to be reset for proper operation. The core sets this bit when the utmiotg_bvalid signal is deasserted. This bit can be set only by the core and the application should write 1 to clear it.



GINTSTS

Interrupt Status Register

MEM Offset (B0050000)	014h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 104. Detailed Description of GINTSTS

Bits	Access Type	Default	Description
31	RW/1C	1'h0	Resume/Remote Wakeup Detected Interrupt (WK_UP_INT) Wakeup Interrupt during Suspend(L2) or LPM(L1) state. During Suspend(L2): - Device Mode - This interrupt is asserted only when Host Initiated Resume is detected on USB. - Host Mode - This interrupt is asserted only when Device Initiated Remote Wakeup is detected on USB. For more information, see 'Partial Power-Down and Clock Gating Programming Model'. During LPM(L1):- - Device Mode - This interrupt is asserted for either Host Initiated Resume or Device Initiated Remote Wakeup on USB. - Host Mode - This interrupt is asserted for either Host Initiated Resume or Device Initiated Remote Wakeup on USB. For more information, see 'LPM Entry and Exit Programming Model'
30	RW/1C/V	1'h0	Session Request/New Session Detected Interrupt (SESS_REQ_INT) Mode: Host and Device In Host mode, this interrupt is asserted when a session request is detected from the device. In Host mode, this interrupt is asserted when a session request is detected from the device. In Device mode, this interrupt is asserted when the utmisrp_bvalid signal goes high. For more information on how to use this interrupt, see 'Partial Power-Down and Clock Gating Programming Model'
29	RO	1'h0	RSV_4 (RSV_4) Reserved
28	RW/1C/V	1'h0	Connector ID Status Change (CON_IDSTS_CHG) Mode: Host and Device The core sets this bit when there is a change in connector ID status.
27	RO	1'h0	RSVD (RSVD) Reserved
26:24	RO	3'h0	RSV_3 (RSV_3) Reserved



Bits	Access Type	Default	Description
23	RW/1C	1'h0	Reset detected Interrupt (RESET_DET) In Device mode, this interrupt is asserted when a reset is detected on the USB in partial power-down mode when the device is in Suspend. In Host mode, this interrupt is not asserted.
22	RW/1C	1'h0	Data Fetch Suspended (FET_SUSP) This interrupt is valid only in DMA mode. This interrupt indicates that the core has stopped fetching data For IN endpoints due to the unavailability of TxFIFO space or Request Queue space. This interrupt is used by the application for an endpoint mismatch algorithm. For example, after detecting an endpoint mismatch, the application: Sets a Global non-periodic IN NAK handshake Disables In endpoints Flushes the FIFO Determines the token sequence from the IN Token Sequence Learning Queue Re-enables the endpoints Clears the Global non-periodic IN NAK handshake If the Global non-periodic IN NAK is cleared, the core has not yet fetched data for the IN endpoint, and the IN token is received. The core generates an 'IN token received when FIFO empty' interrupt. The OTG Then sends the host a NAK response. To avoid this scenario, the application can check the GINTSTS.FET_SUSP interrupt, which ensures that the FIFO is full before clearing a Global NAK handshake. Alternatively, the application can mask the IN token received when FIFO empty interrupt when clearing a Global IN NAK handshake.
21	RW/1C	1'h0	Incomplete Isochronous OUT Transfer (INCOMP_IP) In Host mode, the core sets this interrupt bit when there are incomplete periodic transactions still pending which are scheduled For the current microframe. In Device mode, the core sets this interrupt to indicate that there is at least one isochronous OUT endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register.
20	RW/1C	1'h0	Incomplete Isochronous IN Transfer (INCOMPL_SOIN) The core sets this interrupt to indicate that there is at least one isochronous IN endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register. Note: This interrupt is not asserted in Scatter/Gather DMA mode.



Bits	Access Type	Default	Description
19	RO	1'h0	OUT Endpoints Interrupt (OEP_INT) The core sets this bit to indicate that an interrupt is pending on one of the OUT endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the OUT endpoint on which the interrupt occurred, and then read the corresponding Device OUT Endpoint-n Interrupt (DOEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DOEPINTn register to clear this bit.
18	RO	1'h0	IN Endpoints Interrupt (IEP_INT) The core sets this bit to indicate that an interrupt is pending on one of the IN endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the IN endpoint on Device IN Endpoint-n Interrupt (DIEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DIEPINTn register to clear this bit.
17	RW/1C	1'h0	Endpoint Mismatch Interrupt (EP_MIS) Mode: Device only Note: This interrupt is valid only in shared FIFO operation. Indicates that an IN token has been received for a non-periodic endpoint, but the data for another endpoint is present in the top of the Non-periodic Transmit FIFO and the IN endpoint mismatch count programmed by the application has expired.
16	RO	1'h0	RSV_2 (RSV_2) Reserved
15	RW/1C	1'h0	End of Periodic Frame Interrupt (EOPF) Indicates that the period specified in the Periodic Frame Interval field of the Device Configuration register (DCFG.PER_FR_INT) has been reached in the current microframe.
14	RW/1C	1'h0	Isochronous OUT Packet Dropped Interrupt (ISO_OUT_DROP) Mode: Device only The core sets this bit when it fails to write an isochronous OUT packet into the RxFIFO because the RxFIFO does not have enough space to accommodate a maximum packet size packet for the isochronous OUT endpoint.
13	RW/1C	1'h0	Enumeration Done (ENUM_DONE) Mode: Device only The core sets this bit to indicate that speed enumeration is complete. The application must read the Device Status (DSTS) register to obtain the enumerated speed.
12	RW/1C	1'h0	USB Reset (USB_RST) The core sets this bit to indicate that a reset is detected on the USB.
11	RW/1C	1'h0	USB Suspend (USB_SUSP) The core sets this bit to indicate that a suspend was detected on the USB. The core enters the Suspended state when there is no activity on the linestate signal For an extended period of time.



Bits	Access Type	Default	Description
10	RW/1C	1'h0	Early Suspend (ERLY_SUSP) Mode: Device only The core sets this bit to indicate that an Idle state has been detected on the USB For 3 ms.
9:8	RO	2'h0	RSV_1 (RSV_1) Reserved
7	RO	1'h0	Global OUT NAK Effective (GOUT_NAK_EFF) Mode: Device only Indicates that the Set Global OUT NAK bit in the Device Control register (DCTL.SG_OUT_NAK), Set by the application, has taken effect in the core. This bit can be cleared by writing the Clear Global OUT NAK bit in the Device Control register (DCTL.CG_OUT_NAK).
6	RO	1'h0	Global IN Non-periodic NAK Effective (GIN_NAK_EFF) Mode: Device only Indicates that the Set Global Non-periodic IN NAK bit in the Device Control register (DCTL.SG_NPIN_NAK), set by the application, has taken effect in the core. That is, the core has sampled the Global IN NAK bit Set by the application. This bit can be cleared by clearing the Clear Global Non-periodic IN NAK bit in the Device Control register (DCTL.CG_NPIN_NAK). This interrupt does not necessarily mean that a NAK handshake is sent out on the USB. The STALL bit takes precedence over the NAK bit.
5	RO	1'h0	RSV (RSV)
4	RO	1'h0	RxFIFO Non-Empty (RX_FLVL) Mode: Host and Device Indicates that there is at least one packet pending to be read from the RxFIFO.
3	RW/1C	1'h0	Start of (micro) Frame (SOF) Mode: Host and Device In Host mode, the core sets this bit to indicate that an SOF (FS), micro-SOF (HS), or Keep-Alive (LS) is transmitted on the USB. The application must write a 1 to this bit to clear the interrupt. In Device mode, in the core sets this bit to indicate that an SOF token has been received on the USB. The application can read the Device Status register to get the current (micro) Frame number. This interrupt is seen only when the core is operating at either HS or FS. Note: This register may return 1b1 if read immediately after power on reset. If the register bit reads 1b1 immediately after power on reset it does not indicate that an SOF has been sent (in case of host mode) or SOF has been received (in case of device mode). The read value of this interrupt is valid only after a valid connection between host and device is established. If the bit is set after power on reset the application can clear the bit.



Bits	Access Type	Default	Description
2	RO	1'h0	OTG Interrupt (OTG_INT) The core sets this bit to indicate an OTG protocol event. The application must read the OTG Interrupt Status (GOTGINT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the GOTGINT register to clear this bit.
1	RW/1C	1'h0	Mode Mismatch Interrupt (MODE_MIS) Mode: Host and Device The core sets this bit when the application is trying to access: - A Host mode register, when the core is operating in Device mode - A Device mode register, when the core is operating in Host mode The register access is completed on the AHB with an OKAY response, but is ignored by the core internally and does not affect the operation of the core. This bit can be set only by the core and the application should write 1 to clear it
0	RO	1'h0	Current Mode of Operation (CUR_MOD) Mode: Host and Device Indicates the current mode. 1'b0: Device mode 1'b1: Host mode

GINTMSK

Interrupt Mask Register

MEM Offset (B0050000)	018h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 105. Detailed Description of GINTMSK

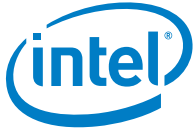
Bits	Access Type	Default	Description
31	RW	1'h0	Resume/Remote Wakeup Detected Interrupt Mask (WK_UP_INT_MSK) Mode: Host and Device Resume/Remote Wakeup Detected Interrupt Mask The WakeUp bit is used for LPM state wake up in a way similar to that of wake up in suspend state.
30	RW	1'h0	Session Request/New Session Detected Interrupt Mask (SESS_REQ_INT_MSK) Mode: Host and Device Session Request/New Session Detected Interrupt Mask



Bits	Access Type	Default	Description
29	RW	1'h0	Disconnect Detected Interrupt Mask (DISCONN_INT_MSK) Mode: Host and Device Disconnect Detected Interrupt Mask
28	RW	1'h0	Connector ID Status Change Mask (CON_ID_STS_CHG_MSK) Mode: Host and Device Connector ID Status Change Mask
27	RO	1'h0	RSVD (RSVD) Reserved
26:24	RO	3'h0	RSV_4 (RSV_4) Reserved
23	RW	1'h0	Reset detected Interrupt Mask (RESET_DET_MSK) Mode: Device only Reset detected Interrupt Mask
22	RW	1'h0	Data Fetch Suspended Mask (FET_SUSP_MSK) Mode: Device only Data Fetch Suspended Mask
21	RW	1'h0	Incomplete Isochronous OUT Transfer Interrupt Mask (INCOMPL_SOOUT_MSK) Mode: Device only Incomplete Isochronous OUT Transfer Interrupt Mask
20	RW	1'h0	Incomplete Isochronous IN Transfer Mask (INCOMPL_SOIN_MSK) Mode: Device only Incomplete Isochronous IN Transfer Mask
19	RW	1'h0	OUT Endpoints Interrupt Mask (OEP_INT_MSK) Mode: Device only OUT Endpoints Interrupt Mask
18	RW	1'h0	IN Endpoints Interrupt Mask (IEP_INT_MSK) Mode: Device only IN Endpoints Interrupt Mask
17	RW	1'h0	Endpoint Mismatch Interrupt Mask (EP_MIS_MSK) Mode: Device only Endpoint Mismatch Interrupt Mask
16	RO	1'h0	RSV_3 (RSV_3) Reserved
15	RW	1'h0	End of Periodic Frame Interrupt Mask (EOPF_MSK) Mode: Device only End of Periodic Frame Interrupt Mask



Bits	Access Type	Default	Description
14	RW	1'h0	Isochronous OUT Packet Dropped Interrupt Mask (ISO_OUT_DROP_MSK) Mode: Device only Isochronous OUT Packet Dropped Interrupt Mask
13	RW	1'h0	Enumeration Done Mask (ENUM_DONE_MSK) Mode: Device only Enumeration Done Mask
12	RW	1'h0	USB Reset Mask (USB_BRST_MSK) Mode: Device only USB Reset Mask
11	RW	1'h0	USB Suspend Mask (USB_SUSP_MSK) Mode: Device only USB Suspend Mask
10	RW	1'h0	Early Suspend Mask (ERLY_SUSP_MSK) Mode: Device only Early Suspend Mask
9:8	RO	2'h0	RSV_2 (RSV_2) Reserved
7	RW	1'h0	Global OUT NAK Effective Mask (GOUT_NAK_EFF_MSK) Device only Global OUT NAK Effective Mask
6	RW	1'h0	Global Non-periodic IN NAK Effective Mask (GIN_NAK_EFF_MSK) Mode: Device only Global Non-periodic IN NAK Effective Mask
5	RO	1'h0	RSV_1 (RSV_1) Reserved
4	RW	1'h0	Receive FIFO Non-Empty Mask (RX_FLVL_MSK) Mode: Host and Device Receive FIFO Non-Empty Mask
3	RW	1'h0	Start of (micro) Frame Mask (SOF_MSK) Mode: Host and Device Start of (micro) Frame Mask
2	RW	1'h0	OTG Interrupt Mask (OTG_INT_MSK) Mode: Host and Device OTG Interrupt Mask
1	RW	1'h0	Mode Mismatch Interrupt Mask (MODE_MIS_MSK) Mode: Host and Device Mode Mismatch Interrupt Mask
0	RO	1'h0	RSV (RSV) Reserved

**GRXSTSR**

Receive Status Read /Pop Register

MEM Offset (B0050000) 01Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 106. Detailed Description of GRXSTSR

Bits	Access Type	Default	Description
31:25	RO	7'h0	RSV (RSV_1) Reserved
24:21	RO	4'h0	Frame Number (FN) This is the least significant 4 bits of the (micro) Frame number in which the packet is received on the USB. This field is supported only when isochronous OUT endpoints are supported.
20:17	RO	4'h0	Packet Status (PKT_STS) Mode: Host only Indicates the status of the received packet 4'b0010: IN data packet received 4'b0011: IN transfer completed (triggers an interrupt) 4'b0101: Data toggle error (triggers an interrupt) 4'b0111: Channel halted (triggers an interrupt) Others: Reserved Mode: Device only Indicates the status of the received packet 4'b0001: Global OUT NAK (triggers an interrupt) 4'b0010: OUT data packet received 4'b0011: OUT transfer completed (triggers an interrupt) 4'b0100: SETUP transaction completed (triggers an interrupt) 4'b0110: SETUP data packet received Others: Reserved



Bits	Access Type	Default	Description
16:15	RO	2'h0	Data PID (DPID) Mode: Host only Indicates the Data PID of the received packet 2'b00: DATA0 2'b10: DATA1 2'b01: DATA2 2'b11: MDATA Mode: Device only Indicates the Data PID of the received OUT data packet 2'b00: DATA0 2'b10: DATA1 2'b01: DATA2 2'b11: MDATA
14:4	RO	11'h0	Byte Count (PKT_CNT) Mode: Host only Indicates the byte count of the received IN data packet. Mode: Device only Indicates the byte count of the received data packet.
3:0	RO	4'h0	Channel Number (EP_NUM) Mode: Host only Indicates the channel number to which the current received packet belongs. Mode: Device only Indicates the endpoint number to which the current received packet belongs.

GRXSTSP

Receive Status Read /Pop Register

MEM Offset (B0050000)	020h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 107. Detailed Description of GRXSTSP

Bits	Access Type	Default	Description
31:25	RO	7'h0	RSV (RSV_1) Reserved



Bits	Access Type	Default	Description
24:21	RO	4'h0	Frame Number (FN) This is the least significant 4 bits of the (micro)Frame number in which the packet is received on the USB. This field is supported only when isochronous OUT endpoints are supported.
20:17	RO	4'h0	Packet Status (PKT_STS) Mode: Host only Indicates the status of the received packet 4'b0010: IN data packet received 4'b0011: IN transfer completed (triggers an interrupt) 4'b0101: Data toggle error (triggers an interrupt) 4'b0111: Channel halted (triggers an interrupt) Others: Reserved Mode: Device only Indicates the status of the received packet 4'b0001: Global OUT NAK (triggers an interrupt) 4'b0010: OUT data packet received 4'b0011: OUT transfer completed (triggers an interrupt) 4'b0100: SETUP transaction completed (triggers an interrupt) 4'b0110: SETUP data packet received Others: Reserved
16:15	RO	2'h0	Data PID (DPID) Mode: Host only Indicates the Data PID of the received packet 2'b00: DATA0 2'b10: DATA1 2'b01: DATA2 2'b11: MDATA Mode: Device only Indicates the Data PID of the received OUT data packet 2'b00: DATA0 2'b10: DATA1 2'b01: DATA2 2'b11: MDATA
14:4	RO	11'h0	Byte Count (PKT_CNT) Mode: Host only Indicates the byte count of the received IN data packet. Mode: Device only Indicates the byte count of the received data packet.



Bits	Access Type	Default	Description
3:0	RO	4'h0	Channel Number (EP_NUM) Mode: Host only Indicates the channel number to which the current received packet belongs. Mode: Device only Indicates the endpoint number to which the current received packet belongs.

GRXFSIZ

Receive FIFO Size Register

MEM Offset (B0050000)	024h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_003Ah

Table 108. Detailed Description of GRXFSIZ

Bits	Access Type	Default	Description
31:6	RO	26'h0	RSV (RSV) Reserved
5:0	RO	6'h3A	AHB Master Idle (RX_FDEP) Mode: Host and Device This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 32,768 The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth during configuration. If Enable Dynamic FIFO Sizing was selected, you can write a new value in this field. Programmed values must not exceed the power-on value

GNPTXFSIZ

Non-periodic Transmit FIFO Size Register

MEM Offset (B0050000)	028h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0022_0022h



Table 109. Detailed Description of GNPTXFSIZ

Bits	Access Type	Default	Description
31:16	RO	16'h22	IN Endpoint Tx FIFO 0 Depth (IN_EP_TXF_0_DEP) Mode: Device only This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 32,768 This field is determined by Enable Dynamic FIFO Sizing Programmed values must not exceed the power-on value.
15:0	RO	16'h22	IN Endpoint FIFO0 Transmit RAM Start Address (IN_EP_TXF_0_ST_ADDR) Mode: Device only This field contains the memory start address For IN Endpoint Transmit FIFO Number 0. Programmed values must not exceed the power-on value.

GSNPSID

ID Register

MEM Offset (B0050000)	040h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	4F54_310Ah

Table 110. Detailed Description of GSNPSID

Bits	Access Type	Default	Description
31:0	RO	32'h4f54310a	ID Release number of the DWC_otg core being used.

GHWCFG1

Hardware configuration register 1

MEM Offset (B0050000)	044h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0500h



Table 111. Detailed Description of GHWCFG1

Bits	Access Type	Default	Description
31:0	RO	32'h500	Endpoint Direction (EPDIR) This 32-bit field uses two bits per endpoint to determine the endpoint direction. Bits [31:30]: Endpoint 15 direction Bits [29:28]: Endpoint 14 direction ... Bits [3:2]: Endpoint 1 direction Bits [1:0]: Endpoint 0 direction (always BIDIR) Direction 2'b00: BIDIR (IN and OUT) endpoint 2'b01: IN endpoint 2'b10: OUT endpoint 2'b11: Reserved

GHWCFG2

Hardware configuration register 2

MEM Offset (B0050000)	048h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	2280_D514h

Table 112. Detailed Description of GHWCFG2

Bits	Access Type	Default	Description
31	RO	1'b0	RSV (RSV) Reserved
30:26	RO	5'h08	Device Mode IN Token Sequence Learning Queue Depth (TKNQ_DEPTH) Device Mode IN Token Sequence Learning Queue Depth Range: 0-30
25:24	RO	2'h2	Host Mode Periodic Request Queue Depth (PTXQ_DEPTH) Host Mode Periodic Request Queue Depth 2'b00: 2 2'b01: 4 2'b10: 8 2'b11: 16



Bits	Access Type	Default	Description
23:22	RO	2'h2	Non-periodic Request Queue Depth (NPTXQ_DEPTH) Non-periodic Request Queue Depth 2'b00: 2 2'b01: 4 2'b10: 8 Others: Reserved
21	RO	1'h0	RSV_1 (RSV_1) Reserved
20	RO	1'h0	Multi Processor Interrupt Enabled (MULTI_PROC_INTRPT) Multi Processor Interrupt Enabled 1'b0: No 1'b1: Yes
19	RO	1'h0	Dynamic FIFO Sizing Enabled (DYN_FIFO_SIZING) Dynamic FIFO Sizing Enabled 1'b0: No 1'b1: Yes
18	RO	1'h0	Periodic OUT Channels Supported in Host Mode (PERIO_SUPPORT) Periodic OUT Channels Supported in Host Mode 1'b0: No 1'b1: Yes
17:14	RO	4'h3	Number of Host Channels (NUM_HST_CHNL) Number of Host Channels Indicates the number of host channels supported by the core in Host mode. The range of this field is 0-15: 0 specifies 1 channel, 15 specifies 16 channels.
13:10	RO	4'h5	Number of Device Endpoints (NUM_DEV_EPS) Number of Device Endpoints Indicates the number of device endpoints supported by the core in Device mode in addition to control endpoint 0. The range of this field is 1-15.
9:8	RO	2'h1	Full-Speed PHY Interface Type (FS_PHY_TYPE) Full-Speed PHY Interface Type 2'b00: Full-speed interface not supported 2'b01: Dedicated full-speed interface 2'b10: FS pins shared with UTMI+ pins 2'b11: FS pins shared with ULPI pins
7:6	RO	2'h0	High-Speed PHY Interface Type (HS_PHY_TYPE) High-Speed PHY Interface Type 2'b00: High-Speed interface not supported 2'b01: UTMI+ 2'b10: ULPI 2'b11: UTMI+ and ULPI



Bits	Access Type	Default	Description
5	RO	1'h0	Point-to-Point (SING_PNT) Point-to-Point 1'b0: Multi-point application (hub and split support) 1'b1: Single-point application (no hub and split support)
4:3	RO	2'h2	OTG Architecture (OTG_ARCH) Architecture 2'b00: Slave-Only 2'b01: External DMA 2'b10: Internal DMA Others: Reserved
2:0	RO	3'h4	Mode of Operation (OTG_MODE) Mode of Operation 3'b000: HNP- and SRP-Capable OTG (Host and Device) 3'b001: SRP-Capable OTG (Host and Device) 3'b010: Non-HNP and Non-SRP Capable OTG (Host and Device) 3'b011: SRP-Capable Device 3'b100: Non-OTG Device 3'b101: SRP-Capable Host 3'b110: Non-OTG Host Others: Reserved

GHWCFG3

Hardware configuration register 3

MEM Offset (B0050000)	04Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0124_0468h

Table 113. Detailed Description of GHWCFG3

Bits	Access Type	Default	Description
31:16	RO	16'h0124	DFIFO DEPTH (DFIFO_DEPTH) DFIFO Depth (DfifoDepth - EP_LOC_CNT) This value is in terms of 32-bit words. Minimum value is 32 Maximum value is 32,768
15	RO	1'h0	LPM mode (LPM_MODE) LPM mode specified for Mode of Operation.



Bits	Access Type	Default	Description
14	RO	1'h0	Battery Charger Support (BC_SUPPORT) This bit indicates the HS OTG controller support for Battery Charger. 0 - No Battery Charger Support 1 - Battery Charger support present.
13	RO	1'h0	HSIC Mode (HSIC_MODE) HSIC mode specified for Mode of Operation Value Range: 0 - 1 1: HSIC-capable with shared UTMI PHY interface 0: Non-HSIC-capable
12	RO	1'h0	ADP Support (ADP_SUPPORT) This bit indicates whether ADP logic is present within or external to the HS OTG controller 0: No ADP logic present with HSOTG controller 1: ADP logic is present along with HSOTG controller.
11	RO	1'h0	Reset Type (RST_TYPE) Reset style for clocked always blocks in RTL 1'b0: Asynchronous reset is used in the core 1'b1: Synchronous reset is used in the core
10	RO	1'h1	Optional Features Removed (OPT_FEATURE) Optional Features Removed Indicates whether the User ID register, GPIO interface ports, and SOF toggle and counter ports were removed for gate count optimization by enabling Remove Optional Features. 1'b0: No 1'b1: Yes
9	RO	1'h0	Vendor Control Interface Support (VND_CTL_SUPT) Vendor Control Interface Support 1'b0: Vendor Control Interface is not available on the core. 1'b1: Vendor Control Interface is available.
8	RO	1'h0	I2C Selection (I2C_INT_SEL) I2C Selection 1'b0: I2C Interface is not available on the core. 1'b1: I2C Interface is available on the core.
7	RO	1'h0	OTG Function Enabled (OTG_EN) OTG Function Enabled The application uses this bit to indicate the DWC_otg core's OTG capabilities. 1'b0: Not OTG capable 1'b1: OTG Capable



Bits	Access Type	Default	Description
6:4	RO	3'h6	Packet Size Counter Width (PKT_SIZE_WIDTH) Width of Packet Size Counters 3'b000: 4 bits 3'b001: 5 bits 3'b010: 6 bits 3'b011: 7 bits 3'b100: 8 bits 3'b101: 9 bits 3'b110: 10 bits Others: Reserved
3:0	RO	4'h8	Transfer Size Counter Width (XFER_SIZE_WIDTH) Width of Transfer Size Counters 4'b0000: 11 bits 4'b0001: 12 bits ... 4'b1000: 19 bits Others: Reserved

GHWCFG4

Hardware configuration register 4

MEM Offset (B0050000)	050h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	1600_8020h

Table 114. Detailed Description of GHWCFG4

Bits	Access Type	Default	Description
31	RO	1'h0	Scatter/Gather DMA configuration (DESC_DMA) Scatter/Gather DMA configuration 1'b0: Non Dynamic configuration 1'b1: Dynamic configuration
30	RO	1'h0	Scatter/Gather DMA configuration (DESC_DMA_ENABLED) Scatter/Gather DMA configuration 1'b0: Non-Scatter/Gather DMA configuration 1'b1: Scatter/Gather DMA configuration



Bits	Access Type	Default	Description
29:26	RO	4'h5	Number of Device Mode IN Endpoints (IN_EPS) Number of Device Mode IN Endpoints Including Control Endpoints Range 0 -15 0 : 1 IN Endpoint 1 : 2 IN Endpoints 15 : 16 IN Endpoints
25	RO	1'h1	Dedicated Transmit FIFO Mode (DED_FIFO_MODE) Enable Dedicated Transmit FIFO for device IN Endpoints 1'b0 : Dedicated Transmit FIFO Operation not enabled. 1'b1 : Dedicated Transmit FIFO Operation enabled.
24	RO	1'h0	Session End Filter Enabled (SESS_END_FLTR) Session End Filter Enabled 1'b0: No filter 1'b1: Filter
23	RO	1'h0	B valid Filter Enabled (BVALID_FLTR) B valid Filter Enabled 1'b0: No filter 1'b1: Filter
22	RO	1'h0	A valid Filter Enabled (AVALID_FLTR) A valid Filter Enabled 1'b0: No filter 1'b1: Filter
21	RO	1'h0	VBUS Valid Filter Enabled (VBUS_VALID_FLTR) VBUS Valid Filter Enabled 1'b0: No filter 1'b1: Filter
20	RO	1'h0	IDDIG Filter Enable (IDDGFLTR) IDDIG Filter Enable 1'b0: No filter 1'b1: Filter
19:16	RO	4'h0	Number of Device Mode Control Endpoints (NUM_CTL_EPS) Number of Device Mode Control Endpoints in Addition to Endpoint 0 Range: 0-15



Bits	Access Type	Default	Description
15:14	RO	2'h2	UTMI+ PHY/ULPI-to-Internal UTMI+ Wrapper Data Width (PHY_DATA_WIDTH) UTMI+ PHY/ULPI-to-Internal UTMI+ Wrapper Data Width When a ULPI PHY is used, an internal wrapper converts ULPI to UTMI+. 2'b00: 8 bits 2'b01: 16 bits 2'b10: 8/16 bits, software selectable Others: Reserved
13:8	RO	6'h0	RSV (RSV) Reserved
7	RO	1'h0	Extended Hibernation (EXTENDED_HIBERNATION) Number of Host Channels Indicates the number of host channels supported by the core in Host mode. The range of this field is 0-15: 0 specifies 1 channel, 15 specifies 16 channels.
6	RO	1'h0	Enable Hibernation (HIBERNATION) Enable Hibernation 1'b0: Hibernation feature not enabled 1'b1: Hibernation feature enabled
5	RO	1'h1	AHB Frequency (AHB_FREQ) Minimum AHB Frequency Less Than 60 MHz 1'b0: No 1'b1: Yes
4	RO	1'h0	Enable Partial Power Down (PARTIAL_PWR_DWN) Enable Partial Power Down 1'b0: Partial Power Down Not Enabled 1'b1: Partial Power Down Enabled
3:0	RO	4'h0	Number of Device Mode Periodic IN Endpoints (NUM_DEV_PERIO_EPS) Number of Device Mode Periodic IN Endpoints Range: 0-15

GDFIFOCFG

Global DFIFO Configuration Register

MEM Offset (B0050000)	054h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0124_012Eh



Table 115. Detailed Description of GDFIFOCFG

Bits	Access Type	Default	Description
31:16	RW	16'h0124	IN Endpoint TxFIFO 0 Depth (EP_INFO_BASE_ADDR) This field provides the start address of the EP info controller.
15:0	RW	16'h012e	IN Endpoint FIFO0 Transmit RAM Start Address (GD_FIFO_CFG) This field is for dynamic programming of the DFIFO Size. This value takes effect only when the application programs a non zero value to this register. The value programmed must conform to the guidelines described in 'FIFO RAM Allocation'. The DWC_otg core does not have any corrective logic if the FIFO sizes are programmed incorrectly.

DIEPTXF1

Device IN Endpoint Transmit FIFO Size Register 1

MEM Offset (B0050000)	104h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0022_005Ch

Table 116. Detailed Description of DIEPTXF1

Bits	Access Type	Default	Description
31:16	RW	16'h0022	IN Endpoint TxFIFO Depth (IN_EPN_TXF_DEP) This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 32,768 The power-on reset value of this register is specified as the largest IN Endpoint FIFO number Depth. Programmed values must not exceed the power-on value.
15:0	RW	16'h005c	IN Endpoint FIFO 1 Transmit RAM Start Address (IN_EPN_TXF_ST_ADDR) This field contains the memory start address For IN endpoint Transmit FIFO 1. The power-on reset value of this register is specified as the largest Rx Data FIFO Depth. Programmed values must not exceed the power-on value.

DIEPTXF2

Device IN Endpoint Transmit FIFO Size Register 2

MEM Offset (B0050000)	108h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits



Default

0022_007Eh

Table 117 Detailed Description of DIEPTXF2

Bits	Access Type	Default	Description
31:16	RW	16'h0022	IN Endpoint TxFIFO Depth (IN_EPN_TXF_DEP) This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 32,768 The power-on reset value of this register is specified as the largest IN Endpoint FIFO number Depth. Programmed values must not exceed the power-on value.
15:0	RW	16'h007e	IN Endpoint FIFO 2 Transmit RAM Start Address (IN_EPN_TXF_ST_ADDR) This field contains the memory start address For IN endpoint Transmit FIFO 2. The power-on reset value of this register is specified as the largest Rx Data FIFO Depth. Programmed values must not exceed the power-on value.

DIEPTXF3

Device IN Endpoint Transmit FIFO Size Register 3

MEM Offset (B0050000) 10Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0022_00A0h

Table 118. Detailed Description of DIEPTXF3

Bits	Access Type	Default	Description
31:16	RW	16'h0022	IN Endpoint TxFIFO Depth (IN_EPN_TXF_DEP) This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 32,768 The power-on reset value of this register is specified as the largest IN Endpoint FIFO number Depth. Programmed values must not exceed the power-on value.
15:0	RW	16'h00a0	IN Endpoint FIFO 3 Transmit RAM Start Address (IN_EPN_TXF_ST_ADDR) This field contains the memory start address For IN endpoint Transmit FIFO 3. The power-on reset value of this register is specified as the largest Rx Data FIFO Depth. Programmed values must not exceed the power-on value.

**DIEPTXF4**

Device IN Endpoint Transmit FIFO Size Register 4

MEM Offset (B0050000) 110h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0022_00C2h

Table 119. Detailed Description of DIEPTXF4

Bits	Access Type	Default	Description
31:16	RW	16'h0022	IN Endpoint TxFIFO Depth (IN_EPN_TXF_DEP) This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 32,768 The power-on reset value of this register is specified as the largest IN Endpoint FIFO number Depth. Programmed values must not exceed the power-on value.
15:0	RW	16'h00c2	IN Endpoint FIFO 4 Transmit RAM Start Address (IN_EPN_TXF_ST_ADDR) This field contains the memory start address For IN endpoint Transmit FIFO 4. The power-on reset value of this register is specified as the largest Rx Data FIFO Depth. Programmed values must not exceed the power-on value.

DIEPTXF5

Device IN Endpoint Transmit FIFO Size Register 5

MEM Offset (B0050000) 114h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0022_00E4h

Table 120. Detailed Description of DIEPTXF5

Bits	Access Type	Default	Description
31:16	RW	16'h0022	IN Endpoint TxFIFO Depth (IN_EPN_TXF_DEP) This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 32,768 The power-on reset value of this register is specified as the largest IN Endpoint FIFO number Depth. Programmed values must not exceed the power-on value.



Bits	Access Type	Default	Description
15:0	RW	16'h00e4	IN Endpoint FIFO 5 Transmit RAM Start Address (IN_EPN_TXF_ST_ADDR) This field contains the memory start address For IN endpoint Transmit FIFO 5. The power-on reset value of this register is specified as the largest Rx Data FIFO Depth. Programmed values must not exceed the power-on value.

DCFG

Device Configuration Register

MEM Offset (B0050000)	800h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0800_0000h

Table 121. Detailed Description of DCFG

Bits	Access Type	Default	Description
31:26	RW	6'h02	Resume Validation Period (RES_VALID) This field is effective only when DCFG.Ena32kHzSusp is set. It will control the resume period when the core resumes from suspend. The core counts for ResValid number of clock cycles to detect a valid resume when this is set
25:24	RW	2'h0	Periodic Scheduling Interval (PER_SCH_INTTVL) PerSchIntvl must be programmed only for Scatter/Gather DMA mode. Description: This field specifies the amount of time the Internal DMA engine must allocate for fetching periodic IN endpoint data. Based on the number of periodic endpoints, this value must be specified as 25,50 or 75% of (micro)frame. When any periodic endpoints are active, the internal DMA engine allocates the specified amount of time in fetching periodic IN endpoint data. When no periodic endpoints are active, Then the internal DMA engine services non-periodic endpoints, ignoring this field. After the specified time within a (micro)frame, the DMA switches to fetching for non-periodic endpoints. 2'b00: 25% of (micro)frame. 2'b01: 50% of (micro)frame. 2'b10: 75% of (micro)frame. 2'b11: Reserved. Reset: 2'b00
23:16	RO	8'h0	RSV (RSV) Reserved



Bits	Access Type	Default	Description
15	RW	1'h0	Erratic Error Interrupt Mask (ERRATICINTMSK) 1'b1: Mask early suspend interrupt on erratic error 1'b0: Early suspend interrupt is generated on erratic error
14	RW	1'h0	XCVRDLT (XCVRDLT) 1'b1: Enable delay between xcvr_sel and txvalid during Device chirp 1'b0: No delay between xcvr_sel and txvalid during Device chirp
13	RW/O/V	1'h0	Enable Device OUT NAK (EN_DEV_OUT_NAK) This bit enables setting NAK for Bulk OUT endpoints after the transfer is completed for Device mode Descriptor DMA 1'b0 : The core does not set NAK after Bulk OUT transfer complete 1'b1 : The core sets NAK after Bulk OUT transfer complete It is one time programmable after reset like any other DCFG register bits.
12:11	RW	2'h0	Periodic Frame Interval (PER_FR_INT) Indicates the time within a (micro)frame at which the application must be notified using the End Of Periodic Frame Interrupt. This can be used to determine If all the isochronous traffic for that (micro)frame is complete. 2'b00: 80% of the (micro)frame interval 2'b01: 85% 2'b10: 90% 2'b11: 95%
10:4	RW	7'h0	Device Address (DEV_ADDR) The application must program this field after every SetAddress control command.
3	RW	1'h0	Enable 32 kHz Suspend mode (ENA_32KHZ_SUSP) This bit can be set only if FS PHY interface is selected. Else, this bit needs to be set to zero. When FS PHY interface is chosen and this bit is set, the core expects that the PHY clock during Suspend is switched from 48 MHz to 32 kHz.
2	RW	1'h0	Non-Zero-Length Status OUT Handshake (NZ_STS_OUTH_SHK) The application can use this field to select the handshake the core sends on receiving a nonzero-length data packet during the OUT transaction of a control transfer's Status stage. 1'b1: Send a STALL handshake on a nonzero-length status OUT transaction and do not send the received OUT packet to the application. 1'b0: Send the received OUT packet to the application (zerolength or nonzero-length) and send a handshake based on the NAK and STALL bits for the endpoint in the Device Endpoint Control register.



Bits	Access Type	Default	Description
1:0	RW	2'h0	Device Speed (DEV_SPD) Indicates the speed at which the application requires the core to enumerate, or the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the core is connected. 2'b00: Not supported 2'b01: Not supported 2'b10: Low speed (USB 1.1 transceiver clock is 6 MHz). If you select 6 MHz LS mode, you must do a soft reset. 2'b11: Full speed (USB 1.1 transceiver clock is 48 MHz)

DCTL

Device Control Register

MEM Offset (B0050000)	804h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0002h

Table 122. Detailed Description of DCTL

Bits	Access Type	Default	Description
31:17	RW	15'h0	RSV_1 (RSV_1)
16	RW	1'h0	NAK on Babble Error (NAK_ON_BABLE) Set NAK automatically on babble. The core sets NAK automatically for the endpoint on which babble is received



Bits	Access Type	Default	Description
15	RW	1'h0	Ignore Frame number for Isochronous End points (IGNR_FRM_NUM) Do NOT program IgnrFrmNum bit to 1'b1 when the core is operating in threshold mode. Note: When Scatter/Gather DMA mode is enabled this feature is not applicable to High Speed, High bandwidth transfers. When this bit is enabled, there must be only one packet per descriptor. 0: The core transmits the packets only in the frame number in which they are intended to be transmitted. 1: The core ignores the frame number, sending packets immediately as the packets are ready. In Scatter/Gather DMA mode, if this bit is enabled, the packets are not flushed when a ISOC IN token is received for an elapsed frame. When Scatter/Gather DMA mode is disabled, this field is used by the application to enable periodic transfer interrupt. The application can program periodic endpoint transfers for multiple (micro) frames. 0: periodic transfer interrupt feature is disabled, application needs to program transfers for periodic endpoints every (micro) frame 1: periodic transfer interrupt feature is enabled, application can program transfers for multiple (micro)frames for periodic endpoints. In non Scatter/Gather DMA mode the application will receive transfer complete interrupt after transfers for multiple (micro)frames are completed.
14:12	RO	3'h0	RSV (RSV) Reserved
11	RW	1'h0	Power-On Programming Done (PWR_ON_PROG_DONE) The application uses this bit to indicate that register programming is completed after a wake-up from Power Down mode.
10	WO	1'h0	Clear Global OUT NAK (CG_OUT_NAK) A write to this field clears the Global OUT NAK.
9	WO	1'h0	Set Global OUT NAK (SG_OUT_NAK) A write to this field sets the Global OUT NAK. The application uses this bit to send a NAK handshake on all OUT endpoints. The application must Set the this bit only after making sure that the Global OUT NAK Effective bit in the Core Interrupt Register (GINTSTS.GOUTNakEff) is cleared.
8	WO	1'h0	Clear Global Non-periodic IN NAK (CGNP_IN_NAK) A write to this field clears the Global Non-periodic IN NAK.



Bits	Access Type	Default	Description
7	WO	1'h0	Set Global Non-periodic IN NAK (SGNP_IN_NAK) A write to this field sets the Global Non-periodic IN NAK. The application uses this bit to send a NAK handshake on all non periodic IN endpoints. The core can also Set this bit when a timeout condition is detected on a non-periodic endpoint in shared FIFO operation. The application must Set this bit only after making sure that the Global IN NAK Effective bit in the Core Interrupt Register (GINTSTS.GIN_NAK_EFF) is cleared
6:4	RW	3'h0	Test Control (TST_CTL) 3'b000: Test mode disabled 3'b001: Test_J mode 3'b010: Test_K mode 3'b011: Test_SE0_NAK mode 3'b100: Test_Packet mode 3'b101: Test_Force_Enable Others: Reserved
3	RO	1'h0	Global OUT NAK Status (GOUT_NAK_STS) 1'b0: A handshake is sent based on the FIFO Status and the NAK and STALL bit settings. 1'b1: No data is written to the RxFIFO, irrespective of space availability. Sends a NAK handshake on all packets, except on SETUP transactions. All isochronous OUT packets are dropped.
2	RO	1'h0	Global Non-periodic IN NAK Status (GNPIN_NAK_STS) 1'b0: A handshake is sent out based on the data availability in the transmit FIFO. 1'b1: A NAK handshake is sent out on all non-periodic IN endpoints, irrespective of the data availability in the transmit FIFO.
1	RW	1'h1	Soft Disconnect (SFT_DISCON) The application uses this bit to signal the DWC_otg core to do a soft disconnect. As long as this bit is Set, the host does not see that the device is connected, and the device does not receive signals on the USB. The core stays in the disconnected state until the application clears this bit. The minimum duration for which the core must keep this bit set is 1002.5us when in the suspended state or 2.5us when not in the suspended state. 1'b0: Normal operation. When this bit is cleared after a soft disconnect, the core drives the phy_opmode_o signal on the UTMI+ to 2'b00, which generates a device connect event to the USB host. When the device is reconnected, the USB host restarts device enumeration. 1'b1: The core drives the phy_opmode_o signal on the UTMI+ to 2'b01, which generates a device disconnect event to the USB host. Note: This bit can be also used for ULPI/FS Serial interfaces. Note: This bit is not impacted by a soft reset.



Bits	Access Type	Default	Description
0	RW	1'h0	Remote Wakeup Signalling (RMT_WK_UP_SIG) When the application sets this bit, the core initiates remote signalling to wake up the USB host. The application must Set this bit to instruct the core to exit the Suspend state. The application must clear this bit 1-15 ms after setting it.

DSTS

Device Status Register

MEM Offset (B0050000) 808h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0002h

Table 123. Detailed Description of DSTS

Bits	Access Type	Default	Description
31:24	RO	8'h0	RSV_1 (RSV_1) Reserved
23:22	RO	2'h0	Device Line Status (DEV_LN_STS) Indicates the current logic level USB data lines DEV_LN_STS[1]: Logic level of USB_PADP DEV_LN_STS[0]: Logic level of USB_PADN
21:8	RO	14'h0	Frame number of Received SOF (SOFFN) SOFFN is valid only after a valid connection between host and device is established. This register may return a non zero value if read immediately after power on reset. In case the register bit reads non zero immediately after power on reset it does not indicate that SOF has been received from the host.
7:4	RW	4'h0	RSV (RSV) Reserved
3	RO	1'h0	Erratic Error (ERRATIC_ERR) The core sets this bit to report any erratic errors (phy_rxvalid_i/phy_rxvldh_i or phy_rxactive_i is asserted for at least 2 ms, due to PHY error) seen on the UTMI+. Due to erratic errors, the DWC_otg core goes into Suspended state and an interrupt is generated to the application with Early Suspend bit of the Core Interrupt register (GINTSTS.ERLY_SUSP). If the early suspend is asserted due to an erratic error, the application can only perform a soft disconnect recover.



Bits	Access Type	Default	Description
2:1	RO	2'h1	Enumerated Speed (ENUM_SPD) Indicates the speed at which the DWC_otg core has come up after speed detection through a chirp sequence. 2'b00: Not supported 2'b01: Not supported 2'b10: Low speed (PHY clock is running at 6 MHz) 2'b11: Full speed (PHY clock is running at 48 MHz).
0	RO	1'h0	Suspend Status (SUSP_STS) In Device mode, this bit is Set as long as a Suspend condition is detected on the USB. The core enters the Suspended state when there is no phy activity for an extended period of time. The core comes out of the suspend state: - When there is any phy activity - When the application writes to the Remote Wakeup Signalling bit in the Device Control register (DCTL.RMT_WK_UP_SIG)

DIEPMSK

Device IN Endpoint Common Interrupt Mask Register

MEM Offset (B0050000)	810h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 124. Detailed Description of DIEPMSK

Bits	Access Type	Default	Description
31:14	RO	18'h0	RSV_2 (RSV_2) Reserved
13	RW	1'h0	NYET interrupt Mask (NAK_INTRPT_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
12:9	RO	4'h0	RSV_1 (RSV_1) Reserved
8	RW	1'h0	Fifo Underrun Mask (TX_FIFO_UNDRUN_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
7	RO	1'h0	RSV (RSV) Reserved



Bits	Access Type	Default	Description
6	RW	1'h0	IN Endpoint NAK Effective Mask (IN_TKN_NAK_EFF_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
5	RW	1'h0	IN Token received with EP Mismatch Mask (IN_TKN_EP_MIS_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
4	RW	1'h0	IN Token Received When TxFIFO Empty Mask (IN_TKN_TX_FEMP_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
3	RW	1'h0	Timeout Condition Mask (TIME_OUT_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
2	RW	1'h0	AHB Error Mask (AHB_ERR_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
1	RW	1'h0	Endpoint Disabled Interrupt Mask (EP_DISBLD_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
0	RW	1'h0	Transfer Completed Interrupt Mask (XFER_COMPL_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.

DOEPMASK

Device OUT Endpoint Common Interrupt Mask Register

MEM Offset (B0050000)	168h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 125. Detailed Description of DOEPMASK

Bits	Access Type	Default	Description
31:15	RO	17'h0	RSV_2 (RSV_2) Reserved
14	RW	1'h0	NYET interrupt Mask (NYET_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.



Bits	Access Type	Default	Description
13	RW	1'h0	NAK Interrupt Mask (NAK_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
12	RW	1'h0	Babble Error Interrupt Mask (BBLE_ERR_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
11:9	RO	3'h0	RSV_1 (RSV_1) Reserved
8	RW	1'h0	OUT Packet Error Interrupt Mask (OUT_PKT_ERR_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
7	RO	1'h0	RSV (RSV) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
6	RW	1'h0	Back-to-Back SETUP Packets Received Interrupt Mask (BAC2BACK_SETUP_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
5	RW	1'h0	Status Phase Received Interrupt Mask (STS_PHSE_RCVD_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
4	RW	1'h0	OUT Token Received when Endpoint Disabled Interrupt Mask (OUT_TKN_EP_DIS_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
3	RW	1'h0	SETUP Phase Done Interrupt Mask (SET_UP_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
2	RW	1'h0	AHB Error Interrupt Mask (AHB_ERR_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
1	RW	1'h0	Endpoint Disabled Interrupt Mask (EP_DISBLD_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
0	RW	1'h0	Transfer Completed Interrupt Mask (XFER_COMPL_MSK) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.

DAINT

Device Interrupt Register



MEM Offset (B0050000)	818h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 126. Detailed Description of DAIN

Bits	Access Type	Default	Description
31:20	RO	12'h0	RSV_1 (RSV_1) Reserved
19	RO	1'h0	Out Endpoint 3 Interrupt Bit (OUT_EP_INT3)
18	RO	1'h0	Out Endpoint 2 Interrupt Bit (OUT_EP_INT2)
17	RO	1'h0	Out Endpoint 1 Interrupt Bit (OUT_EP_INT1)
16	RO	1'h0	Out Endpoint 0 Interrupt Bit (OUT_EP_INT0)
15:6	RO	10'h0	RSV (RSV) Reserved
5	RO	1'h0	In Endpoint 5 Interrupt Bit (IN_EP_INT5)
4	RO	1'h0	In Endpoint 4 Interrupt Bit (IN_EP_INT4)
3	RO	1'h0	In Endpoint 3 Interrupt Bit (IN_EP_INT3)
2	RO	1'h0	In Endpoint 2 Interrupt Bit (IN_EP_INT2)
1	RO	1'h0	In Endpoint 1 Interrupt Bit (IN_EP_INT1)
0	RO	1'h0	In Endpoint 0 Interrupt Bit (IN_EP_INT0)

DAINTMSK

Device Interrupt Mask Register

MEM Offset (B0050000)	81Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 127. Detailed Description of DAINTRMSK

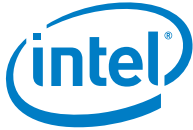
Bits	Access Type	Default	Description
31:20	RW	12'h0	RSV_1 (RSV_1) Reserved
19	RW	1'h0	Out Endpoint 3 Interrupt mask bit. (OUT_EP_MSK3) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
18	RW	1'h0	Out Endpoint 2 Interrupt mask bit. (OUT_EP_MSK2) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
17	RW	1'h0	Out Endpoint 1 Interrupt mask bit. (OUT_EP_MSK1) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
16	RW	1'h0	Out Endpoint 0 Interrupt mask bit. (OUT_EP_MSK0) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
15:6	RW	10'h0	RSV (RSV) Reserved
5	RW	1'h0	In Endpoint 5 Interrupt mask bit. (IN_EP_MSK5) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
4	RW	1'h0	In Endpoint 4 Interrupt mask bit. (IN_EP_MSK4) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
3	RW	1'h0	In Endpoint 3 Interrupt mask bit. (IN_EP_MSK3) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
2	RW	1'h0	In Endpoint 2 Interrupt mask bit. (IN_EP_MSK2) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
1	RW	1'h0	In Endpoint 1 Interrupt mask bit. (IN_EP_MSK1) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.
0	RW	1'h0	In Endpoint 0 Interrupt mask bit. (IN_EP_MSK0) 1'b1: Interrupt masked. 1'b0: Interrupt unmasked.

DVBUSDIS

Device VBUS Discharge Time Register

MEM Offset (B0050000)

828h



Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_17D7h

Table 128. Detailed Description of DVBUSDIS

Bits	Access Type	Default	Description
31:16	RO	16'h0	RSV (RSV) Reserved
15:0	RW	16'h17d7	Device VBUS Discharge Time (DV_BUS_DIS) Specifies the VBUS discharge time after VBUS pulsing during SRP. This value equals: VBUS discharge time in PHY clocks / 1,024 The value you use depends whether the PHY is operating at 30 MHz (16-bit data width) or 60 MHz (8-bit data width). Depending on your VBUS load, this value can need adjustment. Indicates that the AHB Master State Machine is in the IDLE condition.

DVBUSPULSE

Device VBUS Discharge Time Register

MEM Offset (B0050000) 82Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_05B8h

Table 129. Detailed Description of DVBUSPULSE

Bits	Access Type	Default	Description
31:12	RO	20'h0	RSV (RSV) Reserved
11:0	RW	12'h5b8	Device VBUS Pulsing Time (DV_BUS_PULSE) Specifies the VBUS pulsing time during SRP. This value equals: VBUS pulsing time in PHY clocks / 1,024 The value you use depends whether the PHY is operating at 30 MHz (16-bit data width) or 60 MHz (8-bit data width).

DTHRCTL

Device Threshold Control Register

MEM Offset (B0050000) 830h
Security_PolicyGroup
IntelRsvd False
Size 32 bits

Default

0810_0010h

Table 130. Detailed Description of DTHRCTL

Bits	Access Type	Default	Description
31:28	RO	4'h0	RSV_2 (RSV_2) Reserved
27	RW	1'h1	Arbiter Parking Enable (ARB_PRK_EN) This bit controls internal DMA arbiter parking For IN endpoints. When thresholding is enabled and this bit is Set to one, Then the arbiter parks on the IN endpoint For which there is a token received on the USB. This is done to avoid getting into underrun conditions. By Default the parking is enabled.
26	RO	1'h0	RSV_1 (RSV_1) Reserved
25:17	RW	9'h8	Receive Threshold Enable (RX_THR_LEN) This field specifies Receive thresholding size in DWORDS. This field also specifies the amount of data received on the USB before the core can start transmitting on the AHB. The threshold length has to be at least eight DWORDS. The recommended value for RX_THR_LEN is to be the same as the programmed AHB Burst Length (GAHBCFG.HBST_LEN).
16	RW	1'h0	Receive Threshold Enable (RX_THR_EN) When this bit is Set, the core enables thresholding in the receive direction. Note: We recommend that you do not enable RX_THR_EN, because it may cause issues in the RxFIFO especially during error conditions such as RxError and Babble.
15:13	RO	3'h0	RSV (RSV) Reserved
12:11	RW	2'h0	AHB Threshold Ratio (AHB_THR_RATIO) These bits define the ratio between the AHB threshold and the MAC threshold for the transmit path only. The AHB threshold always remains less than or equal to the USB threshold, because this does not increase overhead. Both the AHB and the MAC threshold must be DWORD-aligned. The application needs to program TX_THR_LEN and the AHB_THR_RATIO to make the AHB Threshold value DWORD aligned. If the AHB threshold value is not DWORD aligned, the core might not behave correctly. When programming the TX_THR_LEN and AHB_THR_RATIO, the application must ensure that the minimum AHB threshold value does not go below 8 DWORDS to meet the USB turnaround time requirements. 2'b00: AHB threshold = MAC threshold 2'b01: AHB threshold = MAC threshold / 2 2'b10: AHB threshold = MAC threshold / 4 2'b11: AHB threshold = MAC threshold / 8



Bits	Access Type	Default	Description
10:2	RW	9'h4	Transmit Threshold Length (TX_THR_LEN) This field specifies Transmit thresholding size in DWORDS. This also forms the MAC threshold and specifies the amount of data in bytes to be in the corresponding endpoint transmit FIFO, before the core can start transmit on the USB. The threshold length has to be at least eight DWORDS when the value of AHB_THR_RATIO is 2'h00. In case the AHB_THR_RATIO is non zero the application needs to ensure that the AHB Threshold value does not go below the recommended eight DWORD. This field controls both isochronous and non-isochronous IN endpoint thresholds. The recommended value for THR_LEN is to be the same as the programmed AHB Burst Length (GAHBCFG.HBST_LEN).
1	RW	1'h0	ISO IN Endpoints Threshold Enable (ISO_THR_EN) When this bit is Set, the core enables thresholding for isochronous IN endpoints.
0	RW	1'h0	Non-ISO IN Endpoints Threshold Enable (NON_ISO_THR_EN) When this bit is Set, the core enables thresholding for Non Isochronous IN endpoints.

DIEPEMPMSK

Device IN Endpoint FIFO Empty Interrupt Mask Register

MEM Offset (B0050000)	834h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 131. Detailed Description of DIEPEMPMSK

Bits	Access Type	Default	Description
31:16	RO	16'h0	RSV (RSV) Reserved
15:0	RW	16'h0	IN EP Tx FIFO Empty Interrupt Mask Bits (IN_EP_TX_FEMP_MSK) These bits acts as mask bits For DIEPINTn.TX_FEMP interrupt one bit per IN Endpoint: Bit 0 for IN EP 0, bit 15 for IN EP 15.

DIEPCTL0

Device IN End Point Control Register 0

MEM Offset (B0050000)	900h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_8000h



Table 132. Detailed Description of DIEPCTL0

Bits	Access Type	Default	Description
31	RW/1S/V	1'h0	Endpoint Enable (EP_ENA) When Scatter/Gather DMA mode is enabled, for IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. When Scatter/Gather DMA mode is disabled such as in buffer pointer based DMA mode this bit indicates that data is ready to be transmitted on the endpoint. The core clears this bit before setting the following interrupts on this endpoint: - Endpoint Disabled - Transfer Completed
30	RW/1S/V	1'h0	Endpoint Disable (EP_DIS) The application sets this bit to stop transmitting data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled Interrupt. The application must Set this bit only if Endpoint Enable is already Set for this endpoint.
29:28	RO	2'h0	RSV_2 (RSV_2) Reserved
27	WO	1'h0	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also Set this bit for an endpoint after a SETUP packet is received on that endpoint.
26	WO	1'h0	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint.
25:22	RW	4'h0	TxFIFO Number (TX_FNUM) For Shared FIFO operation, this value is always Set to 0, indicating that control IN endpoint 0 data is always written in the Non-Periodic Transmit FIFO. For Dedicated FIFO operation, this value is Set to the FIFO number that is assigned to IN Endpoint 0.
21	RW/O	1'h0	STALL Handshake (STALL) The application can only set this bit, and the core clears it, when a setup token is received for this endpoint. If a NAK bit, Global Non periodic IN NAK, or Global OUT NAK is Set along with this bit, the STALL bit takes priority.
20	RO	1'h0	RSV_1 (RSV_1)
19:18	RO	2'h0	Endpoint Type (EP_TYPE) Hardcoded to 00 for control



Bits	Access Type	Default	Description
17	RO	1'h0	NAK Status (NAK_STS) Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status 1'b1: The core is transmitting NAK handshakes on this endpoint. When this bit is Set, either by the application or core, the core stops transmitting data, even If there is data available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
16	RO	1'h0	RSV_3 (RSV_3)
15	RO	1'h1	USB Active Endpoint (USB_ACT_EP) This bit is always SET to 1, indicating that control endpoint 0 is always active in all configurations and interfaces.
14:2	RO	13'h0	RSV (RSV) Reserved
1:0	RW	2'h0	Maximum Packet Size (MPS) Applies to IN and OUT endpoints. The application must program this field with the maximum packet size for the current logical endpoint. 2'b00: 64 bytes 2'b01: 32 bytes 2'b10: 16 bytes 2'b11: 8 bytes

DIEPINT0

Device In EP0 Interrupt Register

MEM Offset (B0050000)	908h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0080h

Table 133. Detailed Description of DIEPINT0

Bits	Access Type	Default	Description
31:15	RO	17'h0	RSV_2 (RSV_2) Reserved
14	RW/1C	1'h0	NYET Interrupt (NYET_INTRPT) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint.



Bits	Access Type	Default	Description
13	RW/1C	1'h0	NAK Interrupt (NAK_INTRPT) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo.
12	RW/1C	1'h0	Babble Error Interrupt (BBLE_ERR) The core generates this interrupt when babble is received for the endpoint.
11	RW/1C	1'h0	Packet Drop Status (PKT_DRP_STS) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.
10	RO	1'h0	RSV_1 (RSV_1) Reserved
9	RW/1C	1'h0	Buffer Not Available Interrupt (BNA_INTR) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done
8	RW/1C	1'h0	Transmit Fifo Underrun (TX_FIFO_UNDRUN) Applies to IN endpoints Only. The core generates this interrupt when it detects a transmit FIFO underrun condition in threshold mode for this endpoint.
7	RO	1'h1	Transmit FIFO Empty (TX_FEMP) This bit is valid only for IN Endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTXFE_EMP_LVL)).
6	RW/1C/V/L	1'h0	In Endpoint NAK Effective (IN_TKN_NAK_EFF) Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCTLn.CNAK. This interrupt indicates that the core has sampled the NAK bit Set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit Set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit.



Bits	Access Type	Default	Description
5	RW/1C	1'h0	IN Token Received with EP Mismatch (IN_TKN_EP_MIS) Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received.
4	RW/1C	1'h0	IN Token Received When TxFIFO is Empty (IN_TKN_TX_FEMP) Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received.
3	RW/1C	1'h0	Timeout Condition (TIME_OUT) In shared TX FIFO mode, applies to non-isochronous IN endpoints only. In dedicated FIFO mode, applies only to Control IN endpoints. In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint.
2	RW/1C	1'h0	AHB Error (AHB_ERR) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address.
1	RW/1C/V/L	1'h0	Endpoint Disabled Interrupt (EP_DISBLD) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.
0	RW/1C	1'h0	Transfer Completed Interrupt (XFER_COMPL) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled: - For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. - For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is Set. When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint.

DIEPTSIZE

Device IN Size Register 0



MEM Offset (B0050000) 910h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 134. Detailed Description of DIEPTSIZE0

Bits	Access Type	Default	Description
31:21	RO	11'h0	RSV_2 (RSV_2) Reserved
20:19	RW	2'h0	Packet Count (PKT_CNT) Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. In Endpoints : This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. OUT Endpoints: This field is decremented every time a packet (maximum size or short packet) is written to the RxFIFO.
18:7	RO	12'h0	RSV (RSV) Reserved
6:0	RW	7'h0	Transfer Size (XFER_SIZE_WIDTH) This field contains the transfer size in bytes for the current endpoint. The transfer size (XferSize) = Sum of buffer sizes across all descriptors in the list for the endpoint. In Buffer DMA, the core only interrupts the application after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. IN Endpoints: The core decrements this field every time a packet from the external memory is written to the TxFIFO. OUT Endpoints: The core decrements this field every time a packet is read from the RxFIFO and written to the external memory.

DIEPDMA0

Device OUT End Point DMA Address Register 0

MEM Offset (B0050000) 914h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

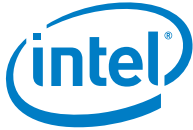


Table 135. Detailed Description of DIEPDMA0

Bits	Access Type	Default	Description
31:0	RW	32'h0	DMA Address (DMA_ADDR) Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list.

DTXFSTS0

Device IN Endpoint Transmit FIFO Status Register 0

MEM Offset (B0050000)	918h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0022h

Table 136. Detailed Description of DTXFSTS0

Bits	Access Type	Default	Description
31:16	RO	16'h0	RSV (RSV) Reserved
15:0	RO	16'h22	IN Endpoint TxFIFO Space Avail (IN_EP_TXF_SPC_AVAIL) Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. 16'h0: Endpoint TxFIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'h n : n words available (where $0 \leq n \leq 32,768$) 16'h8000: 32,768 words available Others: Reserved

DIEPINTn (DIEPINTn [1..5])

Device In EPn Interrupt Register

MEM Offset (B0050000)	[1]:928h [2]:948h [3]:968h [4]:988h [5]:9A8h
Security_PolicyGroup	
IntelRsvd	False



Size
Default

32 bits
0000_0080h

Table 137. Detailed Description of DIEPINTn (DIEPINTn [1..5])

Bits	Access Type	Default	Description
31:15	RO	17'h0	RSV_2 (RSV_2) Reserved
14	RW/1C	1'h0	NYET Interrupt (NYET_INTRPT) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint.
13	RW/1C	1'h0	NAK Interrupt (NAK_INTRPT) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo.
12	RW/1C	1'h0	Babble Error (BBLE_ERR) The core generates this interrupt when babble is received for the endpoint.
11	RW/1C	1'h0	Packet Drop Status (PKT_DRP_STS) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.
10	RO	1'h0	RSV_1 (RSV_1) Reserved
9	RW/1C	1'h0	Buffer Not Available Interrupt (BNA_INTR) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done
8	RW/1C	1'h0	Fifo Underrun (TX_FIFO_UNDRUN) Applies to IN endpoints Only This bit is valid only If thresholding is enabled. The core generates this interrupt when it detects a transmit FIFO underrun condition for this endpoint.
7	RO	1'h1	Transmit FIFO Empty (TX_FEMP) This bit is valid only for IN Endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTXFE_EMP_LVL)



Bits	Access Type	Default	Description
6	RW/1C	1'h0	IN Endpoint NAK Effective (IN_TKN_NAK_EFF) Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCTLn.CNAK. This interrupt indicates that the core has sampled the NAK bit Set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit Set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit.
5	RW/1C	1'h0	IN Token Received with EP Mismatch (IN_TKN_EP_MIS) Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received.
4	RW/1C	1'h0	IN Token Received When TxFIFO is Empty (IN_TKN_TX_FEMP) Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received.
3	RW/1C	1'h0	TIME_OUT (TIME_OUT) In shared TX FIFO mode, applies to non-isochronous IN endpoints only. In dedicated FIFO mode, applies only to Control IN endpoints. In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint.
2	RW/1C	1'h0	AHB Error (AHB_ERR) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address.
1	RW/1C/V/L	1'h0	Endpoint Disabled Interrupt (EP_DISBLD) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.



Bits	Access Type	Default	Description
0	RW/1C	1'h0	Transfer Completed Interrupt (XFER_COMPL) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled: - For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. - For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is Set. When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint.

DIEPCTLn (DIEPCTLn [1..5])

Device IN End Point Control Register n

MEM Offset (B0050000)	[0]:920h [1]:940h [2]:960h [3]:980h [4]:9A0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_8000h

Table 138. Detailed Description of DIEPCTLn (DIEPCTLn [1..5])

Bits	Access Type	Default	Description
31	RW/1S/V	1'h0	Endpoint Enable (EP_ENA) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, for IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. for OUT endpoints it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is disabled such as for buffer-pointer based DMA mode: - For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. - For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. - The core clears this bit before setting any of the following interrupts on this endpoint: SETUP Phase Done Endpoint Disabled Transfer Completed Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory.



Bits	Access Type	Default	Description
30	RW/1S/V	1'h0	Endpoint Disable (EP_DIS) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.
29	WO	1'h0	Set DATA1 PID (SETD1PID) Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode.
28	WO	1'h0	Set DATA0 PID (SETDOPID) Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode.
27	WO	1'h0	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint.
26	WO	1'h0	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint.
25:22	RW	4'h0	TxFIFO Number (TX_FNUM) Shared FIFO Operation non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. 4'h0: Non-Periodic TxFIFO Others: Specified Periodic TxFIFO.number Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum field is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint, and the number of this FIFO must be programmed into the TX_FNUM field. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. In dedicated FIFO Operation these bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This field is valid only for IN endpoints.
21	RW/O	1'h0	STALL Handshake (STALL) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core.



Bits	Access Type	Default	Description
20	RO	1'h0	RSV_1 (RSV_1)
19:18	RW	2'h0	Endpoint Type (EP_TYPE) This is the transfer type supported by this logical endpoint. 2'b00: Control 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt
17	RO	1'h0	NAK Status (NAK_STS) Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
16	RO	1'h0	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. 1'b0: DATA0 1'b1: DATA1 This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode.
15	RW/V	1'h1	USB Active Endpoint (USB_ACT_EP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit.
14:11	RO	4'h0	RSV (RSV) Reserved
10:0	RW	11'h0	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes.

**DIEPTSiZn (DIEPTSiZn [1..5])**

Device IN Size Register n

MEM Offset (B0050000) [0]:930h [1]:950h [2]:970h [3]:990h
[4]:9B0h

Security_PolicyGroup**IntelRsvd**

False

Size

32 bits

Default

0000_0000h

Table 139. Detailed Description of DIEPTSiZn (DIEPTSiZn [1..5])

Bits	Access Type	Default	Description
31	RO	1'h0	RSV (RSV) Reserved
30:29	RW	2'h0	Multi Count (MC) Applies to IN endpoints only. For periodic IN endpoints, this field indicates the number of packets that must be transmitted per microframe on the USB. The core uses this field to calculate the data PID for isochronous IN endpoints. 2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets For non-periodic IN endpoints, this field is valid only in Internal DMA mode. It specifies the number of packets the core must fetch for an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint field of the Device Endpoint-n Control register (DIEPCTLn.NEXT_EP)
28:19	RW	10'h0	Packet Count (PKT_CNT) Indicates the total number of USB packets that constitute the Transfer Size amount of data For endpoint 0. This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO.
18:0	RW	19'h0	Transfer Size (XFER_SIZE_WIDTH) Indicates the transfer size in bytes For endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet from the external memory is written to the TxFIFO.

DIEPDMA_n (DIEPDMA_n [1..5])

Device OUT End Point DMA Address Register n

MEM Offset (B0050000) [0]:934h [1]:954h [2]:974h [3]:994h
[4]:9B4h

Security_PolicyGroup**IntelRsvd**

False



Size 32 bits
Default 0000_0000h

Table 140. Detailed Description of DIEPDMA_n (DIEPDMA_n [1..5])

Bits	Access Type	Default	Description
31:0	RW	32'h0	DMA Address (DMA_ADDR) Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list.

DTXFST_n (DTXFST_n [1..5])

Device IN Endpoint Transmit FIFO Status Register n

MEM Offset (B0050000) [0]:938h [1]:958h [2]:978h [3]:998h [4]:9B8h

Security_PolicyGroup IntelRsvd False

Size 32 bits

Default 0000_0022h

Table 141. Detailed Description of DTXFST_n (DTXFST_n [1..5])

Bits	Access Type	Default	Description
31:16	RO	16'h0	RSV (RSV) Reserved
15:0	RO	16'h22	IN Endpoint Tx FIFO Space Avail (IN_EP_TXF_SPC_AVAIL) Indicates the amount of free space available in the Endpoint Tx FIFO. Values are in terms of 32-bit words. 16'h0: Endpoint Tx FIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'h _n : n words available (where 0 ≤ n ≤ 32,768) 16'h8000: 32,768 words available Others: Reserved

DOEPTL0

Device OUT End Point Control Register 0

MEM Offset (B0050000) B00h



Security_PolicyGroup

IntelRsvd

False

Size

32 bits

Default

0000_8000h

Table 142. Detailed Description of DOEPCTL0

Bits	Access Type	Default	Description
31	RW/O	1'h0	Endpoint Enable (EP_ENA) When Scatter/Gather DMA mode is enabled, for OUT endpoints this bit indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is disabled(such as for buffer-pointer based DMA mode)this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: - SETUP Phase Done - Endpoint Disabled - Transfer Completed Note: In DMA mode, this bit must be set for the core to transfer SETUP data packets into memory.
30	RO	1'h0	Endpoint Disable (EP_DIS) The application cannot disable control OUT endpoint 0.
29:28	RO	2'h0	RSV_3 (RSV_3)
27	WO	1'h0	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set bit on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.
26	WO	1'h0	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint.
25:22	RO	4'h0	RSV_2 (RSV_2)
21	RW/O	1'h0	STALL Handshake (STALL) The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
20	RW	1'h0	Snoop Mode (SNP) This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.
19:18	RO	2'h0	Endpoint Type (EP_TYPE) Hardcoded to 2'b00 for control.



Bits	Access Type	Default	Description
17	RO	1'h0	NAK Status (NAK_STS) Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit, the core stops receiving data, even if there is space in the RxFIFO to accommodate the incoming packet. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
16	RO	1'h0	RSV_1 (RSV_1)
15	RO	1'h1	USB Active Endpoint (USB_ACT_EP) This bit is always set to 1, indicating that a control endpoint 0 is always active in all configurations and interfaces.
14:2	RO	13'h0	RSV (RSV) Reserved
1:0	RO	2'h0	Maximum Packet Size (MPS) The maximum packet size for control OUT endpoint 0 is the same as what is programmed in control IN Endpoint 0. 2'b00: 64 bytes 2'b01: 32 bytes 2'b10: 16 bytes 2'b11: 8 bytes

DOEPINT0

Device Out EP0 Interrupt Register

MEM Offset (B0050000)	B08h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 143. Detailed Description of DOEPINT0

Bits	Access Type	Default	Description
31:16	RO	16'h0	RSV_2 (RSV_2) Reserved



Bits	Access Type	Default	Description
15	RW/1C	1'h0	Setup Packet Received (STUP_PKT_RCVD) Applicable for Control OUT Endpoints in Buffer DMA Mode Set by the DWC_otg core, this bit indicates that this buffer holds 8 bytes of Setup packet, the DWC_otg core closes the buffer and disables the corresponding endpoint. The application has to re-enable the endpoint to receive any OUT data for the Control Transfer and reprogram the buffer start address. Note: Because of the above behaviour, the DWC_otg core can receive any number of back to back setup packets and one buffer for every setup packet is used. 1'b0: No Setup packet received 1'b1: Setup packet received Reset: 1b0
14	RW/1C	1'h0	NYET Interrupt (NYET_INTRPT) The core generates this interrupt when a NYET response is transmitted for a non-isochronous OUT endpoint.
13	RW/1C	1'h0	NAK Interrupt (NAK_INTRPT) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TX Fifo.
12	RW/1C	1'h0	Babble Error Interrupt (BBLE_ERR) The core generates this interrupt when babble is received for the endpoint.
11	RW/1C	1'h0	Packet Drop Status (PKT_DRP_STS) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.
10	RO	1'h0	RSV_1 (RSV_1) Reserved
9	RW/1C	1'h0	Buffer Not Available Interrupt (BNA_INTR) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done
8	RW/1C	1'h0	OUT Packet Error (OUT_PKT_ERR) Applies to OUT endpoints Only This interrupt is valid only when thresholding is enabled. This interrupt is asserted when the core detects an overflow or a CRC error for non-Isochronous OUT packet.
7	RO	1'h0	RSV (RSV) Reserved



Bits	Access Type	Default	Description
6	RW/1C	1'h0	Back-to-Back SETUP Packets Received (BAC2BACK_SETUP) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint.
5	RW/1C	1'h0	Status Phase Received for Control Write (STS_PHSE_RCVD) This interrupt is valid only for Control OUT endpoints and only in Scatter Gather DMA mode. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the status phase, after it has decoded the data phase. This is applicable only in Case of Scatter Gather DMA mode.
4	RW/1C	1'h0	OUT Token Received When Endpoint Disabled (OUT_TKN_EP_DIS) Applies only to control OUT endpoints. Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received.
3	RW/1C	1'h0	SETUP Phase Done (SET_UP) Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet.
2	RW/1C	1'h0	AHB Error (AHB_ERR) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address.
1	RW/1C/V/L	1'h0	Endpoint Disabled Interrupt (EP_DISBLD) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.



Bits	Access Type	Default	Description
0	RW/1C	1'h0	Transfer Completed Interrupt (XFER_COMPL) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled: - For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. - For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is Set. When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint.

DOEPTSIZE0

Device OUT Size Register 0

MEM Offset (B0050000)

B10h

Security_PolicyGroup**IntelRsvd**

False

Size

32 bits

Default

0000_0000h

Table 144. Detailed Description of DOEPTSIZE0

Bits	Access Type	Default	Description
31	RO	1'h0	RSV_2 (RSV_2) Reserved
30:29	RW	2'h0	SETUP Packet Count (SUP_CNT) This field specifies the number of back-to-back SETUP datapackets the endpoint can receive. 2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets
28:20	RO	9'h0	RSV_1 (RSV_1) Reserved
19	RW	1'h0	Packet Count (PKT_CNT) This field is decremented to zero after a packet is written into the RxFIFO.
18:7	RO	12'h0	RSV (RSV) Reserved



Bits	Access Type	Default	Description
6:0	RW	7'h0	Transfer Size (XFER_SIZE_WIDTH) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from the RxFIFO and written to the external memory.

DOEPDMA0

Device OUT End Point DMA Address Register 0

MEM Offset (B0050000)	B14h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 145. Detailed Description of DOEPDMA0

Bits	Access Type	Default	Description
31:0	RW	32'h0	DMA Address (DMA_ADDR) Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list.

DOEPINTn (DOEPINTn [1..3])

Device Out EPn Interrupt Register

MEM Offset (B0050000)	[0]:0B28h [1]:0B48h [2]:0B68h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 146. Detailed Description of DOEPINTn (DOEPINTn [1..3])

Bits	Access Type	Default	Description
31:16	RO	16'h0	RSV_2 (RSV_2) Reserved



Bits	Access Type	Default	Description
15	RW/1C	1'h0	Setup Packet Received (STUP_PKT_RCVD) Applicable for Control OUT Endpoints in only in the Buffer DMA Mode Set by the DWC_otg core, this bit indicates that this buffer holds 8 bytes of setup data. There is only one setup packet per buffer. On receiving a setup packet, the DWC_otg core closes the buffer and disables the corresponding endpoint. The application has to re-enable the endpoint to receive any OUT data for the Control Transfer and reprogram the buffer start address. Note: Because of the above behaviour, the DWC_otg core can receive any number of back to back setup packets and one buffer for every setup packet is used. 1'b0: No Setup packet received 1'b1: Setup packet received Reset: 1b0
14	RW/1C	1'h0	NYET Interrupt (NYET_INTRPT) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint.
13	RW/1C	1'h0	NAK Interrupt (NAK_INTRPT) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo.
12	RW/1C	1'h0	Babble Error Interrupt (BBLE_ERR) The core generates this interrupt when babble is received for the endpoint.
11	RW/1C	1'h0	Packet Drop Status (PKT_DRP_STS) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.
10	RO	1'h0	RSV_1 (RSV_1) Reserved
9	RW/1C	1'h0	Buffer Not Available) Interrupt (BNA_INTR) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done.
8	RW/1C	1'h0	OUT Packet Error (OUT_PKT_ERR) Applies to OUT endpoints Only This interrupt is valid only when thresholding is enabled. This interrupt is asserted when the core detects an overflow or a CRC error for non-Isochronous OUT packet.
7	RO	1'h0	RSV (RSV) Reserved



Bits	Access Type	Default	Description
6	RW/1C	1'h0	Back-to-Back SETUP Packets Received (BAC2BACK_SETUP) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint.
5	RW/1C	1'h0	Status Phase Received for Control Write (STS_PHSE_RCVD) This interrupt is valid only for Control OUT endpoints and only in Scatter Gather DMA mode. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in Case of Scatter Gather DMA mode.
4	RW/1C	1'h0	OUT Token Received When Endpoint Disabled (OUT_TKN_EP_DIS) Applies only to control OUT endpoints. Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received.
3	RW/1C	1'h0	Setup Phase Done (SET_UP) Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet.
2	RW/1C	1'h0	AHB Error (AHB_ERR) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address.
1	RW/1C/V/L	1'h0	Endpoint Disabled Interrupt (EP_DISBLD) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.



Bits	Access Type	Default	Description
0	RW/1C	1'h0	Transfer Completed Interrupt (XFER_COMPL) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled: - For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. - For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is Set. When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint.

DOEPCTLn (DOEPCTLn [1..3])

Device OUT End Point Control Register n

MEM Offset (B0050000)	[0]:0B20h [1]:0B40h [2]:0B60h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 147. Detailed Description of DOEPCTLn (DOEPCTLn [1..3])

Bits	Access Type	Default	Description
31	RW/O	1'h0	Endpoint Enable (EP_ENA) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, for IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. For OUT endpoints it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is disabled such as for buffer-pointer based DMA mode: - For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. - For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. - The core clears this bit before setting any of the following interrupts on this endpoint: SETUP Phase Done Endpoint Disabled Transfer Completed Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory.



Bits	Access Type	Default	Description
30	RW/O	1'h0	Endpoint Disable (EP_DIS) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.
29	WO	1'h0	Set DATA1 PID (SETD1PID) Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode.
28	WO	1'h0	Set DATA0 PID (SETD0PID) Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode.
27	WO	1'h0	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also Set this bit for an endpoint after a SETUP packet is received on that endpoint
26	WO	1'h0	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint.
25:22	RO	4'h0	RSV_2 (RSV_2)
21	RW/O	1'h0	STALL Handshake (STALL) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core.
20	RW	1'h0	Snoop Mode (SNP) Applies to OUT endpoints only. This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory
19:18	RW	2'h0	Endpoint Type (EP_TYPE) This is the transfer type supported by this logical endpoint. 2'b00: Control 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt



Bits	Access Type	Default	Description
17	RO	1'h0	NAK Status (NAK_STS) Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
16	RO	1'h0	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. 1'b0: DATA0 1'b1: DATA1 This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode.
15	RW/1S/V	1'h0	USB Active Endpoint (USB_ACT_EP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit.
14:11	RO	4'h0	RSV (RSV) Reserved
10:0	RW	11'h0	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes.

DOEPDMA_n (DOEPDMA_n [1..3])

Device OUT End Point DMA Address Register n

MEM Offset (B0050000)

[0]:0B34h [1]:0B54h [2]:0B74h

Security_PolicyGroup**IntelRsvd**

False

Size

32 bits

Default

0000_0000h

Table 148. Detailed Description of DOEPDMA_n (DOEPDMA_n [1..3])

Bits	Access Type	Default	Description
31:0	RW	32'h0	DMA Address (DMA_ADDR) Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list.

DOEPTSIZE_n (DOEPTSIZE_n [1..3])

Device OUT Size Register n

MEM Offset (B0050000)	[0]:0B30h [1]:0B50h [2]:0B70h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 149. Detailed Description of DOEPTSIZE_n (DOEPTSIZE_n [1..3])

Bits	Access Type	Default	Description
31	RO	1'h0	RSV (RSV) Reserved
30:29	RO	2'h0	RX_DPID (RX_DPID) For isochronous OUT endpoints: This is the data PID (RX_DPID) received in the last packet for this endpoint. 2'b00: DATA0 2'b01: DATA2 2'b10: DATA1 2'b11: MDATA For control OUT Endpoints: This field specifies the number of back-to-back SETUP data (SUP_CNT) packets the endpoint can receive: 2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets
28:19	RW	10'h0	Packet Count (PKT_CNT) This field is decremented to zero after a packet is written into the RxFIFO.



Bits	Access Type	Default	Description
18:0	RW	19'h0	Transfer Size (XFER_SIZE_WIDTH) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from the RxFIFO and written to the external memory.

PCGCCTL

Power and Clock Gating Control Register

MEM Offset (B0050000)	E00h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 150. Detailed Description of PCGCCTL

Bits	Access Type	Default	Description
31:8	RO	24'h0	RSV_2 (RSV_2) Reserved
7	RO	1'h0	L1 Sleep (L1_SUSPENDED) Indicates that the PHY is in Sleep when in L1 state.
6	RO	1'h0	PHY In Sleep (PHY_SLEEP) Indicates that the PHY is in Sleep State.
5:4	RO	2'h0	RSV_1 (RSV_1) Reserved
3	RW	1'h0	Reset Power-Down Modules (RST_PDWN_MODULE) This bit is valid only in Partial Power-Down mode. The application sets this bit when the power is turned off. The application clears this bit after the power is turned on and the PHY clock is up. Note: The R/W of all core registers are possible only when this bit is set to 1'b0.
2:1	RO	2'h0	RSV (RSV) Reserved
0	RW	1'h0	IN Endpoint TxFIFO Space Avail (STOP_PCLK) The application sets this bit to stop the PHY clock (phy_clk) when the USB is suspended, the session is not valid, or the device is disconnected. The application clears this bit when the USB is resumed or a new session starts.



16 I²C

The Intel® Quark™ SE Microcontroller C1000 implements two instances of an I²C controller. Both 7 bit and 10 bit addressing modes are supported.

16.1 Signal Descriptions

I²C is a two-wire bus for inter-IC communication. Data and clock signals carry information between the connected devices. The following is the I²C Interface. The Intel® Quark™ SE Microcontroller C1000 supports two I²C interfaces for general purpose to control external devices.

Please see [Chapter 2, “Physical Interfaces”](#) for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction:** The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in [Chapter 4, “Electrical Characteristics”](#).
- **Description:** A brief explanation of the signal's function

Table 151. Memory 0 Signals

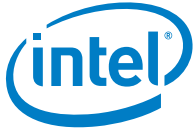
Signal Name	Direction/ Type	Description
I2C_M_0_CLK	I/O	I2C Serial Clock: <i>Signal Description</i>
I2C_M_0_DATA	I/O	I2C Serial Data: <i>Signal Description</i>

Table 152. Memory 1 Signals

Signal Name	Direction/ Type	Description
I2C_M_1_CLK	I/O	I2C Serial Clock: <i>Signal Description</i>
I2C_M_1_DATA	I/O	I2C Serial Data: <i>Signal Description</i>

16.2 Features

The following is a list of the I²C features:



16.2.1 I²C Protocol

The I²C bus is a two-wire serial interface, consisting of a serial data line and a serial clock. These wires carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a “transmitter” or “receiver,” depending on the function of the device. Devices are considered slaves when performing data transfers, as the Intel® Quark™ SE Microcontroller C1000 will always be a Master. A master is a device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

- Two I²C Interfaces
- Supports both Master and Slave operation
- Operational speeds:
 - Standard Mode (0 to 100 Kbps)
 - Fast Mode (≤ 400 Kbps)
 - Fast Mode Plus (≤ 1 Mbps)
- 7 bit or 10 bit Addressing
- Supports clock stretching by slave devices
- Multi-master arbitration
- Spike suppression
- Hardware handshake interface to support DMA capability
- Interrupt control
- FIFO support with 16B deep RX and TX FIFOs

16.2.2 I²C Modes of Operation

The I²C module can operate in the following modes:

- Standard mode (with a bit rate up to 100 Kb/s)
- Fast mode (with a bit rate up to 400 Kb/s)
- Fast-mode Plus (Fm+, with a bit rate up to 1 Mb/s)

The I²C can communicate with devices only using these modes as long as they are attached to the bus. Additionally, high speed mode, fast mode plus, and fast mode devices are downward compatible.

- High-speed mode devices can communicate with fast mode and standard mode devices in a mixed speed bus system.
- Fast mode devices can communicate with standard mode devices in a 0–100 Kb/s I²C bus system.

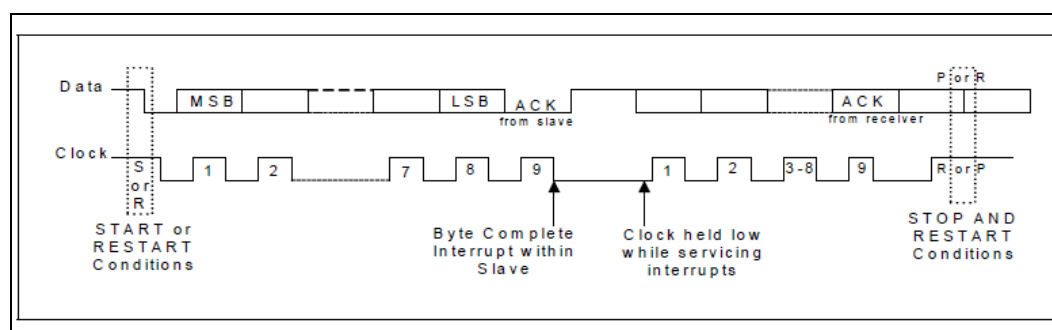


However, according to the I²C specification, standard mode devices are not upward compatible and should not be incorporated in a fast-mode I²C bus system since they cannot follow the higher transfer rate and unpredictable states would occur.

16.2.3 Functional Description

- The I²C master is responsible for generating the clock and controlling the transfer of data.
- The slave is responsible for either transmitting or receiving data to and from the master.
- The acknowledgement of data is sent by the device that is receiving data, which can be either a master or a slave.
- Each slave has a unique address that is determined by the system designer
 - When a master wants to communicate with a slave, the master transmits a START/RESTART condition that is then followed by the slave's address and a control bit (R/W), to determine if the master wants to transmit data or receive data from the slave.
 - The slave then sends an acknowledgment (ACK) pulse after the address.
- If the master (master-transmitter) is writing to the slave (slave-receiver):
 - The receiver gets one byte of data.
 - This transaction continues until the master terminates the transmission with a STOP condition.
- If the master is reading from a slave (master-receiver):
 - The slave transmits (slave-transmitter) a byte of data to the master, and the master then acknowledges the transaction with the ACK pulse.
 - This transaction continues until the master terminates the transmission by not acknowledging (NACK) the transaction after the last byte is received, and then the master issues a STOP condition or addresses another slave after issuing a RESTART condition. This behavior is illustrated in the following figure.

Figure 18. I²C Protocol



16.2.4 START and STOP Conditions

When the bus is idle, both the clock and data signals are pulled high through external pull-up resistors on the bus.

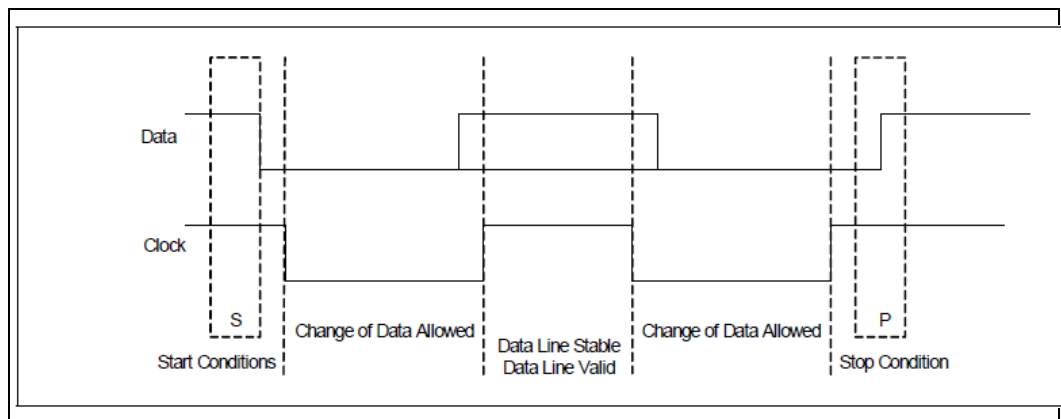
When the master wants to start a transmission on the bus, the master issues a START condition. This is defined to be a high-to-low transition of the data signal while the clock is high.

When the master wants to terminate the transmission, the master issues a STOP condition. This is defined to be a low-to-high transition of the data line while the clock is high.

The following figure shows the timing of the START and STOP conditions.

When data is being transmitted on the bus, the data line must be stable when the clock is high.

Figure 19. I²C Start and Stop Conditions



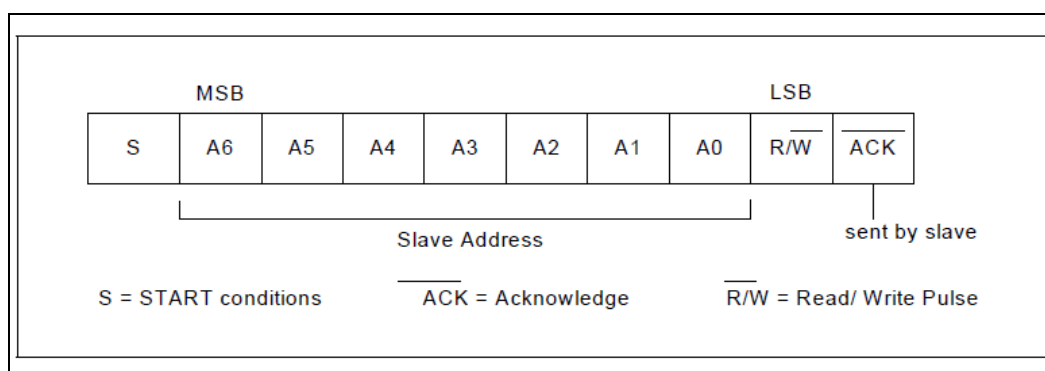
The signal transitions for the START/STOP conditions, as depicted in the previous figure, reflect those observed at the output of the master driving the I²C bus. Care should be taken when observing the data/clock signals at the input of the slave(s), because unequal line delays may result in an incorrect data/clock timing relationship.

16.2.5 Addressing Slave Protocol

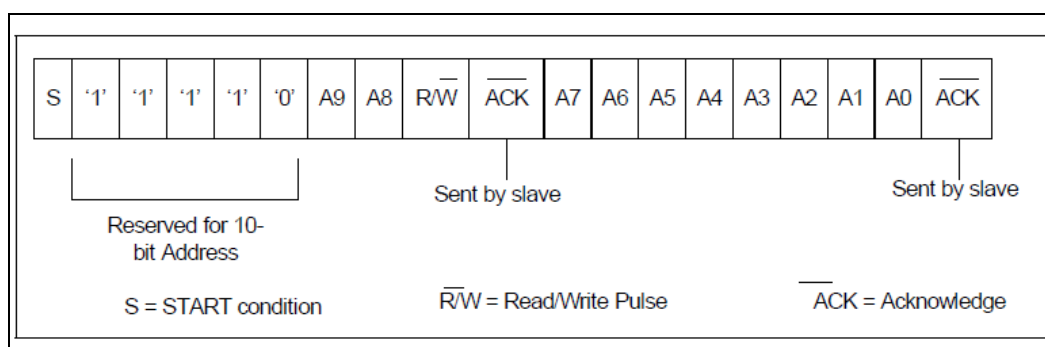
There are two address formats: 7-bit and 10-bit.

7-bit Address Format

- During the seven-bit address format, the first seven bits (bits 7:1) of the first byte set the slave address and the LSB bit (bit 0) is the R/W bit as shown in [Figure 20](#).
- When bit 0 (R/W) is set to 0, the master writes to the slave. When bit 0 (R/W) is set to 1, the master reads from the slave.

Figure 20: I²C 7-bit Addressing**10-Bit Address Format**

- During 10-bit addressing, 2 bytes are transferred to set the 10-bit address. The transfer of the first byte contains the following bit definition.
 - The first five bits (bits 7:3) notify the slaves that this is a 10-bit transfer. The next two bits (bits 2:1) set the slaves address bits 9:8, and the LSB bit (bit 0) is the RW bit.
 - The second byte transferred sets bits 7:0 of the slave address.
 - The following figure shows the 10-bit address format, and the following table defines the special purpose and reserved first byte addresses.

Figure 21. I²C 10-Bit AddressingTable 153. I²C Special Purpose First Byte Addresses

Slave Address	RW Bit	Description
0000 000	0	General Call Address: The I2C controller places the data in the receive buffer and issues a General Call Interrupt
0000 000	1	START byte: For more information, see the I2C bus specification section 3.15.
0000 001	X	CBUS address: I2C controller ignores these accesses.

Slave Address	RW Bit	Description
0000 010	X	Reserved
0000 011	X	Reserved
0000 1XX	X	High-speed master code
1111 1XX	X	Reserved
1111 0XX	X	Ten (10)-bit slave addressing

16.2.6 Transmit and Receive Protocol

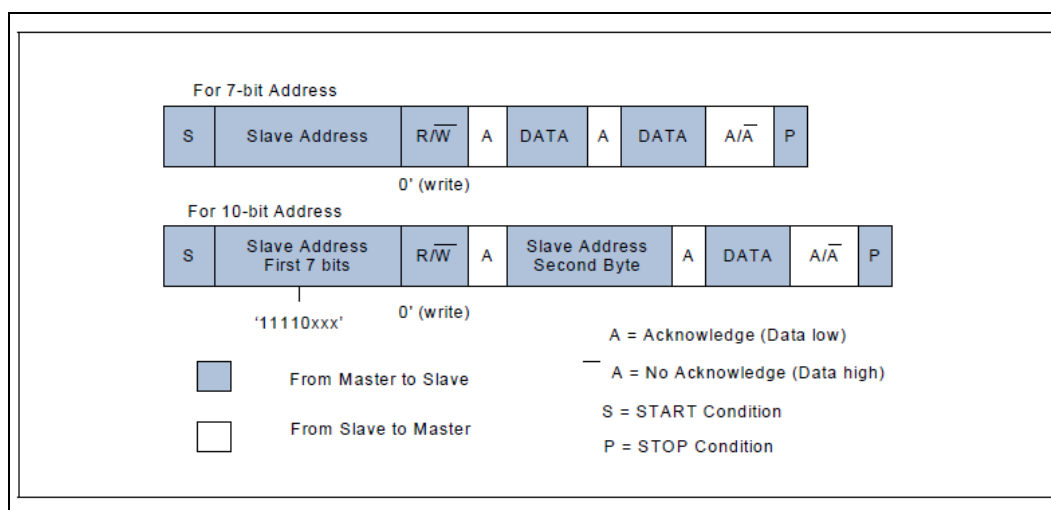
The master can initiate data transmission and reception to/from the bus, acting as either a master-transmitter or master-receiver. A slave responds to requests from the master by either transmitting data or receiving data to/from the bus, acting as either a slave-transmitter or slave-receiver, respectively.

Master-Transmitter and Slave-Receiver

All data is transmitted in byte format, with no limit on the number of bytes transferred per data transfer. After the master sends the address and RW bit or the master transmits a byte of data to the slave, the slave-receiver must respond with the acknowledge signal (ACK). When a slave-receiver does not respond with an ACK pulse, the master aborts the transfer by issuing a STOP condition. The slave must leave the data line high so that the master can abort the transfer.

If the master-transmitter is transmitting data as shown in the following figure, then the slave receiver responds to the master-transmitter with an acknowledgment pulse after every byte of data is received.

Figure 22. Master Slave Request

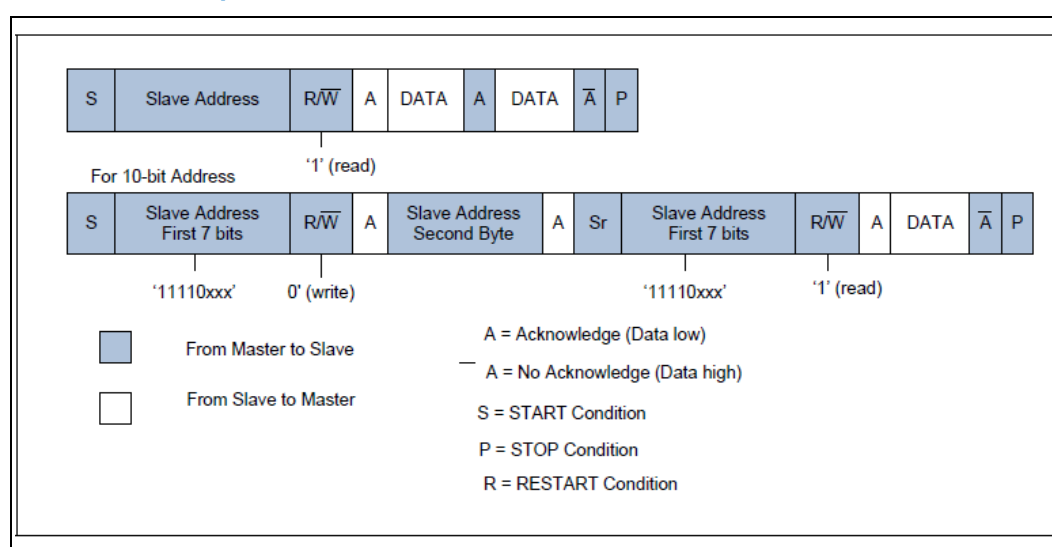


Master-Receiver and Slave-Transmitter

If the master is receiving data as shown in the following figure, the master responds to the Slave-Transmitter with an acknowledge pulse after a byte of data has been received, except for the last byte. This is the way the Master-Receiver notifies the Slave-Transmitter that this is the last byte. The Slave-Transmitter relinquishes the data line after detecting the No Acknowledge (NACK) so that the master can issue a STOP condition.

When a master does not want to relinquish the bus with a STOP condition, the master can issue a RESTART condition. This is identical to a START condition except it occurs after the ACK pulse. The master can then communicate with the same slave or a different slave.

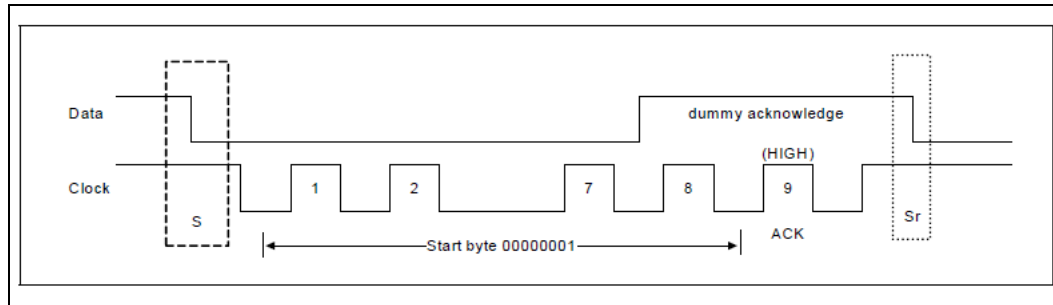
Figure 23. Master Slave Response



16.2.7 START BYTE Transfer Protocol

The START BYTE Transfer protocol is set up for systems that do not have an on-board dedicated I2C hardware module. When the I2C controller is a master, it supports the generation of START BYTE transfers at the beginning of every transfer in case a slave device requires it. This protocol consists of 7 '0's being transmitted followed by a 1, as illustrated in the following figure. This allows the processor that is polling the bus to under-sample the address phase until 0s are detected. Once the microcontroller detects a 0, it switches from the under sampling rate to the correct rate of the master.

Figure 24. Start Byte Operation



The START BYTE procedure is as follows:

1. Master generates a START condition.
2. Master transmits the START byte (0000 0001).
3. Master transmits the ACK clock pulse. (Present only to conform with the byte handling format used on the bus.)
4. No slave sets the ACK signal to 0.
5. Master generates a RESTART (R) condition.

A hardware receiver does not respond to the START BYTE because it is a reserved address and resets after the RESTART condition is generated.

16.3 I2C Modes and usage

16.3.1 Master Mode Operation

To use the I²C controller as a master, perform the following steps:

1. Disable the I²C controller by writing 0 (zero) to IC_ENABLE.ENABLE.
2. Write to the IC_CON register to set the maximum speed mode supported for slave operation IC_CON.SPEED and to specify whether the I²C controller starts its transfers in 7/10 bit addressing mode when the device is a slave (IC_CON.IC_10BITADDR_SLAVE).
3. Write to the IC_TAR register the address of the I²C device to be addressed. It also indicates whether a General Call or a START BYTE command is going to be performed by I²C. The desired speed of the I²C controller master-initiated transfers, either 7-bit or 10-bit addressing, is controlled by the IC_TAR.IC_10BITADDR_MASTER bit field.
4. Write to the IC_HS_MADDR register the desired master code for the I²C controller. The master code is programmer-defined.
5. Enable the I²C controller by writing a 1 in IC_ENABLE.
6. Now write the transfer direction and data to be sent to the IC_DATA_CMD register. If the IC_DATA_CMD register is written before the I²C controller is enabled, the data



and commands are lost as the buffers are kept cleared when the I2C controller is not enabled.

The I2C controller supports dynamic updating of the IC_TAR.IC_TAR and IC_TAR.IC_10BITADDR_MASTER. The IC_TAR register can be dynamically written to providing the following conditions are met:

- The I2C controller is not enabled (IC_ENABLE.ENABLE=0)
- The I2C controller is enabled (IC_ENABLE.ENABLE=1); AND the I2C controller is NOT engaged in any Master (tx, rx) operation (IC_STATUS.MST_ACTIVITY=0); AND the I2C controller is enabled to operate in Master mode (IC_CON.MASTER_MODE=1); AND there are NO entries in the TX FIFO (IC_STATUS.TFE=1).

The I2C controller supports switching back and forth between reading and writing dynamically. To transmit data, write the data to be written to the lower byte of the I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD). The IC_DATA_CMD.CMD should be written to 0 for I2C write operations. Subsequently, a read command may be issued by writing "don't cares" to IC_DATA_CMD.DAT register bits, and a 1 should be written to the IC_DATA_CMD.CMD bit.

16.3.2 Slave Mode Operation

To use the the I2C controller as a slave, perform the following steps:

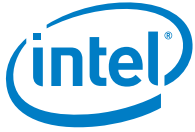
1. Disable the I2C controller by writing 0 (zero) to IC_ENABLE.ENABLE.
2. Write to the IC_SAR register (bits 9:0) to set the slave address. This is the address to which I2C controller responds. Refer to "[Chapter 15.4 Memory Mapped IO Registers](#)"
3. Write to the IC_CON register to specify which type of addressing is supported (7- or 10-bit by setting bit 3). Enable the I2C controller in slave-only mode by writing a '0' into bit 6 (IC_SLAVE_DISABLE) and a '0' to bit 0 (MASTER_MODE).
4. Enable the I2C controller by writing a '1' in bit 0 of the IC_ENABLE register.

Note: Slaves and masters do not have to be programmed with the same type of addressing 7- or 10-bit address. For instance, a slave can be programmed with 7-bit addressing and a master with 10-bit addressing, and vice versa.

16.3.3 Disabling the I2C Controller

The register IC_ENABLE allows software to unambiguously determine when the hardware has completely shutdown in response to the IC_ENABLE.ENABLE register being cleared from 1 to 0.

Procedure



1. Define a timer interval (ti2c_poll) equal to 10 times the signalling period for the highest I²C transfer speed used in the system and supported by the I2C controller. For example, if the highest I2C transfer mode is 400Kb/s, then this ti2c_poll is 25 us.
2. Define a maximum time-out parameter, MAX_T_POLL_COUNT, such that if any repeated polling operation exceeds this maximum value, an error is reported.
3. Execute a blocking thread/process/function that prevents any further I²C master transactions to be started by software, but allows any pending transfers to be completed.
4. The variable POLL_COUNT is initialized to zero (0).
5. Clear IC_ENABLE.ENABLE to zero (0).
6. Read the IC_ENABLE_STATUS.IC_EN bit. Increment POLL_COUNT by one. If POLL_COUNT >= MAX_T_POLL_COUNT, exit with the relevant error code.
7. If IC_ENABLE_STATUS.IC_EN is 1, then sleep for ti2c_poll and proceed to the previous step. Otherwise, exit with a relevant success code.

16.4 Memory Mapped IO Registers

Registers listed are for I²C 0, starting at base address B0002800h. I²C 1 contains the same registers starting at base address B0002C00h. same registers. Differences between the I²Cs are noted in individual registers.

Table 154. Summary of I²C Registers—0xB0002800

MEM Address	Default	Instance Name	Name
0x0	0000_007Fh	IC_CON	Control Register
0x4	0000_2055h	IC_TAR	Master Target Address
0x8	0000_0055h	IC_SAR	Slave Address
0xC	0000_0001h	IC_HS_MADDR	High Speed Master ID
0x10	0000_0000h	IC_DATA_CMD	Data Buffer and Command
0x14	0000_0190h	IC_SS_SCL_HCNT	Standard Speed Clock SCL High Count
0x18	0000_01D6h	IC_SS_SCL_LCNT	Standard Speed Clock SCL Low Count
0x1C	0000_003Ch	IC_FS_SCL_HCNT	Fast Speed Clock SCL High Count
0x20	0000_0082h	IC_FS_SCL_LCNT	Fast Speed I2C Clock SCL Low Count
0x24	0000_0006h	IC_HS_SCL_HCNT	High Speed I2C Clock SCL High Count
0x28	0000_0010h	IC_HS_SCL_LCNT	High Speed I2C Clock SCL Low Count
0x2C	0000_0000h	IC_INTR_STAT	Interrupt Status
0x30	0000_08FFh	IC_INTR_MASK	Interrupt Mask
0x34	0000_0000h	IC_RAW_INTR_STAT	Raw Interrupt Status
0x38	0000_000Fh	IC_RX_TL	Receive FIFO Threshold Level



MEM Address	Default	Instance Name	Name
0x3C	0000_0000h	IC_TX_TL	Transmit FIFO Threshold Level
0x40	0000_0000h	IC_CLR_INTR	Clear Combined and Individual Interrupt
0x44	0000_0000h	IC_CLR_RX_UNDER	Clear RX_UNDER Interrupt
0x48	0000_0000h	IC_CLR_RX_OVER	Clear RX_OVER Interrupt
0x4C	0000_0000h	IC_CLR_TX_OVER	Clear TX_OVER Interrupt
0x50	0000_0000h	IC_CLR_RD_REQ	Clear RD_REQ Interrupt
0x54	0000_0000h	IC_CLR_TX_ABRT	Clear TX_ABRT Interrupt
0x58	0000_0000h	IC_CLR_RX_DONE	Clear RX_DONE Interrupt
0x5C	0000_0000h	IC_CLR_ACTIVITY	Clear ACTIVITY Interrupt
0x60	0000_0000h	IC_CLR_STOP_DET	Clear STOP_DET Interrupt
0x64	0000_0000h	IC_CLR_START_DET	Clear START_DET Interrupt
0x68	0000_0000h	IC_CLR_GEN_CALL	Clear GEN_CALL Interrupt
0x6C	0000_0000h	IC_ENABLE	Enable
0x70	0000_0006h	IC_STATUS	Status
0x74	0000_0000h	IC_TXFLR	Transmit FIFO Level
0x78	0000_0000h	IC_RXFLR	Receive FIFO Level
0x7C	0001_0001h	IC_SDA_HOLD	SDA Hold
0x80	0000_0000h	IC_TX_ABRT_SOURCE	Transmit Abort Source
0x88	0000_0000h	IC_DMA_CR	SDA Setup
0x8C	0000_0000h	IC_DMA_TDLR	DMA Transmit Data Level Register
0x90	0000_0000h	IC_DMA_RDLR	I2C Receive Data Level Register
0x94	0000_0064h	IC_SDA_SETUP	SDA Setup
0x98	0000_0001h	IC_ACK_GENERAL_CALL	General Call Ack
0x9C	0000_0000h	IC_ENABLE_STATUS	Enable Status
0xA0	0000_0007h	IC_FS_SPKLEN	SS and FS Spike Suppression Limit
0xF4	000F_0FAEh	IC_COMP_PARAM_1	Configuration Parameters. RSVD (Reserved)
0xF8	3131_352Ah	IC_COMP_VERSION	Component Version. RSVD (Reserved)
0xFC	4457_0140h	IC_COMP_TYPE	Component Type. RSVD (Reserved)

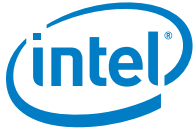
16.4.1 Control Register (IC_CON)

Used to control the I2C controller. Can be written only when the I2C is disabled (IC_ENABLE==0). Writes at other times have no effect.

MEM Offset (B0002800)
Security_PolicyGroup
IntelRsvd

0h

False



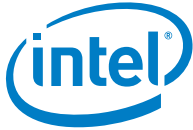
Size
Default

32 bits
0000_007Fh

Table 155. Detailed Description of Control Register (IC_CON)

Bits	Access Type	Default	Description
31:10	RO	22'b0	Reserved (RSV)
9	RW	1'b0	RX_FIFO_FULL_HLD_CTRL (RX_FIFO_FULL_HLD_CTRL) This bit controls whether DW_apb_i2c should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH, as described in the IC_RX_FULL_HLD_BUS_EN parameter. Dependencies: This register bit value is applicable only when the IC_RX_FULL_HLD_BUS_EN configuration parameter is set to 1. If IC_RX_FULL_HLD_BUS_EN = 0, then this bit is read-only. If IC_RX_FULL_HLD_BUS_EN = 1, then this bit can be read or write
8	RW	1'b0	TX_EMPTY_CTRL (TX_EMPTY_CTRL) This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register
7	RW	1'b0	STOP_DET_IFADDRESSED (STOP_DET_IFADDRESSED) In slave mode: 1b1 issues the STOP_DET interrupt only when it is addressed. 1b0 issues the STOP_DET irrespective of whether its addressed or not.
6	RW	1'b1	Slave Mode Disable (IC_SLAVE_DISABLE) This bit controls whether I2C has its slave disabled. If this bit is set (slave disabled), I2C controller functions only as a master. 0: slave is enabled 1: slave is disabled NOTE: Software must ensure slave and master mode are mutually exclusive. IMPORTANT: if IC_SLAVE_DISABLE == 0 --> MASTER_MODE == 0

Bits	Access Type	Default	Description
5	RW	1'b1	Restart Support (IC_RESTART_EN) Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several I2C controller operations. 0: disable 1: enable When RESTART is disabled, the master is prohibited from performing the following functions: - Change direction within a transfer (split) - Send a START BYTE - High-speed mode operation - Combined format transfers in 7-bit addressing modes - Read operation with a 10-bit address - Send multiple bytes per transfer By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple I2C transfers. If the above operations are performed, it will result in setting TX_ABORT of the IC_RAW_INTR_STAT register
4	RW	1'b1	Master Addressing Mode (IC_10BITADDR_MASTER) Controls whether the I2C controller starts its transfers in 7- or 10-bit addressing mode when acting as a master. 0: 7-bit addressing 1: 10-bit addressing
3	RW	1'b1	Slave Addressing Mode (IC_10BITADDR_SLAVE) When acting as a slave, this bit controls whether the I2C controller responds to 7- or 10-bit addresses. - 0: 7-bit addressing ignores transactions that involve 10-bit addressing; for 7-bit addressing, only the lower 7 bits of the IC_SAR register are compared - 1: 10-bit addressing responds to only 10-bit addressing transfers that match the full 10 bits of the IC_SAR register
2:1	RW	2'b11	Speed Mode (SPEED) I2C Master operational speed. Relevant only in master mode. 01: standard mode (100 kbit/s) 10: fast mode (400 kbit/s) 11: high speed mode (3.4 Mbit/s)
0	RW	1'b1	Master Mode Enable (MASTER_MODE) This bit controls whether the I2C master is enabled. 0: master disabled 1: master enabled NOTE: Software must ensure master and slave mode are mutually exclusive if MASTER_MODE == 1 --> IC_SLAVE_DISABLE == 1



16.4.2 Master Target Address (IC_TAR)

Can be written only when the I2C is disabled (IC_ENABLE==0). Writes at other times have no effect.

MEM Offset (B0002800)	4h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_2055h

Table 156. Detailed Description of Master Target Address (IC_TAR)

Bits	Access Type	Default	Description
31:13	RO	19'h00001	Reserved (RSV)
12	RW	1'b0	IC_10BITADDR_MASTER (IC_10BITADDR_MASTER) This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. 0: 7-bit addressing 1: 10-bit addressing
11	RW	1'b0	Special Command Enable (SPECIAL) This bit indicates whether software performs a General Call or START BYTE command. 0: ignore bit 10 GC_OR_START and use IC_TAR normally 1: perform special I2C command as specified in GC_OR_START field
10	RW	1'b0	Special Command Type (GC_OR_START) If IC_TAR bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call or START byte command is to be performed by the I2C Controller. 0: General Call Address after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. I2C controller remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. 1: START BYTE



Bits	Access Type	Default	Description
9:0	RW	10'h055	Master Target Address (IC_TAR) This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave. IMPORTANT: if MASTER_MODE == 1 --> IC_SLAVE_DISABLE == 1

16.4.3 Slave Address (IC_SAR)

Holds the slave address when the I2C is operating as a slave. Can be written only when the I2C is disabled (IC_ENABLE==0). Writes at other times have no effect

MEM Offset (B0002800)	8h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0055h

Table 157. Detailed Description of Slave Address (IC_SAR)

Bits	Access Type	Default	Description
31:10	RO	22'b0	Reserved (RSV)
9:0	RW	10'h055	Slave Address (IC_SAR) For 7-bit addressing, only IC_SAR[6:0] is used.

16.4.4 High Speed Master ID (IC_HS_MADDR)

I2C High Speed Master Mode Code Address. Can be written only when the I2C is disabled (IC_ENABLE==0). Writes at other times have no effect.

MEM Offset (B0002800)	0Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0001h

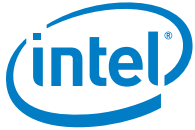


Table 158. Detailed Description of High Speed Master ID (IC_HS_MADDR)

Bits	Access Type	Default	Description
31:3	RO	29'b0	Reserved (RSV)
2:0	RW	3'b01	HS Master Code (IC_HS_MAR) This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high-speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7.

16.4.5 Data Buffer and Command (IC_DATA_CMD)

CPU writes to it when filling the TX FIFO and the reads from when retrieving bytes from RX FIFO.

MEM Offset (B0002800)	10h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

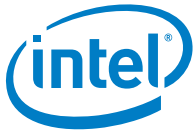
Table 159. Detailed Description of Data Buffer and Command (IC_DATA_CMD)

Bits	Access Type	Default	Description
31:11	RO	21'b0	Reserved (RSV)
10	RO	1'b0	Restart Bit Control (RESTART) This bit controls whether a RESTART is issued before the byte is sent or received. - 1 if IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. - 0 If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead

Bits	Access Type	Default	Description
9	RO	1'b0	Stop Bit Control (STOP) This bit controls whether a STOP is issued after the byte is sent or received: - 1 STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. - 0 STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.
8	RW	1'b0	Command (CMD) This bit controls whether a read or a write is performed. This bit controls the direction only in I2C master mode. 0 = Write 1 = Read When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a 'don't care' because writes to this register are not required. In slave-transmitter mode, a '0' indicates that CPU data is to be transmitted and as DAT or IC_DATA_CMD[7:0]. NOTE: when programming this bit, attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the IC_RAW_INTR_STAT register), unless bit 11 (SPECIAL) in the IC_TAR register has been cleared. If a '1' is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs. NOTE: It is possible that while attempting a master I2C read transfer, a RD_REQ interrupt may have occurred simultaneously due to a remote I2C master addressing I2C controller. In this type of scenario, the I2C controller ignores the IC_DATA_CMD write, generates a TX_ABRT interrupt, and waits to service the RD_REQ interrupt.
7:0	RW	8'b0	Data Buffer (DAT) Contains the data to be transmitted or received on the I2C bus. When writing to this register and want to perform a read, DAT field is ignored by the I2C controller. When reading this register, DAT return the value of data received on the I2C controller interface.

16.4.6 Standard Speed Clock SCL High Count (IC_SS_SCL_HCNT)

Sets the SCL clock high-period count for standard speed (SS). Can be written only when the I2C is disabled (IC_ENABLE==0). Writes at other times have no effect.



MEM Offset (B0002800) 14h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0190h

Table 160. Detailed Description of Standard Speed Clock SCL High Count (IC_SS_SCL_HCNT)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved (RSV)
15:0	RW	16'h0190	SS SCL clock high-period count (IC_SS_SCL_HCNT) Must be set before any I2C bus transaction can take place to ensure proper I/O timing. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. This register must not be programmed to a value higher than 65525, because I2C controller uses a 16-bit counter to flag an I2C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT + 10.

16.4.7 Standard Speed Clock SCL Low Count (IC_SS_SCL_LCNT)

Sets the SCL clock low-period count for standard speed (SS). Can be written only when the I2C is disabled (IC_ENABLE==0). Writes at other times have no effect.

MEM Offset (B0002800) 18h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_01D6h

Table 161. Detailed Description of Standard Speed Clock SCL Low Count (IC_SS_SCL_LCNT)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved (RSV)
15:0	RW	16'h01d6	SS SCL clock low-period count (IC_SS_SCL_LCNT) Must be set before any I2C bus transaction can take place to ensure proper I/O timing. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set.



16.4.8 Fast Speed Clock SCL High Count (IC_FS_SCL_HCNT)

Sets the SCL clock high-period count for fast speed (FS). Can be written only when the I²C is disabled (IC_ENABLE==0). Writes at other times have no effect.

MEM Offset (B0002800) 1Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_003Ch

Table 162. Detailed Description of Fast Speed Clock SCL High Count (IC_FS_SCL_HCNT)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved (RSV)
15:0	RW	16'h003c	FS SCL clock high-period count (IC_FS_SCL_HCNT) Must be set before any I2C bus transaction can take place to ensure proper I/O timing. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set.

16.4.9 Fast Speed I2C Clock SCL Low Count (IC_FS_SCL_LCNT)

Sets the SCL clock low-period count for fast speed (FS). Can be written only when the I2C is disabled (IC_ENABLE==0). Writes at other times have no effect.

MEM Offset (B0002800) 20h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0082h

Table 163. Detailed Description of Fast Speed I2C Clock SCL Low Count (IC_FS_SCL_LCNT)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved (RSV)
15:0	RW	16'h0082	SS SCL clock low-period count (IC_FS_SCL_LCNT) Must be set before any I2C bus transaction can take place to ensure proper I/O timing. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set.



16.4.10 High Speed I²C Clock SCL High Count (IC_HS_SCL_HCNT)

Sets the SCL clock high-period count for high speed (HS). Can be written only when the I²C is disabled (IC_ENABLE==0). Writes at other times have no effect.

MEM Offset (B0002800)	24h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0006h

Table 164. Detailed Description of High Speed I²C Clock SCL High Count (IC_HS_SCL_HCNT)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved (RSV)
15:0	RW	16'h0006	HS SCL clock high-period count (IC_HS_SCL_HCNT) Must be set before any I2C bus transaction can take place to ensure proper I/O timing. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set.

16.4.11 High Speed I²C Clock SCL Low Count (IC_HS_SCL_LCNT)

Sets the SCL clock low-period count for high speed (HS). Can be written only when the I²C is disabled (IC_ENABLE==0). Writes at other times have no effect.

MEM Offset (B0002800)	28h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0010h

Table 165. Detailed Description of High Speed I²C Clock SCL Low Count (IC_HS_SCL_LCNT)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved (RSV)
15:0	RW	16'h0010	SS SCL clock low-period count (IC_HS_SCL_LCNT) Must be set before any I2C bus transaction can take place to ensure proper I/O timing. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set.



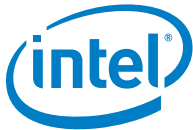
16.4.12 Interrupt Status (IC_INTR_STAT)

Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register

MEM Offset (B0002800)	2Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 166. Detailed Description of Interrupt Status (IC_INTR_STAT)

Bits	Access Type	Default	Description
31:13	RO	19'b0	Reserved (RSV)
12	RW	1'b1	M_RESTART_DET Mask (M_RESTART_DET) This bit masks the R_RESTART_DET interrupt status bit in the IC_INTR_STAT register.
11	RO	1'b1	General Call Acknowledged (R_GEN_CALL) Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling the I2C controller or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register. I2C controller stores the received data in the Rx buffer
10	RO	1'b0	Start Detected (R_START_DET) Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether the controller is operating in slave or master mode
9	RO	1'b0	Stop Detected (R_STOP_DET) Indicates whether a STOP condition has occurred on the I2C interface regardless of whether the controller is operating in slave or master mode.
8	RO	1'b0	Activity (R_ACTIVITY) This bit captures I2C controller activity and stays set until it is cleared. There are four ways to clear it: - Disabling the controller - Reading the IC_CLR_ACTIVITY register - Reading the IC_CLR_INTR register - System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the controller is idle, this bit remains set until cleared, indicating that there was activity on the bus



Bits	Access Type	Default	Description
7	RO	1'b0	RX Completed (R_RX_DONE) When the I2C controller is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done
6	RO	1'b0	TX Abort (R_TX_ABORT) This bit indicates if the I2C controller, in transmitter mode, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a 'transmit abort'. When this bit is set to 1, the IC_TX_ABORT_SOURCE register indicates the reason why the transmit abort takes places. NOTE: The controller flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register IC_CLR_TX_ABORT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes for transmission
5	RO	1'b0	Read Requested (R_RD_REQ) This bit is set to 1 when I2C controller is acting as a slave and another I2C master is attempting to read data from it. The controller holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the IC_DATA_CMD register. This bit is set to 0 just after the processor reads the IC_CLR_RD_REQ register
4	RO	1'b0	TX Empty (R_TX_EMPTY) This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When the IC_ENABLE bit 0 is 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with ic_en=0, this bit is set to 0. Reset value
3	RO	1'b0	TX Overflow (R_TX_OVER) Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared
2	RO	1'b0	RX Full (R_RX_FULL) Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (IC_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the IC_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues

Bits	Access Type	Default	Description
1	RO	1'b0	RX Overflow (R_RX_OVER) Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The I2C Controller acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.
0	RO	1'b0	RX Underflow (R_RX_UNDER) Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.

16.4.13 Interrupt Mask (IC_INTR_MASK)

These bits mask their corresponding interrupt status bits. They are active high; a value of 0 prevents a bit from generating an interrupt.

MEM Offset (B0002800)	30h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_08FFh

Table 167. Detailed Description of Interrupt Mask (IC_INTR_MASK)

Bits	Access Type	Default	Description
31:12	RO	19'b0	Reserved (RSV)
12	RW	1'b1	M_RESTART_DET Mask (M_RESTART_DET) This bit masks the R_RESTART_DET interrupt status bit in the IC_INTR_STAT register.
11	RW	1'b1	General Call Acknowledged Mask (M_GEN_CALL) Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling the I2C controller or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register. I2C controller stores the received data in the Rx buffer
10	RW	1'b0	Start Detected Mask (M_START_DET) Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether the controller is operating in slave or master mode



Bits	Access Type	Default	Description
9	RW	1'b0	Stop Detected Mask (M_STOP_DET) Indicates whether a STOP condition has occurred on the I2C interface regardless of whether the controller is operating in slave or master mode.
8	RW	1'b0	Activity Mask (M_ACTIVITY) This bit captures I2C controller activity and stays set until it is cleared. There are four ways to clear it: - Disabling the controller - Reading the IC_CLR_ACTIVITY register - Reading the IC_CLR_INTR register - System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the controller is idle, this bit remains set until cleared, indicating that there was activity on the bus
7	RW	1'b1	RX Completed Mask (M_RX_DONE) When the I2C controller is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done
6	RW	1'b1	TX Abort Mask (M_TX_ABORT) This bit indicates if the I2C controller, in transmitter mode, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a 'transmit abort'. When this bit is set to 1, the IC_TX_ABORT_SOURCE register indicates the reason why the transmit abort takes places. NOTE: The controller flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register IC_CLR_TX_ABORT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes for transmission
5	RW	1'b1	Read Requested Mask (M_RD_REQ) This bit is set to 1 when I2C controller is acting as a slave and another I2C master is attempting to read data from it. The controller holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the IC_DATA_CMD register. This bit is set to 0 just after the processor reads the IC_CLR_RD_REQ register
4	RW	1'b1	TX Empty Mask (M_TX_EMPTY) This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When the IC_ENABLE bit 0 is 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with ic_en=0, this bit is set to 0. Reset value

Bits	Access Type	Default	Description
3	RW	1'b1	TX Overflow Mask (M_TX_OVER) Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared
2	RW	1'b1	RX Full Mask (M_RX_FULL) Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (IC_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the IC_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues
1	RW	1'b1	RX Overflow Mask (M_RX_OVER) Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The I2C Controller acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.
0	RW	1'b1	RX Underflow Mask (M_RX_UNDER) Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.

16.4.14 Raw Interrupt Status (IC_RAW_INTR_STAT)

Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the I²C controller

MEM Offset (B0002800)	34h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 168. Detailed Description of Raw Interrupt Status (IC_RAW_INTR_STAT)

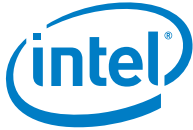
Bits	Access Type	Default	Description
31:12	RO	20'b0	Reserved (RSV)
12	RO	1'b0	R_RESTART_DET



Bits	Access Type	Default	Description
11	RO	1'b0	General Call Acknowledged (GEN_CALL) Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling the I2C controller or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register. I2C controller stores the received data in the Rx buffer
10	RO	1'b0	Start Detected (START_DET) Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether the controller is operating in slave or master mode
9	RO	1'b0	Stop Detected (STOP_DET) Indicates whether a STOP condition has occurred on the I2C interface regardless of whether the controller is operating in slave or master mode.
8	RO	1'b0	Activity (ACTIVITY) This bit captures I2C controller activity and stays set until it is cleared. There are four ways to clear it: - Disabling the controller - Reading the IC_CLR_ACTIVITY register - Reading the IC_CLR_INTR register - System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the controller is idle, this bit remains set until cleared, indicating that there was activity on the bus
7	RO	1'b0	RX Completed (RX_DONE) When the I2C controller is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done
6	RO	1'b0	TX Abort (TX_ABRT) This bit indicates if the I2C controller, in transmitter mode, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a 'transmit abort'. When this bit is set to 1, the IC_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. NOTE: The controller flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register IC_CLR_TX_ABRT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes for transmission



Bits	Access Type	Default	Description
5	RO	1'b0	Read Requested (RD_REQ) This bit is set to 1 when I2C controller is acting as a slave and another I2C master is attempting to read data from it. The controller holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the IC_DATA_CMD register. This bit is set to 0 just after the processor reads the IC_CLR_RD_REQ register
4	RO	1'b0	TX Empty (TX_EMPTY) This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When the IC_ENABLE bit 0 is 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with ic_en=0, this bit is set to 0. Reset value
3	RO	1'b0	TX Overflow (TX_OVER) Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared
2	RO	1'b0	RX Full (RX_FULL) Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (IC_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the IC_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues
1	RO	1'b0	RX Overflow (RX_OVER) Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The I2C Controller acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.
0	RO	1'b0	RX Underflow (RX_UNDER) Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.



16.4.15 Receive FIFO Threshold Level (IC_RX_TL)

Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in IC_RAW_INTR_STAT register)

MEM Offset (B0002800)	38h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_000Fh

Table 169. Detailed Description of Receive FIFO Threshold Level (IC_RX_TL)

Bits	Access Type	Default	Description
31:4	RO	28'b0	Reserved (RSV)
3:0	RW	4'hF	Receive FIFO Threshold Level (RX_TL) The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries

16.4.16 Transmit FIFO Threshold Level (IC_TX_TL)

Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register).

MEM Offset (B0002800)	3Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 170. Detailed Description of Transmit FIFO Threshold Level (IC_TX_TL)

Bits	Access Type	Default	Description
31:4	RO	28'b0	Reserved (RSV)
3:0	RW	4'h0	Transmit FIFO Threshold Level (TX_TL) The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries



16.4.17 Clear Combined and Individual Interrupt (IC_CLR_INTR)

Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register.

MEM Offset (B0002800)	40h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 171. Detailed Description of Clear Combined and Individual Interrupt (IC_CLR_INTR)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)
0	RO	1'b0	Clear Combined and Individual Interrupt (CLR_INTR) This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE

16.4.18 Clear RX_UNDER Interrupt (IC_CLR_RX_UNDER)

Clear a single interrupt type

MEM Offset (B0002800)	44h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

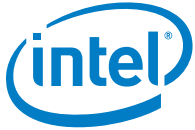
Table 172. Detailed Description of Clear RX_UNDER Interrupt (IC_CLR_RX_UNDER)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)
0	RO	1'b0	Clear RX_UNDER (CLR_RX_UNDER) Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT

16.4.19 Clear RX_OVER Interrupt (IC_CLR_RX_OVER)

Clear a single interrupt type

MEM Offset (B0002800)	48h



Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 173. Detailed Description of Clear RX_OVER Interrupt (IC_CLR_RX_OVER)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)
0	RO	1'b0	Clear RX_OVER (CLR_RX_OVER) Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT

16.4.20 Clear TX_OVER Interrupt (IC_CLR_TX_OVER)

Clear a single interrupt type

MEM Offset (B0002800) 4Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 174. Detailed Description of Clear TX_OVER Interrupt (IC_CLR_TX_OVER)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)
0	RO	1'b0	Clear TX_OVER (CLR_TX_OVER) Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT

16.4.21 Clear RD_REQ Interrupt (IC_CLR_RD_REQ)

Clear a single interrupt type

MEM Offset (B0002800) 50h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h



Table 175. Detailed Description of Clear RD_REQ Interrupt (IC_CLR_RD_REQ)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)
0	RO	1'b0	Clear RD_REQ (CLR_RD_REQ) Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT

16.4.22 Clear TX_ABRT Interrupt (IC_CLR_TX_ABRT)

Clear a single interrupt type

MEM Offset (B0002800)	54h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 176. Detailed Description of Clear TX_ABRT Interrupt (IC_CLR_TX_ABRT)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)
0	RO	1'b0	Clear TX_ABRT (CLR_TX_ABRT) Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE

16.4.23 Clear RX_DONE Interrupt (IC_CLR_RX_DONE)

Clear a single interrupt type

MEM Offset (B0002800)	58h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

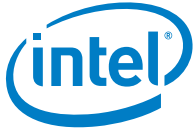


Table 177. Detailed Description of Clear RX_DONE Interrupt (IC_CLR_RX_DONE)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)
0	RO	1'b0	Clear RX_DONE (CLR_RX_DONE) Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT

16.4.24 Clear ACTIVITY Interrupt (IC_CLR_ACTIVITY)

Clear a single interrupt type

MEM Offset (B0002800)	5Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 178. Detailed Description of Clear ACTIVITY Interrupt (IC_CLR_ACTIVITY)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)
0	RO	1'b0	Clear ACTIVITY (CLR_TX_ABRT) Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT

16.4.25 Clear STOP_DET Interrupt (IC_CLR_STOP_DET)

Clear a single interrupt type

MEM Offset (B0002800)	60h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h


Table 179. Detailed Description of Clear STOP_DET Interrupt (IC_CLR_STOP_DET)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)
0	RO	1'b0	Clear STOP_DET (CLR_STOP_DET) Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT

16.4.26 Clear START_DET Interrupt (IC_CLR_START_DET)

Clear a single interrupt type

MEM Offset (B0002800)	64h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 180. Detailed Description of Clear START_DET Interrupt (IC_CLR_START_DET)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)
0	RO	1'b0	Clear START_DET (CLR_START_DET) Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT

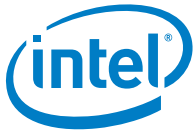
16.4.27 Clear GEN_CALL Interrupt (IC_CLR_GEN_CALL)

Clear a single interrupt type

MEM Offset (B0002800)	68h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 181. Detailed Description of Clear GEN_CALL Interrupt (IC_CLR_GEN_CALL)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)



Bits	Access Type	Default	Description
0	RO	1'b0	Clear GEN_CALL (CLR_GEN_CALL) Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT

16.4.28 Enable (IC_ENABLE)

Controls whether the I2C controller is enabled. Software can disable I2C controller while it is active.

MEM Offset (B0002800)	6Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 182. Detailed Description of Enable (IC_ENABLE)

Bits	Access Type	Default	Description
31:2	RO	30'b0	Reserved (RSV)
1	RW	1'b0	Abort I2C Controller (ABORT) The software can abort the I2C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation. When set, the controller initiates the transfer abort. 0: ABORT not initiated or ABORT done 1: ABORT operation in progress



Bits	Access Type	Default	Description
0	RW	1'b0	Enable I2C Controller (ENABLE) 0: Disabled (TX/RX FIFOs are held in an erased state) 1: Enabled NOTE: ensure that the controller is disabled properly. When disabled, the following occurs: - The TX FIFO and RX FIFO get flushed. - Status bits in the IC_INTR_STAT register are still active until the I2C Controller goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the controller stops the current transfer at the end of the current byte and does not acknowledge the transfer. There is a two I2C clocks delay when enabling or disabling the controller

16.4.29 Status (IC_STATUS)

Read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt.

- When the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register: bits 1 and 2 are set to 1, bits 3 and 4 are set to 0
- When the master or slave state machines goes to idle and ic_en=0: bits 5 and 6 are set to 0

MEM Offset (B0002800)	70h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0006h

Table 183. Detailed Description of Status (IC_STATUS)

Bits	Access Type	Default	Description
31:7	RO	25'b0	Reserved (RSV)
6	RO	1'b0	SLV_ACTIVITY (SLV_ACTIVITY) When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. 0: Slave FSM is in IDLE state so the Slave part is not Active 1: Slave FSM is not in IDLE state so the Slave part is Active

Bits	Access Type	Default	Description
5	RO	1'b0	Master FSM Activity Status (MST_ACTIVITY) When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. 0: Master FSM is in IDLE state so the Master part is not Active 1: Master FSM is not in IDLE state so the Master part is Active NOTE: IC_STATUS[0]-that is, ACTIVITY bit-is the OR of SLV_ACTIVITY and MST_ACTIVITY bits
4	RO	1'b0	Receive FIFO Completely Full (RFF) When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0: Receive FIFO is not full 1: Receive FIFO is full
3	RO	1'b0	Receive FIFO Not Empty (RFNE) This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. 0: Receive FIFO is empty 1: Receive FIFO is not empty
2	RO	1'b1	Transmit FIFO Completely Empty (TFE) When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty
1	RO	1'b1	Transmit FIFO Not Full (TFNF) Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0: Transmit FIFO is full 1: Transmit FIFO is not full
0	RO	1'b0	Activity (ACTIVITY) Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. 0: Receive FIFO is empty 1: Receive FIFO is not empty

16.4.30 Transmit FIFO Level (IC_TXFLR)

Contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever: - The I2C is disabled - There is a transmit abort that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register - The slave bulk transmit mode is aborted. The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO



MEM Offset (B0002800) 74h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 184. Detailed Description of Transmit FIFO Level (IC_TXFLR)

Bits	Access Type	Default	Description
31:5	RO	27'b0	Reserved (RSV)
4:0	RO	5'b0	Transmit FIFO Level (TXFLR) Contains the number of valid data entries in the transmit FIFO

16.4.31 Receive FIFO Level (IC_RXFLR)

Read this register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever: - The I2C is disabled - Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABORT_SOURCE. The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO

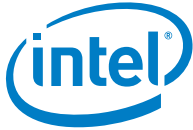
MEM Offset (B0002800) 78h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 185. Detailed Description of Receive FIFO Level (IC_RXFLR)

Bits	Access Type	Default	Description
31:5	RO	27'b0	Reserved (RSV)
4:0	RO	5'b0	Receive FIFO Level (RXFLR) Contains the number of valid data entries in the receive FIFO

16.4.32 SDA Hold (IC_SDA_HOLD)

This register controls the amount of hold time on the SDA signal after a negative edge of SCL line in units of I2C clock period. The value programmed must be greater than the minimum hold time in each mode for the value to be implemented: 1 cycle in master, 7 cycles in slave mode. Writes to this register succeed only when I2C controller is disabled (IC_ENABLE=0)



MEM Offset (B0002800) 7Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0001_0001h

Table 186. Detailed Description of SDA Hold (IC_SDA_HOLD)

Bits	Access Type	Default	Description
31:24	RO	8'b0	Reserved (RSV)
23:16	RW	8'h1	SDA Hold (IC_SDA_RX_HOLD) Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a transmitter.
15:0	RW	16'h1	IC_SDA_TX_HOLD (IC_SDA_TX_HOLD) Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a receiver

16.4.33 Transmit Abort Source (IC_TX_ABRT_SOURCE)

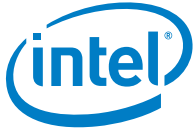
Used to indicate the source of the TX_ABRT interrupt. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

MEM Offset (B0002800) 80h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 187. Detailed Description of Transmit Abort Source (IC_TX_ABRT_SOURCE)

Bits	Access Type	Default	Description
31:17	RO	15'b0	Reserved (RSV)
16	RO	1'b0	ABRT_USER_ABRT (ABRT_USER_ABRT) This is a master-mode-only bit. Master has detected the transfer abort (IC_ENABLE[1])

Bits	Access Type	Default	Description
15	RO	1'b0	Slave Read Completion (ABRT_SLVRD_INTX) Set if the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register
14	RO	1'b0	Slave Lost Bus (ABRT_SLV_ARBLOST) Set if slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time. Note: Even though the slave never 'owns' the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then I2C controller no longer own the bus
13	RO	1'b0	Slave Flush TX FIFO (ABRT_SLVFLUSH_TXFIFO) Set if slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	RO	1'b0	Master Lost Arbitration (ARB_LOST) Set if master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Note: I2C can be both master and slave at the same time
11	RO	1'b0	Master Disabled (ABRT_MASTER_DIS) Set if user tries to initiate a Master operation with the Master mode disabled
10	RO	1'b0	10 Bit Address READ and RESTART Disabled (ABRT_10B_RD_NORSTRT) Set if the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the master sends a read command in 10-bit addressing mode
9	RO	1'b0	START With RESTART Disabled (ABRT_SBYTE_NORSTRT) To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets reasserted. Set if the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to send a START Byte
8	RO	1'b0	HS Mode With RESTART Disabled (ABRT_HS_NORSTRT) Set if the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to use the master to transfer data in High Speed mode
7	RO	1'b0	START Acknowledged (ABRT_SBYTE_ACKDET) Set if master has sent a START Byte and the START Byte was acknowledged (wrong behavior).



Bits	Access Type	Default	Description
6	RO	1'b0	HS Master ID Acknowledged (ABRT_HS_ACKDET) Set if master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	RO	1'b0	Read After General Call (ABRT_GCALL_READ) Set if master sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	RO	1'b0	General Call Not Acknowledged (ABRT_GCALL_NOACK) 1: I2C Controller in master mode sent a General Call and no slave on the bus acknowledged the General Call
3	RO	1'b0	TX Data Not Acknowledged (ABRT_TXDATA_NOACK) Set if master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledgement from the remote slave(s).
2	RO	1'b0	10 Bit Address Second Not Acknowledged (ABRT_10ADDR2_NOACK) Set if master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave
1	RO	1'b0	10 Bit Address First Not Acknowledged (ABRT_10ADDR1_NOACK) Set if master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave
0	RO	1'b0	7 Bit Address Not Acknowledged (ABRT_7B_ADDR_NOACK) Set if master is in 7-bit addressing mode and the address sent was not acknowledged by any slave

16.4.34 SDA Setup (IC_DMA_CR)

This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the registers address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE

MEM Offset (B0002800)	88h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 188. Detailed Description of SDA Setup (IC_DMA_CR)

Bits	Access Type	Default	Description
31:2	RO	30'b0	Reserved (RSV)
1	RW	1'h0	Transmit DMA Enable. (TDMAE) This bit enables/disables the transmit FIFO DMA channel. 0b: Transmit DMA disabled 1b: Transmit DMA enabled
0	RW	1'b0	Receive DMA Enable (RDMAE) This bit enables/disables the receive FIFO DMA channel. 0b: Receive DMA disabled 1b: Receive DMA enabled

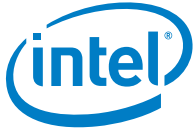
16.4.35 DMA Transmit Data Level Register (IC_DMA_TDLR)

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero

MEM Offset (B0002800)	8Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 189. Detailed Description of DMA Transmit Data Level Register (IC_DMA_TDLR)

Bits	Access Type	Default	Description
31:5	RO	27'b0	Reserved (RSV)
4:0	RW	5'h0	Transmit Data Level (DMATDL) Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1



16.4.36 I2C Receive Data Level Register (IC_DMA_RDLR)

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

MEM Offset (B0002800)	90h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 190. Detailed Description of I2C Receive Data Level Register (IC_DMA_RDLR)

Bits	Access Type	Default	Description
31:5	RO	27'b0	Reserved (RSV)
4:0	RW	5'h0	Receive Data Level (DMARDL) This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE = 1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO

16.4.37 SDA Setup (IC_SDA_SETUP)

Controls the amount of time delay (in terms of number of I2C clock periods) introduced in the rising edge of SCL relative to SDA changing, by holding SCL low when servicing a read request while operating as a slave-transmitter. This register must be programmed with a value equal to or greater than 2.

MEM Offset (B0002800)	94h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0064h



Table 191. Detailed Description of SDA Setup (IC_SDA_SETUP)

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	RW	8'h64	SDA Setup (SDA_SETUP) It is recommended that if the required delay is 1us, then for an I2C clock frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

16.4.38 General Call Ack (IC_ACK_GENERAL_CALL)

Controls whether the I2C controller responds with a ACK or NACK when it receives an I2C General Call address.

MEM Offset (B0002800)	98h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0001h

Table 192. Detailed Description of General Call Ack (IC_ACK_GENERAL_CALL)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)
0	RW	1'h1	I2C General Call Ack (ACK_GEN_CALL) When set to 1, the I2C controller responds with a ACK when it receives a General Call. Otherwise, the controller responds with a NACK.

16.4.39 Enable Status (IC_ENABLE_STATUS)

Report the I²C hardware status

MEM Offset (B0002800)	9Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 193. Detailed Description of Enable Status (IC_ENABLE_STATUS)

Bits	Access Type	Default	Description
31:3	RO	29'b0	Reserved (RSV)
2	RO	1'b0	Slave Received Data Lost (SLV_RX_DATA_LOST) Indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0. When read as 1, the I2C controller is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. NOTE: If the remote I2C master terminates the transfer with a STOP condition before the controller has a chance to NACK a transfer, and IC_ENABLE has been set to 0, then this bit is also set to 1. When read as 0, the controller is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. NOTE: The CPU can safely read this bit when IC_EN (bit 0) is read as 0
1	RO	1'b0	Slave Disabled While Busy (SLV_DISABLED_WHILE_BUSY) This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the IC_ENABLE register while: (a) the I2C controller is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, the controller is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address (IC_SAR register) OR if the transfer is completed before IC_ENABLE is set to 0 but has not taken effect. NOTE: If the remote I2C master terminates the transfer with a STOP condition before the controller has a chance to NACK a transfer, and IC_ENABLE has been set to 0, then this bit will also be set to 1. When read as 0, controller is deemed to have been disabled when there is master activity, or when the I2C bus is idle. NOTE: The CPU can safely read this bit when IC_EN (bit 0) is read as 0
0	RO	1'b0	I2C Enable Status (IC_EN) When read as 1, the controller is deemed to be in an enabled state. When read as 0, the controller is deemed completely inactive. NOTE: The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read SLV_RX_DATA_LOST (bit 2) and SLV_DISABLED_WHILE_BUSY (bit 1)

16.4.40 SS and FS Spike Suppression Limit (IC_FS_SPKLEN)

Used to store the duration, measured in I2C clock cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in



Standard/Fast Speed modes. The relevant I2C requirement is detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 2.

MEM Offset (B0002800)	0A0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0007h

Table 194. Detailed Description of SS and FS Spike Suppression Limit (IC_FS_SPKLEN)

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	RW	8'h07	I2C SS and FS Spike Length (IC_FS_SPKLENRX_TL) Must be set before any I2C bus transaction can take place to ensure stable operation.

17 I2S

The Intel® Quark™ SE Microcontroller C1000 supports a single instance of the I2S controller. The controller presents two I2S bus interfaces that are fully compliant with the Philips I2S bus specification. These two ports are used in PCM mode and enable simultaneous transmission and reception of stereo audio streams over I2S.

17.1 Signal Descriptions

Please see [Chapter 2, “Physical Interfaces”](#) for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction:** The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in [Chapter 4, “Electrical Characteristics”](#).
- **Description:** A brief explanation of the signal's function

Table 195. Memory Signals

Signal Name	Direction/ Type	Description
I2S_TSCK	I/O 1.8V or 3.3V	Transmit Interface Serial Clock: <i>Output when I2S Transmit Channel in Master Mode, Input when I2S Transmit Channel in Slave Mode</i>
I2S_TWS	I/O 1.8V or 3.3V	Transmit Interface Word Select: <i>Output when I2S Transmit Channel in Master Mode, Input when I2S Transmit Channel in Slave Mode</i>
I2S_TSD	O 1.8V or 3.3V	Transmit Interface Serial Data: <i>Transmit Channel Serial Data Output</i>
I2S_RSCK	I/O 1.8V or 3.3V	Receive Interface Serial Clock: <i>Output when I2S Receive Channel in Master Mode, Input when I2S Receive Channel in Slave Mode</i>
I2S_RWS	I/O 1.8V or 3.3V	Receive Interface Word Select: <i>Output when I2S Receive Channel in Master Mode, Input when I2S Receive Channel in Slave Mode</i>
I2S_RSD	I 1.8V or 3.3V	Receive Interface Serial Data: <i>Receive Channel Serial Data Input</i>



17.2 Features

The following is a list of the I2S controller features:

- 2 I2S Bus Interfaces
 - Transmit Interface
 - Receive Interface
- Audio Sample Rates of up to 48 kHz
- Audio Sample Resolution from 12 bit up to 32 bit
- Supports the following I2S Bus Interface Modes:
 - Philips Mode
 - Right Justified Mode
 - Left Justified Mode
 - DSP Mode
 - User Mode
- Each Interface can operate in either Master Mode or Slave Mode:
 - In Master Mode the I2S controller generates the SCK and WS signals
 - In Slave Mode the I2S controller synchronizes to external SCK and WS signals
- Hardware Handshake Interface to support DMA capability
- Both Interfaces are completely decoupled
 - Each Interface has dedicated SCK and WS signals
 - Each Interface can operate at different sample rates
- Interrupt Control
- FIFO mode support with 16B TX and RX FIFOs made from 4 entries of 32bits wide

17.2.1 I2S Protocol

The I2S (inter-IC sound) bus is a three-wire serial interface, consisting of a serial data line, a word select, and a serial clock. The serial data is time-multiplexed to carry stereo audio data. The word select is used to indicate when left audio data and right audio data is being transmitted on the serial data line.

17.2.2 I2S Modes of Operation

The I2S controller can operate in the following I2S bus interface modes:

- Philips Mode
- Right Justified Mode
- Left Justified Mode
- DSP Mode

These modes are configured through the DEV_CONF (Device Configuration) Register as outlined in the following table. See [Chapter 17.4, “Memory Mapped IO Registers”](#) for more details on this register.

Table 196. I2S Modes of Operation

I2S Mode	DEV_CONF Settings
Philips Mode	TRAN/REC_SCK_POLAR = 0 TRAN/REC_WS_POLAR = 0 TRAN/REC_APB_ALIGN_LR = 0 TRAN/REC_I2S_ALIGN_LR = 1 TRAN/REC_DATA_WS_DEL = 0 TRAN/REC_WS_DSP_MODE = 0
Right Justified Mode	TRAN/REC_SCK_POLAR = 0 TRAN/REC_WS_POLAR = 1 TRAN/REC_APB_ALIGN_LR = 0 TRAN/REC_I2S_ALIGN_LR = 0 TRAN/REC_DATA_WS_DEL = 1 TRAN/REC_WS_DSP_MODE = 0
Left Justified Mode	TRAN/REC_SCK_POLAR = 0 TRAN/REC_WS_POLAR = 1 TRAN/REC_APB_ALIGN_LR = 0 TRAN/REC_I2S_ALIGN_LR = 1 TRAN/REC_DATA_WS_DEL = 1 TRAN/REC_WS_DSP_MODE = 0
DSP Mode	TRAN/REC_SCK_POLAR = 0 TRAN/REC_WS_POLAR = 0 TRAN/REC_APB_ALIGN_LR = 0 TRAN/REC_I2S_ALIGN_LR = 1 TRAN/REC_DATA_WS_DEL = 0 TRAN/REC_WS_DSP_MODE = 1

User Mode is covered by any configuration of the DEV_CONF Register that does not match the above modes. TRAN/REC_APB_ALIGN_LR must be set to 0 for all modes.

The following timing diagrams show the operation of the I2S bus for the various modes.

Figure 25. Philips Mode

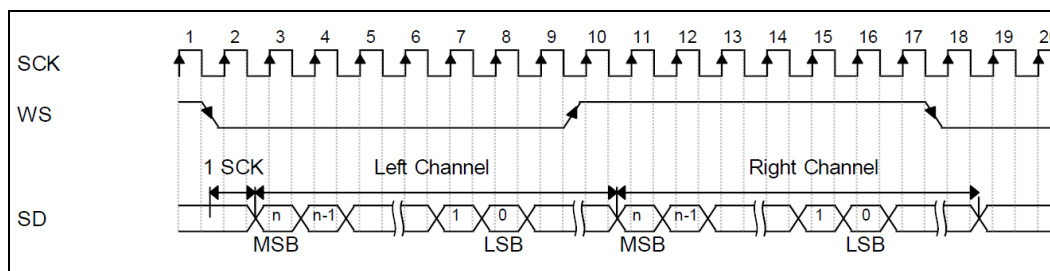


Figure 26. Right Justified Mode

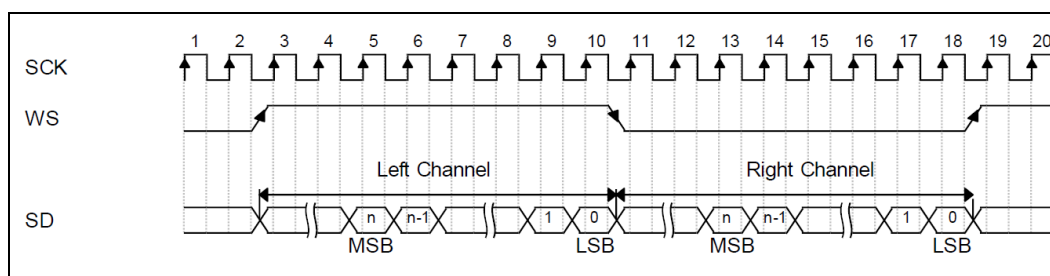


Figure 27. Left Justified Mode

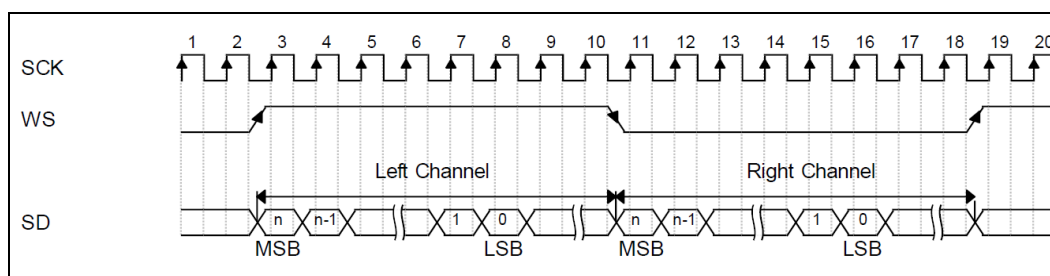
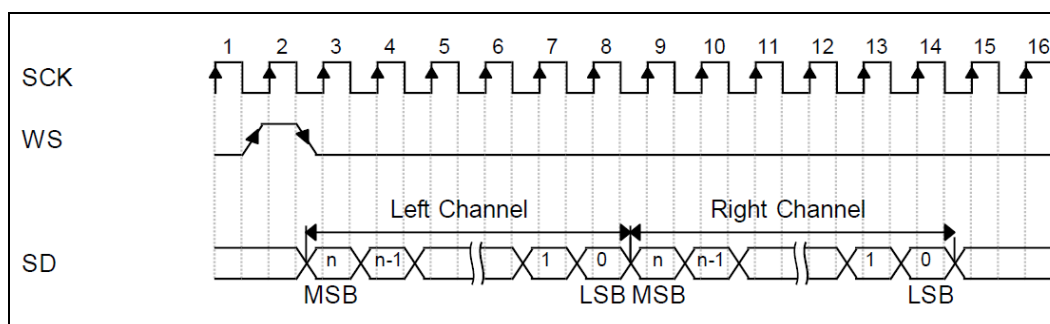
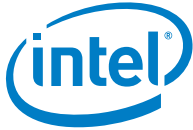


Figure 28. DSP Mode





17.2.3 Functional Operation

The I2S controller exposes two channels, Transmit and Receive, each with their own three-wire serial interface as described in [Chapter 17.1, “Signal Descriptions”](#). The Transmit Interface is associated with Channel 0 and the Receive Interface is associated with Channel 1.

Other than the direction of the serial data line, each Channel is identical and can be individually configured with the following options:

- Enable
- Clock Control
- Master Mode or Slave Mode
- Audio Sample Rate
- Audio Sample Resolution from 12bit up to 32bit
- FIFO Control and FIFO Thresholds

In Master Mode, the I2S controller is responsible for generating the serial clock (TSCK or RSCK depending on the channel) and the word select (TWS or RWS). The corresponding I/O become outputs. In Slave Mode, the I2S controller is responsible for synchronizing to an external serial clock (TSCK or RSCK depending on the channel) and external word select (TWS or RWS). The corresponding I/O become inputs.

The required serial clock can be derived from the desired sample rate and sample resolution as follows:

$$\text{Serial Clock Frequency} = \text{Sample Rate} * 2 * \text{Sample Resolution}$$

For example, for a 48 kHz sample rate with a 32bit sample resolution the required serial clock frequency is: $48 \text{ kHz} * 2 * 32 = 3.072 \text{ MHz}$

For details on how to program the serial clock frequency, see [Chapter 17.2.4, “I2S Clocking”](#).

Each channel has a 4-entry FIFO with each entry consisting of 32bits of data. Each entry corresponds to an audio sample. If the audio sample resolution is configured to be less than 32bits, the unused bits are padded with zero in accordance with the alignment configuration for the selected I2S mode.

Each FIFO supports software reset as well as configurable Almost Empty and Almost Full thresholds.

The I2S controller supports interrupt generation with the following maskable sources:

- Transmit FIFO Full
- Transmit FIFO Almost Full



- Transmit FIFO Almost Empty
- Transmit FIFO Empty
- Transmit FIFO Underrun
- Receive FIFO Overrun
- Receive FIFO Full
- Receive FIFO Almost Full
- Receive FIFO Almost Empty
- Receive FIFO Empty

17.2.4 I2S Clcking

The serial clock is derived from the system clock using a programmable divider. Each channel has an individually configurable divider (I2S_SRR.TSAMPLE_RATE and I2S_SRR.RSAMPLE_RATE). For odd divider values, the serial clock low time will be one system clock period longer than the serial clock high time. The serial clock is only generated when the channel is operating in Master Mode.

The following table shows some example serial clock configurations. This assumes a nominal system clock frequency of 32 MHz. The divider values must be updated if the system clock frequency is changed.

Table 197. Serial Clock Generation

Sample Rate	Sample Resolution	Desired Serial Clock Frequency	Divider Value TSAMPLE_RATE RSAMPLE_RATE	Generated Serial Clock Frequency	Generated Serial Clock Accuracy
48 kHz	32bit	3.072 MHz	10	3.2 MHz	4.16%
44.1 kHz	24bit	2.117 MHz	15	2.133 MHz	0.76%
24 kHz	24bit	1.152 MHz	28	1.143 MHz	0.79%
22.05 kHz	24bit	1.058 MHz	30	1.067 MHz	0.85%
12 kHz	16bit	384 kHz	83	386 kHz	0.52%
8 kHz	16bit	256 kHz	125	256 kHz	0 %

48 kHz is the fastest sample rate supported that guarantees a serial clock of sufficient accuracy. This requires a system clock frequency of 32 MHz.

The I2S controller does not generate the master clock for the Audio Codec. Only the serial clock is generated.



17.3 Use

17.3.1 DMA Operation

The I2S controller supports interfacing to the DMA controller. We highly recommend using the DMA controller capabilities to offload the I2S FIFO data transfer. This prevents the processor being unduly burdened with I2S controller interrupt handling as well as I2S FIFO data transfer.

Apply the following DMA controller configuration constraints for correct DMA operation:

*CTLx.SRC_MSIZ*E = 1

*CTLx.DEST_MSIZ*E = 1

Apply the following I2S controller configuration constraints for correct DMA operation:

TFIFO_CTRL.TAFULL_THRESHOLD = 1

RFIFO_CTRL.RAFULL_THRESHOLD = 1

17.3.2 Loopback Modes

The I2S controller supports internal loopback capabilities with the following constraints.

Table 198. Loopback Capabilities

Loopback Capability	Configuration / Constraint
Transmit Serial Data (TSD) to Receive Serial Data (RSD)	<i>I2S_CTRL.LOOP_BACK_0_1</i> = 1 This mode is not for normal functional operation and is only intended as a test mode.
Transmit Serial Clock (TSCK) to Receive Serial Clock (RSCK) and Transmit Word Select (TWS) to Receive Word Select (RWS)	<i>I2S_CTRL.RSYNC_LOOP_BACK</i> = 1 The Transmit Channel must be configured for Master Mode operation and the Receive Channel must be configured for Slave Mode operation. This mode can be used for normal functional operation.
Receive Serial Clock (RSCK) to Transmit Serial Clock (TSCK) & Receive Word Select (RWS) to Transmit Word Select (TWS)	<i>I2S_CTRL.TSYNC_LOOP_BACK</i> = 1 The Transmit Channel must be configured for Slave Mode operation and the Receive Channel must be configured for Master Mode operation. This mode can be used for normal functional operation.



17.3.3 Codec Connectivity

There are effectively four main methods of connecting to an Audio Codec supporting the I2S bus interface. These are called out in the following table, along with details on connecting to the I2S controller.

Table 199. Codec Connectivity Methods

Codec Interface Description	Connection to I2S Controller
Separate I2S bus for Receive and Transmit, with individual Serial Clock and Word Select signals for Receive and Transmit. (Transmit and Receive Interface are either both Slave Mode, both Master Mode or a mix.)	Connect the Codec Receive Interface signals to all Transmit Channel Interface signals and configure the Transmit Channel for Master Mode or Slave Mode as appropriate. Connect the Codec Transmit Interface signals to all Receive Channel Interface signals and configure the Receive Channel for Master Mode or Slave Mode as appropriate.
Single I2S bus for Receive and Transmit with common Serial Clock and Word Select signals operating in Master Mode.	Connect the Codec Serial Clock, Word Select and Receive Serial Data signals to all Transmit Channel Interface Signals and configure the Transmit Channel for Slave Mode. Connect the Codec Serial Clock, Word Select and Transmit Serial Data signals to all Receive Channel Interface signals and configure the Receive Channel for Slave Mode. That is, codec SCK drives both TSCK and RSCK and Codec WS drive both TWS and RWS.
Single I2S bus for Receive and Transmit with common Serial Clock and Word Select signals operating in Slave Mode.	Connect the Codec Serial Clock, Word Select and Receive Serial Data signals to all Transmit Channel Interface Signals and configure the Transmit Channel for Master Mode. Only connect the Codec Transmit Serial Data signal to the Receive Channel Interface Serial Data signal and configure the Receive Channel for Slave Mode with following loopback capability enabled: (I2S_CTRL.RSYNC_LOOP_BACK = 1) That is, codec only driven by TSCK and TWS, RSCK and RWS are unused and associated pins can be freed up for alternative functions by reconfiguring the pin muxing.



Codec Interface Description	Connection to I2S Controller
Single I2S bus for Receive and Transmit with common Serial Clock and Word Select signals operating in Slave Mode.	Only connect the Codec Receive Serial Data signal to the Transmit Channel Interface Serial Data signal and configure the Transmit Channel for Slave Mode with following loopback capability enabled: (I2S_CTRL.TSYNC_LOOP_BACK = 1) Connect the Codec Serial Clock, Word Select and Transmit Serial Data signals to all Receive Channel Interface Signals and configure the Receive Channel for Master Mode. That is, codec only driven by RSCK and RWS, TSCK and TWS are unused and associated pins can be freed up for alternative functions by reconfiguring the pin muxing.

17.4 Memory Mapped IO Registers

Registers listed are for I2S, starting at base address B0003800h.

Table 200. Summary of I2S Registers—0xB0003800

MEM Address	Default	Instance Name	Name
0x0	0190_0000h	I2S_CTRL	I2S Control Register
0x4	0000_0000h	I2S_STAT	I2S Status Register
0x8	0000_0000h	I2S_SRR	I2S Channels Sample Rate and Resolution Configuration Register
0xC	0000_0000h	CID_CTRL	Clock, Interrupt and DMA Control Register
0x10	0000_0000h	TFIFO_STAT	The Transmit FIFO Status Register
0x14	0000_0000h	RFIFO_STAT	The Receive FIFO Status Register
0x18	0003_0000h	TFIFO_CTRL	Transmit FIFO Control Register
0x1C	0003_0000h	RFIFO_CTRL	Receive FIFO Control Register
0x20	0000_0208h	DEV_CONF	Device Configuration Register
0x50	0000_0000h	DATA_REG	Data Register

I2S Control Register (I2S_CTRL)

MEM Offset (B0003800)	0B0003800h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0190_0000h

Table 201. Detailed Description of I2S Control Register (I2S_CTRL)

Bits	Access Type	Default	Description
31:29	RO	3'b0	Reserved (RSV)
28	RW	1'b0	Loop Back Configuration bit for Receiver Synchronizing Unit (RSYNC_LOOP_BACK) When '1' (normal mode), the SCK and WS inputs of the I2S module (configured to be Receiver Synchronization Unit) are connected internally to the external inputs RSCK and RWS. When '0' (loop-back mode), the SCK and WS inputs of the I2S module (configured to be Receiver Synchronization Unit) are connected internally to the Transmitter Synchronizing Unit outputs TSCK and TWS.
27	RW	1'b0	Loop Back Configuration bit for Transmitter Synchronizing Unit (TSYNC_LOOP_BACK) When '1' (normal mode), the SCK and WS inputs of the I2S module (configured to be Transmitter Synchronization Unit) are connected internally to the external inputs TSCK and TWS. When '0' (loop-back mode), the SCK and WS inputs of the I2S module (configured to be Transmitter Synchronization Unit) are connected internally to the Receiver Synchronizing Unit outputs RSCK and RWS.
26	RW	1'b0	Reset for Receiver Synchronizing Unit (RSYNC_RST) When '0' the Receiver Synchronizing Unit is held in reset, software must set this to '1', to take this unit out of reset for normal operation
25	RW	1'b0	Reset for Transmitter Synchronizing Unit (TSYNC_RST) When '0' the Transmitter Synchronizing Unit is held in reset, software must set this to '1', to take this unit out of reset for normal operation
24	RW	1'b1	Receive FIFO Reset (RFIFO_RST) When '0', Receive FIFO pointers are reset to zero. Threshold level for this FIFO is unchanged. This bit is automatically set to '1' after one clock cycle.
23	RW	1'b1	Transmit FIFO Reset (TFIFO_RST) When '0', Transmit FIFO pointers are reset to zero. Threshold level for this FIFO is unchanged. This bit is automatically set to '1' after one clock cycle.
22	RW	1'b0	Receiver Master/Slave Configuration bit (R_MS) Master (value '1') or Slave (value '0') select bit, for unit synchronizing all receivers with I2S bus.



Bits	Access Type	Default	Description
21	RW	1'b0	Transmitter Master/Slave Configuration bit (T_MS) Master (value '1') or Slave (value '0') select bit, for unit synchronizing all transmitters with I2S bus.
20	RW	1'b1	Configuration Register Soft Reset (SFR_RST) When '0', all bits in registers are reset to default values. This bit is automatically set to '1' after one clock cycle.
19	RW	1'b0	Reserved (RSV14) This field is reserved READ/WRITE but operation of this field is unsupported.
18	RW	1'b0	Reserved (RSV13) This field is reserved READ/WRITE but operation of this field is unsupported.
17	RW	1'b0	Reserved (RSV12) This field is reserved READ/WRITE but operation of this field is unsupported.
16	RW	1'b0	Loop Back Test Configuration bit (LOOP_BACK_0_1) When '1', it configures Channels 0 and 1 into the loop-back mode. In this mode Channels 0 and 1 can work in both directions depending on configuration. Default value '0' causes normal operation without loop-back.
15	RW	1'b0	Reserved (RSV11) This field is reserved READ/WRITE but operation of this field is unsupported.
14	RW	1'b0	Reserved (RSV10) This field is reserved READ/WRITE but operation of this field is unsupported.
13	RW	1'b0	Reserved (RSV9) This field is reserved READ/WRITE but operation of this field is unsupported.
12	RW	1'b0	Reserved (RSV8) This field is reserved READ/WRITE but operation of this field is unsupported.
11	RW	1'b0	Reserved (RSV7) This field is reserved READ/WRITE but operation of this field is unsupported.
10	RW	1'b0	Reserved (RSV6) This field is reserved READ/WRITE but operation of this field is unsupported.



Bits	Access Type	Default	Description
9	RW	1'b0	Receiver Configuration bit (TR_CFG_1) This bit should be programmed to '0'. Receiver only supported on Channel 1. Sampled on the rising edge of the clock.
8	RW	1'b0	Transmitter Configuration bit (TR_CFG_0) This bit should be programmed to '1'. Transmitter only supported on Channel 0. Sampled on the rising edge of the clock.
7	RW	1'b0	Reserved (RSV5) This field is reserved READ/WRITE but operation of this field is unsupported.
6	RW	1'b0	Reserved (RSV4) This field is reserved READ/WRITE but operation of this field is unsupported.
5	RW	1'b0	Reserved (RSV3) This field is reserved READ/WRITE but operation of this field is unsupported.
4	RW	1'b0	Reserved (RSV2) This field is reserved READ/WRITE but operation of this field is unsupported.
3	RW	1'b0	Reserved (RSV1) This field is reserved READ/WRITE but operation of this field is unsupported.
2	RW	1'b0	Reserved (RSV0) This field is reserved READ/WRITE but operation of this field is unsupported.
1	RW	1'b0	Enable bit for I2S Channel 1 (I2S_EN_1) Value '0' resets channel. Value '1' enables channel.
0	RW	1'b0	Enable bit for I2S Channel 0 (I2S_EN_0) Value '0' resets channel. Value '1' enables channel.

I2S Status Register (I2S_STAT)

MEM Offset (B0003800)	0B0003804h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

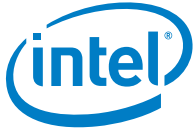


Table 202. Detailed Description of I2S Status Register (I2S_STAT)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved (RSV)
15	RW	1'b0	Receive FIFO Almost Full Flag (RFIFO_AFULL) Active HIGH. Updated on the rising edge of the clock. This bit can trigger the interrupt.
14	RW	1'b0	Receive FIFO Full Flag (RFIFO_FULL) Active HIGH. Updated on the rising edge of the clock. This bit can trigger the interrupt.
13	RW	1'b0	Receive FIFO Almost Empty Flag (RFIFO_AEMPTY) Active HIGH. Updated on the rising edge of the clock. This bit can trigger the interrupt.
12	RW	1'b0	Receive FIFO Empty Flag (RFIFO_EMPTY) Active HIGH. Updated on the rising edge of the clock. This bit can trigger the interrupt.
11	RW	1'b0	Transmit FIFO Almost Full Flag (TFIFO_AFULL) Active HIGH. Updated on the rising edge of the clock. This bit can trigger the interrupt.
10	RW	1'b0	Transmit FIFO Full Flag (TFIFO_FULL) Active HIGH. Updated on the rising edge of the clock. This bit can trigger the interrupt.
9	RW	1'b0	Transmit FIFO Almost Empty Flag (TFIFO_AEMPTY) Active HIGH. Updated on the rising edge of the clock. This bit can trigger the interrupt.
8	RW	1'b0	Transmit FIFO Empty Flag (TFIFO_EMPTY) Active HIGH. Updated on the rising edge of the clock. This bit can trigger the interrupt.



Bits	Access Type	Default	Description
7:5	RO	3'b0	Receiver Overrun Channel Number (OVRERR_CODE) Code of the receiver that caused overrun error. Updated on the rising edge of the clock. The code is a binary notation of the channel's number. This should always be Channel 1
4	RW	1'b0	Receiver Data Overrun Wrror (RDATA_OVRERR) Indicates receiver data overrun error, active HIGH. Sampled and updated on the rising edge of the clock. This bit can trigger the interrupt. Writing a LOW value to this bit resets all receivers and the receive FIFO. The receiver configuration is preserved.
3:1	RO	3'b0	Transmitter Underrun Channel Number (UNDERR_CODE) Code of the transmitter that caused underrun error. Updated on the rising edge of the clock. The code is a binary notation of the channel's number. This should always be Channel 0.
0	RW	1'b0	Transmitter Data Underrun Error (TDATA_UNDERR) Indicates transmitter data underrun error, active HIGH. Sampled and updated on the rising edge of the clock. This bit can trigger the interrupt. Writing a LOW value to this bit resets all transmitters. The transmit FIFO contents and pointers are preserved. The transmitter configuration is preserved.

I2S Channels Sample Rate and Resolution Configuration Register (I2S_SRR)

MEM Offset (B0003800)	0B0003808h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 203. Detailed Description of I2S Channels Sample Rate and Resolution Configuration Register (I2S_SRR)

Bits	Access Type	Default	Description
31:27	RW	5'b0	Receiver Resolution (RRESOLUTION) (0 to 31). This should be assigned the value equal to the number of valid bits minus one.
26:16	RW	11'b0	Receiver Sample Rate (RSAMPLE_RATE) See Sample Rate Generation Details under the I2S Clocking section.
15:11	RW	5'b0	Transmitter Resolution (TRESOLUTION) (0 to 31). This should be assigned the value equal to the number of valid bits minus one.
10:0	RW	11'b0	Transmitter Sample Rate (TSAMPLE_RATE) See Sample Rate Generation Details under the I2S Clocking section.

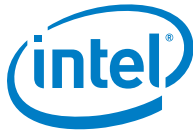


Clock, Interrupt and DMA Control Register (CID_CTRL)

MEM Offset (B0003800)	0B000380Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 204. Detailed Description of Clock, Interrupt and DMA Control Register (CID_CTRL)

Bits	Access Type	Default	Description
31	RW	1'b0	Bit Masking Interrupt Request generation for Receive FIFO Almost Full. (RFIFO_AFULL_MASK) When LOW, masks generation of interrupt request.
30	RW	1'b0	Bit Masking Interrupt Request generation for Receive FIFO Full. (RFIFO_FULL_MASK) When LOW, masks generation of interrupt request.
29	RW	1'b0	Bit Masking Interrupt Request generation for Receive FIFO Almost Empty. (RFIFO_AEMPTY_MASK) When LOW, masks generation of interrupt request.
28	RW	1'b0	Bit Masking Interrupt Request generation for Receive FIFO Empty. (RFIFO_EMPTY_MASK) When LOW, masks generation of interrupt request.
27	RW	1'b0	Bit Masking Interrupt Request generation for Transmit FIFO Almost Full. (TFIFO_AFULL_MASK) When LOW, masks generation of interrupt request.
26	RW	1'b0	Bit Masking Interrupt Request generation for Transmit FIFO Full. (TFIFO_FULL_MASK) When LOW, masks generation of interrupt request.
25	RW	1'b0	Bit Masking Interrupt Request generation for Transmit FIFO Almost Empty. (TFIFO_AEMPTY_MASK) When LOW, masks generation of interrupt request.
24	RW	1'b0	Bit Masking Interrupt Request generation for Transmit FIFO Empty. (TFIFO_EMPTY_MASK) When LOW, masks generation of interrupt request.
23	RW	1'b0	Reserved (RSV12) This field is reserved READ/WRITE but operation of this field is unsupported
22	RW	1'b0	Reserved (RSV11) This field is reserved READ/WRITE but operation of this field is unsupported
21	RW	1'b0	Reserved (RSV10) This field is reserved READ/WRITE but operation of this field is unsupported



Bits	Access Type	Default	Description
20	RW	1'b0	Reserved (RSV9) This field is reserved READ/WRITE but operation of this field is unsupported
19	RW	1'b0	Reserved (RSV8) This field is reserved READ/WRITE but operation of this field is unsupported
18	RW	1'b0	Reserved (RSV7) This field is reserved READ/WRITE but operation of this field is unsupported
17	RW	1'b0	Bit Masking Channel 1 Interrupt Request generation for Underrun/Overrun (I2S_MASK_1) When LOW, masks generation of interrupt request caused by the Channel 1.
16	RW	1'b0	Bit Masking Channel 0 Interrupt Request generation for Underrun/Overrun (I2S_MASK_0) When LOW, masks generation of interrupt request caused by the Channel 0.
15	RW	1'b0	Bit Masking All Interrupt Requests (INTREQ_MASK) When '0' all interrupts are masked, when '1' interrupts use individual masks.
14:10	RO	5'b0	Reserved (RSV6)
9	RW	1'b0	Clock Enable for the Receiver Synchronization Units (STROBE_RS) When high the receiver clock is blocked, else it is enabled.
8	RW	1'b0	Clock Enable for the Transmitter Synchronization Units (STROBE_TS) When high the transmitter clock is blocked, else it is enabled.
7	RW	1'b0	Reserved (RSV5) This field is reserved READ/WRITE but operation of this field is unsupported
6	RW	1'b0	Reserved (RSV4) This field is reserved READ/WRITE but operation of this field is unsupported
5	RW	1'b0	Reserved (RSV3) This field is reserved READ/WRITE but operation of this field is unsupported
4	RW	1'b0	Reserved (RSV2) This field is reserved READ/WRITE but operation of this field is unsupported



Bits	Access Type	Default	Description
3	RW	1'b0	Reserved (RSV1) This field is reserved READ/WRITE but operation of this field is unsupported
2	RW	1'b0	Reserved (RSV0) This field is reserved READ/WRITE but operation of this field is unsupported
1	RW	1'b0	Clock Enable, Channel 1 (I2S_STROBE_1) When high the clock is blocked, else it is enabled.
0	RW	1'b0	Clock Enable, Channel 0 (I2S_STROBE_0) When high the clock is blocked, else it is enabled.

The Transmit FIFO Status Register (TFIFO_STAT)

MEM Offset (B0003800)	0B0003810h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 205. Detailed Description of the Transmit FIFO Status Register (TFIFO_STAT)

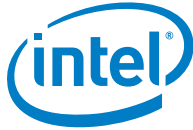
Bits	Access Type	Default	Description
31:5	RO	27'b0	Reserved (RSV)
4:0	RO	5'b0	Transmit FIFO Level (TLEVEL) Indicates transmit FIFO level. Updated on the rising edge of the clock. Legal values 0 - 16.

The Receive FIFO Status Register (RFIFO_STAT)

MEM Offset (B0003800)	0B0003814h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 206. Detailed Description of the Receive FIFO Status Register (RFIFO_STAT)

Bits	Access Type	Default	Description
31:5	RO	27'b0	Reserved (RSV)
4:0	RO	5'b0	Receive FIFO Level (RLEVEL) Indicates receive FIFO level. Updated on the rising edge of the clock. Legal values 0 - 16.

**Transmit FIFO Control Register (TFIFO_CTRL)**

MEM Offset (B0003800) 0B0003818h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0003_0000h

Table 207. Detailed Description of Transmit FIFO Control Register (TFIFO_CTRL)

Bits	Access Type	Default	Description
31:18	RO	14'b0	Reserved (RSV1)
17:16	RW	2'b11	Transmit FIFO Almost Full Threshold (TAFULL_THRESHOLD) Determines threshold for almost full flag in the Transmit FIFO.
15:2	RO	14'b0	Reserved (RSV0)
1:0	RW	2'b0	Transmit FIFO Almost Empty Threshold (TAEMPTY_THRESHOLD) Determines threshold for almost empty flag in the Transmit FIFO.

Receive FIFO Control Register (RFIFO_CTRL)

MEM Offset (B0003800) 0B000381Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0003_0000h

Table 208. Detailed Description of Receive FIFO Control Register (RFIFO_CTRL)

Bits	Access Type	Default	Description
31:18	RO	14'b0	Reserved (RSV1)
17:16	RW	2'b11	Receive FIFO Almost Empty Threshold (RAFULL_THRESHOLD) Determines threshold for almost empty flag in the Receive FIFO.
15:2	RO	14'b0	Reserved (RSV0)
1:0	RW	2'b0	Receive FIFO Almost Empty Threshold (RAEMPTY_THRESHOLD) Determines threshold for almost empty flag in the Receive FIFO.



Device Configuration Register (DEV_CONF)

MEM Offset (B0003800)	0B0003820h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0208h

Table 209. Detailed Description of Device Configuration Register (DEV_CONF)

Bits	Access Type	Default	Description
31:12	RO	20'b0	Reserved (RSV)
11	RW	1'b0	Receive Word Select DSP Mode (REC_WS_DSP_MODE) HIGH value of this bit determines generation of the word select signal format specific to the DSP audio interface mode. LOW value of this bit determines generation of the word select signal format specific to the standard Philips I2S interface.
10	RW	1'b0	Receive Data Delay for I2S Serial Data Input after Word Select (REC_DATA_WS_DEL) When HIGH, the serial data for reception is sampled on the first rising/falling edge of the clock signal after word select signal change. When LOW, the serial data for reception is sampled on the second rising/falling edge of the clock signal after word select signal change.
9	RW	1'b1	Alignment of Receive Data for I2S Serial Data Output (REC_I2S_ALIGN_LR) HIGH value of this bit selects MSB I2S Serial Data side alignment for the received data sample. LOW value of this bit selects LSB I2S Serial Data side alignment for the received data sample. If the received data sample resolution doesn't match the I2S serial data format (24 bits by default), the audio sample is extended with zeros or truncated at the MSB side.
8	RW	1'b0	Alignment of Receive Data for Processor Interface (REC_APB_ALIGN_LR) HIGH value of this bit selects MSB Processor Interface side alignment for the received data sample. LOW value of this bit selects LSB Processor Interface side alignment for the received data sample. This field should be left at 0



Bits	Access Type	Default	Description
7	RW	1'b0	Word Select Polarity for Reception (REC_WS_POLAR) When HIGH, the level of the word select signal for the received left channel data sample is 1 and the level of this signal for the transmitted right channel data sample is 0. When LOW, the level of the word select signal for the received left channel data sample is 0 and the level of this signal for the transmitted right channel data sample is 1.
6	RW	1'b0	Serial Clock Active Edge for Reception (REC_SCK_POLAR) When HIGH, the serial data for reception is sampled on the falling edge of the bit clock. When LOW, the serial data for reception is sampled on the rising edge of the bit clock.
5	RW	1'b0	Transmit Word Select DSP Mode (TRAN_WS_DSP_MODE) HIGH value of this bit determines generation of the word select signal format specific to the DSP audio interface mode. LOW value of this bit determines generation of the word select signal format specific to the standard Philips I2S interface.
4	RW	1'b0	Transmit Data Delay for I2S Serial Data Output after Word Select (TRAN_DATA_WS_DEL) When HIGH, the serial data for transmission is updated on the first rising/falling edge of the clock signal after word select signal change. When LOW, the serial data for transmission is updated on the second rising/falling edge of the clock signal after word select signal change.
3	RW	1'b1	Alignment of Transmit Data for I2S Serial Data Output (TRAN_I2S_ALIGN_LR) HIGH value of this bit selects MSB I2S Serial Data side alignment for the transmitted data sample. LOW value of this bit selects LSB I2S Serial Data side alignment for the transmitted data sample. If the transmitted data sample resolution doesn't match the I2S serial data format (24 bits by default), the audio sample is extended with zeros or truncated at the MSB side.



Bits	Access Type	Default	Description
2	RW	1'b0	Alignment of Transmit Data for Processor Interface (TRAN_APB_ALIGN_LR) HIGH value of this bit selects MSB Processor Interface side alignment for the transmitted data sample. LOW value of this bit selects LSB Processor Interface side alignment for the transmitted data sample. This field should be left at 0
1	RW	1'b0	Word Select Polarity for Transmission (TRAN_WS_POLAR) When HIGH, the level of the word select signal for the transmitted left channel data sample is 1 and the level of this signal for the transmitted right channel data sample is 0. When LOW, the level of the word select signal for the transmitted left channel data sample is 0 and the level of this signal for the transmitted right channel data sample is 1.
0	RW	1'b0	Serial Clock Active Edge for Transmission (TRAN_SCK_POLAR) When HIGH, the serial data for transmission is updated on the falling edge of the bit clock. When LOW, the serial data for transmission is updated on the rising edge of the bit clock.

Data Register (DATA_REG)

MEM Offset (B0003800)	0B0003850h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 210. Detailed Description of Data Register (DATA_REG)

Bits	Access Type	Default	Description
31:0	RW	32'b0	Data Register (DATA_REG) This register is a 32-bit read/write buffer for the Transmit / Receive FIFOs. When the register is read, data is pulled from the receive FIFO. When it is written to, data is moved into the transmit FIFO.





18 UART

The Intel® Quark™ SE Microcontroller C1000 implements two instances of a 16550 compliant UART controller that supports baud rates between 300 baud and 2M baud. Hardware flow control is also supported.

18.1 Signal Descriptions

Please see [Chapter 2, “Physical Interfaces”](#) for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction:** The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in [Chapter 4, “Electrical Characteristics”](#).
- **Description:** A brief explanation of the signal's function

Table 211. Memory 0 Signals

Signal Name	Direction/ Type	Description
UART_0_RXD	I/O	UART 0 Receive Data: <i>Signal Description</i>
UART_0_TXD	I/O	UART 0 Transmit Data: <i>Signal Description</i>
UART_0_RTS_B	I/O	UART 0 Request To Send: <i>Signal Description</i>
UART_0_CTS_B	I/O	UART 0 Clear to Send: <i>Signal Description</i>

Table 212. Memory 1 Signals

Signal Name	Direction/ Type	Description
UART_1_RXD	I/O	UART 1 Receive Data: <i>Signal Description</i>
UART_1_TXD	I/O	UART 1 Transmit Data: <i>Signal Description</i>
UART_1_RTS_B	I/O	UART 1 Request To Send: <i>Signal Description</i>
UART_1_CTS_B	I/O	UART 1 Clear to Send: <i>Signal Description</i>

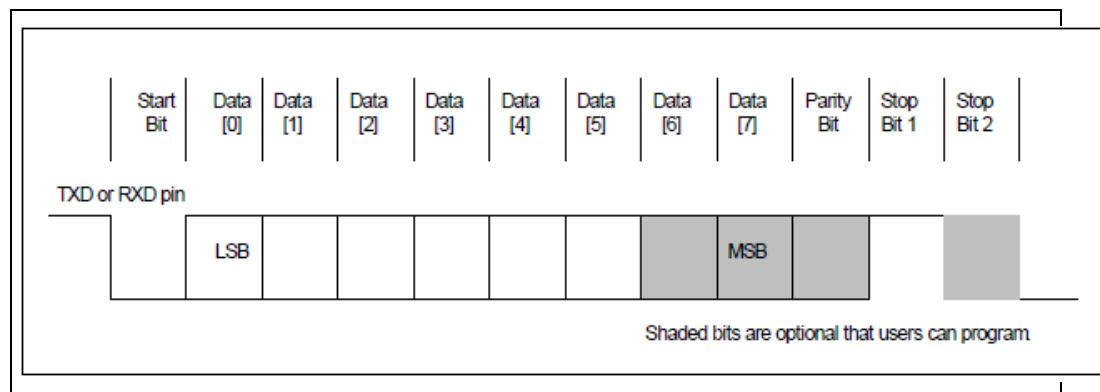
18.2 Features

18.2.1 UART Function

The UART transmits and receives data in bit frames as shown in [Figure 29](#).

- Each data frame is between 7 and 12 bits long, depending on the size of data programmed and if parity and stop bits are enabled.
- The frame begins with a start bit that is represented by a high-to-low transition.
- Next, 5 to 8 bits of data are transmitted, beginning with the least significant bit. An optional parity bit follows, which is set if even parity is enabled and an odd number of ones exist within the data byte; or, if odd parity is enabled and the data byte contains an even number of ones.
- The data frame ends with one, one-and-one-half, or two stop bits (as programmed by users), which is represented by one or two successive bit periods of a logic one.

Figure 29. UART Data Transmission



Each UART has a Transmit FIFO and a Receive FIFO and each holds 16 characters of data. There are two separate methods for moving data into/out of the FIFOs Interrupts and Polling.

18.2.2 Baud Rate Generator

The baud rates for the UARTs are generated from the base frequency (Fbase) indicated in [Table 98](#) by programming the DLH and DLL registers as divisor. The hexadecimal value of the divisor is (IER_DLH[7:0]<<8) | RBR_THR_DLL[7:0]. The output baud rate is equal to the base frequency divided by sixteen times the value of the divisor, as follows:

- $\text{baud rate} = (\text{Fbase}) / (16 * \text{divisor})$



The UART also supports fractional dividers of 1/16 of the divisor by programming the DLF[3:0] register.

- $\text{baud rate} = (\text{Fbase}) / (16 * (\text{divisor} + (\text{fdivisor}/16))$

18.3 Use

Each UART has a transmit FIFO and a receive FIFO, each FIFO holding 16 characters of data. Three separate methods move data into and out of the FIFOs: interrupts, DMA, and polled.

18.3.1 DMA Mode Operation

18.3.1.1 Receiver DMA

The data transfer from the HSUART to host memory is controlled by the DMA write channel. To configure the channel in write mode, channel direction in the channel control register must be programmed to "1". The software must program the descriptor start address register, descriptor transfer size register, and descriptor control register before starting the channel using the channel active bit in the channel control register.

18.3.1.2 Transmit DMA

The data transfer from host memory to HSUART is controlled by DMA read channel. To configure the channel in read mode, channel direction in the channel control register must be programmed to "0". The software must program the descriptor start address register, descriptor transfer size register, and descriptor control register before starting the channel using the channel active bit in the channel control register.

18.3.1.3 Removing Trailing Bytes in DMA Mode

When the number of entries in the Receive FIFO is less than its trigger level, and no additional data is received, the remaining bytes are called trailing bytes. These are DMA'ed out by the DMA as it has visibility into the FIFO Occupancy register.

18.3.1.4 FIFO Polled-Mode Operation

With the FIFOs enabled (IIR_FCR.IID0_FIFOE bit set to 1), clearing IER_DLH[7] and IER_DLH[4:0] puts the serial port in the FIFO Polled Operation mode. Because the receiver and the transmitter are controlled separately, either one or both can be in Polled Operation mode. In this mode, software checks Receiver and Transmitter status using the Line Status Register (LSR). The processor polls the following bits for Receive and Transmit Data Service.



18.3.1.5 Receive Data Service

The processor checks the data ready (LSR.DR) bit which is set when one or more bytes remain in the Receive FIFO or Receive Buffer Register (RBR_THR_DLL).

18.3.1.6 Transmit Data Service

The processor checks transmit data request LSR.THRE bit, which is set when the transmitter needs data. The processor can also check transmitter empty LSR.TEMT, which is set when the Transmit FIFO or Holding register is empty.

18.3.2 Autoflow Control

Autoflow Control uses Clear-to-Send (nCTS) and Request-to-Send (nRTS) signals to automatically control the flow of data between the UART and external modem. When autoflow is enabled, the remote device is not allowed to send data unless the UART asserts nRTS low. If the UART de-asserts nRTS while the remote device is sending data, the remote device is allowed to send one additional byte after nRTS is deasserted. An overflow could occur if the remote device violates this rule. Likewise, the UART is not allowed to transmit data unless the remote device asserts nCTS low. This feature increases system efficiency and eliminates the possibility of a Receive FIFO Overflow error due to long interrupt latency.

Autoflow mode can be used in two ways:

- Full autoflow, automating both nCTS and nRTS
- Half autoflow, automating only nCTS

Full Autoflow is enabled by writing a 1 to bits 1 and 5 of the Modem Control Register (MCR). Auto-nCTS-Only mode is enabled by writing a 1 to bit 5 and a 0 to bit 1 of the MCR register.

18.3.3 RTS (UART Output)

When in full autoflow mode, nRTS is asserted when the UART FIFO is ready to receive data from the remote transmitter. This occurs when the amount of data in the Receive FIFO is below the programmable threshold value. When the amount of data in the Receive FIFO reaches the programmable threshold, nRTS is de-asserted. It will be asserted once again when enough bytes are removed from the FIFO to lower the data level below the threshold.

18.3.4 CTS (UART Input)

When in Full or Half-Autoflow mode, nCTS is asserted by the remote receiver when the receiver is ready to receive data from the UART. The UART checks nCTS before sending the next byte of data and will not transmit the byte until nCTS is low. If nCTS goes high while the transfer of a byte is in progress, the transmitter will complete this byte.



18.4 Memory Mapped IO Registers

Registers listed are for UART 0, starting at base address B0002000h. UART 1 contains the same registers starting at base address B0002400h. Differences between the UARTs are noted in individual registers.

Table 213. Summary of UART Registers—0xB0002000

MEM Address	Default	Instance Name	Name
0x0	0000_0000h	RBR_THR_DLL	Receive Buffer / Transmit Holding / Divisor Latch Low
0x4	0000_0000h	IER_DLH	Interrupt Enable / Divisor Latch High
0x8	0000_0001h	IIR_FCR	Interrupt Identification / FIFO Control
0xC	0000_0000h	LCR	Line Control
0x10	0000_0000h	MCR	MODEM Control
0x14	0000_0060h	LSR	Line Status
0x18	0000_0000h	MSR	MODEM Status
0x1C	0000_0000h	SCR	Scratchpad
0x7C	0000_0000h	USR	UART Status
0xA4	0000_0000h	HTX	Halt Transmission
0xA8	0000_0000h	DMASA	DMA Software Acknowledge
0xC0	0000_0000h	DLF	Divisor Latch Fraction

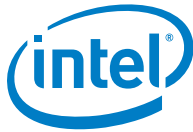
Receive Buffer / Transmit Holding / Divisor Latch Low (RBR_THR_DLL)

Receive Buffer Register (RBR), reading this register when the DLAB bit (LCR[7]) is zero; Transmit Holding Register (THR), writing to this register when the DLAB is zero; Divisor Latch Low (DLL), when DLAB bit is one.

MEM Offset (B0002000)	0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 214. Detailed Description of Receive Buffer / Transmit Holding / Divisor Latch Low (RBR_THR_DLL)

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)



Bits	Access Type	Default	Description
7:0	RW	8'h00	Receive Buffer / Transmit Holding / Divisor Latch Low (FIELD) Different UART registers are accessed depending on read/write transfer type and Line control Register (LCR) DLAB bit value. RBR, Receive Buffer Register Access - Read AND DLAB (LCR[7]) =0 Data byte received on the serial input port. Valid only if the Data Ready (DR) bit in the LSR is set. If FIFOs are disabled (FCR[0] set to zero), the data must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an over-run error occurs. THR, Transmit Holding Register. Access - Write AND DLAB (LCR[7]) =0 Data to be transmitted on the serial output port (sout). Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFOs are disabled (FCR[0] = 0) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost. DLL, Lower part of the Divisor Latch. Access - Read/Write AND DLAB (LCR[7]) =1 Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set. Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of sclk should be allowed to pass before transmitting or receiving data.

Interrupt Enable / Divisor Latch High (IER_DLH)

Interrupt Enable Register (IER), when the DLAB bit is zero; Divisor Latch High (DLH), when the DLAB bit is one.

MEM Offset (B0002000)	4h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 215. Detailed Description of Interrupt Enable / Divisor Latch High (IER_DLH)

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	RW	8'h00	Interrupt Enable / Divisor Latch High (FIELD) Different UART registers are accessed depending on the Line control Register (LCR) DLAB bit value. IER, Interrupt Enable Register Access - Read/write AND DLAB (LCR[7]) =0 Interrupt Enable Register: Each of the bits used has a different function (0 = disabled 1 = enabled): 0 ERBFI, Enable Received Data Available Interrupt 1 ETBEI, Enable Transmit Holding Register Empty Interrupt 2 ELSI, Enable Receiver Line Status Interrupt 3 EDSSI, Enable Modem Status Interrupt 4 RESERVED 5 RESERVED 6 RESERVED 7 PTIME, Programmable THRE Interrupt Mode Enable DLH, Divisor Latch (High) Access - Read/write AND DLAB (LCR[7]) =1 This register makes up the upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set. This register may be accessed only when the DLAB bit (LCR[7]) is set. Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of sclk should be allowed to pass before transmitting or receiving data.

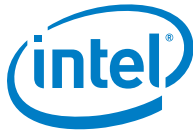
Interrupt Identification / FIFO Control (IIR_FCR)

Interrupt Identification Register (IIR) if reading; FIFO Control Register (FCR) if writing

MEM Offset (B0002000)	8h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0001h

Table 216. Detailed Description of Interrupt Identification / FIFO Control (IIR_FCR)

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)



7:0	RW	8'h01	Interrupt Identification / FIFO Control (FIELD) Different UART registers are accessed depending on read/write transfer type. IIR, Interrupt Identification Register Access - Read only Each of the bits used has a different function: 0-3 IID, Interrupt ID. This indicates the highest priority pending interrupt which can be one of the following types: 0000 = modem status. 0001 = no interrupt pending. 0010 = THR empty. 0100 = received data available. 0110 = receiver line status. 0111 = busy detect. NEVER INDICATED 1100 = character timeout. 4-5 RESERVED read as zero 6-7 FIFOSE, FIFOs Enabled. This is used to indicate whether the FIFOs are enabled or disabled: 00 = disabled 11 = enabled RESET VALUE FOR IIR = 0x01 FCR, FIFO Control Register Access - Write only Used to control the FIFOs. Different functions: 0 FIFOE, FIFO Enable. Enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs will be reset. 1 RFIFOR, RCVR FIFO Reset Resets the control portion of the receive FIFO and treats the FIFO as empty. This will also de-assert the DMA RX request and single signals. NOTE that this bit is 'self-clearing' and it is not necessary to clear this bit. 2 XFIFOR, XMIT FIFO Reset Resets the control portion of the transmit FIFO and treats the FIFO as empty. This will also de-assert the DMA TX request and single signals. NOTE that this bit is 'self-clearing' and it is not necessary to clear this bit.

Bits	Access Type	Default	Description
			3 DMAM, DMA Mode Not used in Dublin Bay LSIO UART due to the use of extra DMA handshake interface signals 4-5 TET, TX Empty Trigger Used to select the empty threshold level at which the THRE Interrupts will be generated when the mode is active. It also determines when the dma_tx_req_n signal will be asserted when in certain modes of operation. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO 1/4 full 11 = FIFO 1/2 full 6-7 RT, RCVR Trigger Used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt will be generated. In auto flow control mode it is used to determine when the rts_n signal will be de-asserted. It also determines when the dma_rx_req_n signal will be asserted when in certain modes of operation. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO 1/4 full 10 = FIFO 1/2 full 11 = FIFO 2 less than full

Line Control (LCR)

Used to specify the format of the asynchronous data communication exchange.

MEM Offset (B0002000)	0Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 217. Detailed Description of Line Control (LCR)

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7	RW	1'h0	Divisor Latch Access Bit (DLAB) Used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.



Bits	Access Type	Default	Description
6	RW	1'h0	Break Control Bit (BC) Used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared.
5	RW	1'h0	Reserved for future use (STICK_PAR)
4	RW	1'h0	Even Parity Select (EPS) Used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic '1's is transmitted or checked. If set to zero, an odd number of logic '1's is transmitted or checked.
3	RW	1'h0	Parity Enable (PEN) Used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0 = parity disabled 1 = parity enabled
2	RW	1'h0	Number of stop bits (STOP) Used to select the number of stop bits per character that the peripheral will transmit and receive. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. NOTE that regardless of the number of stop bits selected the receiver will only check the first stop bit. 0 = 1 stop bit 1 = 1.5 stop bits when DLS (LCR[1:0]) == 00 1 = 2 stop bits when DLS (LCR[1:0]) different from 00
1:0	RW	2'h0	Data Length Select (DLS) Used to select the number of data bits per character that the peripheral will transmit and receive. The number of bit that may be selected areas follows: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits

MODEM Control (MCR)

Controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM)

MEM Offset (B0002000)	10h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 218. Detailed Description of MODEM Control (MCR)

Bits	Access Type	Default	Description
31:6	RO	26'b0	Reserved (RSV)
5	RW	1'h0	Auto Flow Control Enable (AFCE) When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled 0 = Auto Flow Control Mode disabled 1 = Auto Flow Control Mode enabled
4	RW	1'h0	LoopBack Bit (LOOPBACK) Used to put the UART into a diagnostic mode for test purposes. Data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally.
3	RW	1'h0	User designated Output 2 (OUT2) Used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: 0 = out2_n de-asserted (logic 1) 1 = out2_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.
2	RW	1'h0	User designated Output 1 (OUT1) Used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: 0 = out1_n de-asserted (logic 1) 1 = out1_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.



Bits	Access Type	Default	Description
1	RW	1'h0	Request to Send (RTS) Used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, MCR[5] set to one and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal will be de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	RW	1'h0	Data Terminal Ready (DTR) Used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: 0 = dtr_n de-asserted (logic 1) 1 = dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

Line Status (LSR)

Provides status information concerning the data transfer.

MEM Offset (B0002000)	14h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0060h

Table 219. Detailed Description of Line Status (LSR)

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)

Bits	Access Type	Default	Description
7	RO	1'h0	Receiver FIFO Error bit (RFE) This bit is only relevant when FIFO are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. That is: 0 = no error in RX FIFO 1 = error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.
6	RO	1'h1	Transmitter Empty bit (TEMT) If FIFO are enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If FIFO are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	RO	1'h1	Transmit Holding Register Empty bit (THRE) If THRE mode is disabled (IER[7] set to zero) and regardless of FIFOs being enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If the THRE mode and FIFO are enabled (IER[7] and FCR[0] set to one), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	RO	1'h0	Break Interrupt bit (BI) Used to indicate the detection of a break sequence on the serial input data. If in UART mode it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.



Bits	Access Type	Default	Description
3	RO	1'h0	Framing Error bit (FE) Used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs the UART will try resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit, that is, data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no framing error, 1 = framing error Reading the LSR clears the FE bit.
2	RO	1'h0	Parity Error bit (PE) Used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no parity error, 1 = parity error Reading the LSR clears the PE bit.
1	RO	1'h0	Overrun error bit (OE) Used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0 = no overrun error, 1 = overrun error Reading the LSR clears the OE bit.
0	RO	1'h0	Data Ready bit (DR) Used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0 = no data ready, 1 = data ready This bit is cleared when the RBR is read in the non-FIFO mode, or when the receiver FIFO is empty, in the FIFO mode.

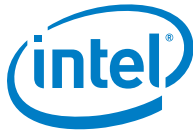
MODEM Status (MSR)

Provides the current state of the control lines from the MODEM (or peripheral device)

MEM Offset (B0002000)	18h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 220. Detailed Description of MODEM Status (MSR)

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7	RO	1'h0	Data Carrier Detect (DCD) Used to indicate the current state of the modem control line dcd_n. That is this bit is the complement dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0 = dcd_n input is de-asserted (logic 1) 1 = dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2).
6	RO	1'h0	Ring Indicator (RI) Used to indicate the current state of the modem control line ri_n. That is this bit is the complement ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0 = ri_n input is de-asserted (logic 1) 1 = ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1).
5	RO	1'h0	Data Set Ready (DSR) Used to indicate the current state of the modem control line dsr_n. That is this bit is the complement dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the UART. 0 = dsr_n input is de-asserted (logic 1) 1 = dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	RO	1'h0	Clear to Send (CTS) Used to indicate the current state of the modem control line cts_n. That is, this bit is the complement cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the UART 0 = cts_n input is de-asserted (logic 1) 1 = cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), CTS is the same as MCR[1] (RTS).



Bits	Access Type	Default	Description
3	RO	1'h0	Delta Data Carrier Detect (DDCD) Used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. That is: 0 = no change on dcd_n since last read of MSR 1 = change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] set to one), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit will get set when the reset is removed if the dcd_n signal remains asserted.
2	RO	1'h0	Trailing Edge of Ring Indicator (TERI) Used to indicate that a change on the input ri_n (from an active low, to an inactive high state) has occurred since the last time the MSR was read. That is: 0 = no change on ri_n since last read of MSR 1 = change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] set to one), TERI reflects when MCR[2] (Out1) has changed state from a high to a low.
1	RO	1'h0	Delta Data Set Ready (DDSR) Used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. That is: 0 = no change on dsr_n since last read of MSR 1 = change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] set to one), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit will get set when the reset is removed if the dsr_n signal remains asserted.
0	RO	1'h0	Delta Clear to Send (DCTS) used to indicate that the modem control line cts_n has changed since the last time the MSR was read. That is: 0 = no change on cts_n since last read of MSR 1 = change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] set to one), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit will get set when the reset is removed if the cts_n signal remains asserted.

Scratchpad (SCR)

Used by the programmer to hold data temporarily

MEM Offset (B0002000)	1Ch
Security_PolicyGroup	
IntelRsvd	False



Size 32 bits
Default 0000_0000h

Table 221. Detailed Description of Scratchpad (SCR)

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	RW	8'h0	Scratchpad Register (SCR) This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

UART Status (USR)

Provides internal status information

MEM Offset (B0002000) 7Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 222. Detailed Description of UART Status (USR)

Bits	Access Type	Default	Description
31:5	RO	27'h0	Reserved (RSV1)
4	RO	1'h0	Receive FIFO Full (RFF) Used to indicate that the receive FIFO is completely full. That is: 0 = Receive FIFO not full 1 = Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	RO	1'h0	Receive FIFO Not Empty (RFNE) Used to indicate that the receive FIFO contains one or more entries. 0 = Receive FIFO is empty 1 = Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	RO	1'h0	Transmit FIFO Empty (TFE) Used to indicate that the transmit FIFO is completely empty. 0 = Transmit FIFO is not empty 1 = Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	RO	1'h0	Transmit FIFO Not Full (TFNF) Used to indicate that the transmit FIFO is not full. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	RO	1'h0	Reserved (RSV0)



Halt Transmission (HTX)

Halt Transmission

MEM Offset (B0002000) 0A4h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 223. Detailed Description of Halt Transmission (HTX)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)
0	RW	1'h0	Halt Transmission (HTX) Used to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are enabled. Note, if FIFOs are not enabled the setting of the halt TX register will have no effect on operation. 0 = Halt TX disabled 1 = Halt TX enabled

DMA Software Acknowledge (DMASA)

DMA software acknowledge if a transfer needs to be terminated due to an error condition.

MEM Offset (B0002000) 0A8h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 224. Detailed Description of DMA Software Acknowledge (DMASA)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)
0	RW	1'h0	DMA Software Acknowledge (DMASA) Used to perform DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the UART should clear its request. This will cause the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing' and it is not necessary to clear this bit.

Divisor Latch Fraction (DLF)

Divisor Latch Fraction

MEM Offset (B0002000) 0C0h



Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 225. Detailed Description of Divisor Latch Fraction (DLF)

Bits	Access Type	Default	Description
31:2	RO	30'b0	Reserved (RSV)
1:0	RW	2'h0	Divisor Latch Fraction (DLF) register Divisor Latch Fraction (DLF) is used to store the Fractional part of BAUD divisor

18.5 Register Map Reference

For more information, see [Chapter 0, “§](#)

[Register Access Methods”](#) and [Chapter 6, “Mapping Address Spaces”](#).

§



19 SPI

The Intel® Quark™ SE Microcontroller C1000 implements three instances of a SPI controller. Two of these controllers support Master operation and one controller supports Slave operation.

19.1 Signal Description

Please see [Chapter 2, “Physical Interfaces”](#) for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction:** The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in [Chapter 4, “Electrical Characteristics”](#).
- **Description:** A brief explanation of the signal's function

Table 226. SPI Master 0 Signals

Signal Name	Direction/ Type	Description
SPI_M_0_SCK	O	SPI Serial Clock: <i>Signal Description</i>
SPI_M_0_SS_B[3:0]	O	SPI Slave Selects: <i>Signal Description</i>
SPI_M_0_MOSI	O	SPI Master Output Slave Input: <i>Signal Description</i>
SPI_M_0_MISO	I	SPI Master Input Slave Output: <i>Signal Description</i>

Table 227. SPI Master 1 Signals

Signal Name	Direction/ Type	Description
SPI_M_1_SCK	O	SPI Serial Clock: <i>Signal Description</i>
SPI_M_1_SS_B[3:0]	O	SPI Slave Selects: <i>Signal Description</i>
SPI_M_1_MOSI	O	SPI Master Output Slave Input: <i>Signal Description</i>
SPI_M_1_MISO	I	SPI Master Input Slave Output: <i>Signal Description</i>



Table 228. SPI Slave 0 Signals

Signal Name	Direction/ Type	Description
SPI_S_0_SCK	I	SPI Serial Clock: <i>Signal Description</i>
SPI_S_0_SS_B	I	SPI Slave Select: <i>Signal Description</i>
SPI_S_0_MOSI	I	SPI Master Output Slave Input: <i>Signal Description</i>
SPI_S_0_MISO	O	SPI Master Input Slave Output: <i>Signal Description</i>

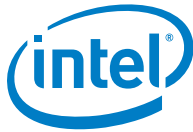
19.2 Features

SPI Master features:

- 2 SPI Master Interfaces
- Control of up to 4 Slave Selects
- Frame Formats:
 - Motorola SPI
 - Texas Instruments SSP
 - National Semiconductors Microwire
- Transfer Modes:
 - Transmit and Receive
 - Transmit Only
 - Receive Only
 - EEPROM Read
- Serial Clock Frequencies up to 16 MHz
- 4 bit to 32 bit Frame Size
- Configurable Clock Polarity and Clock Phase
- Hardware Handshake Interface to support DMA capability
- Interrupt Control
- FIFO mode support with 16B deep TX and RX FIFOs

SPI Slave features:

- 1 SPI Slave Interface
- Frame Formats:
 - Motorola SPI
 - Texas Instruments SSP



- National Semiconductors Microwire
- Transfer Modes:
 - Transmit and Receive
 - Transmit Only
 - Receive Only
 - EEPROM Read
- Serial Clock Frequencies up to 3.2 MHz
- 4 bit to 32 bit Frame Size
- Configurable Clock Polarity and Clock Phase
- Hardware Handshake Interface to support DMA capability
- Interrupt Control
- FIFO mode support with 16B TX and RX FIFOs made from 4 entries of 32bits wide

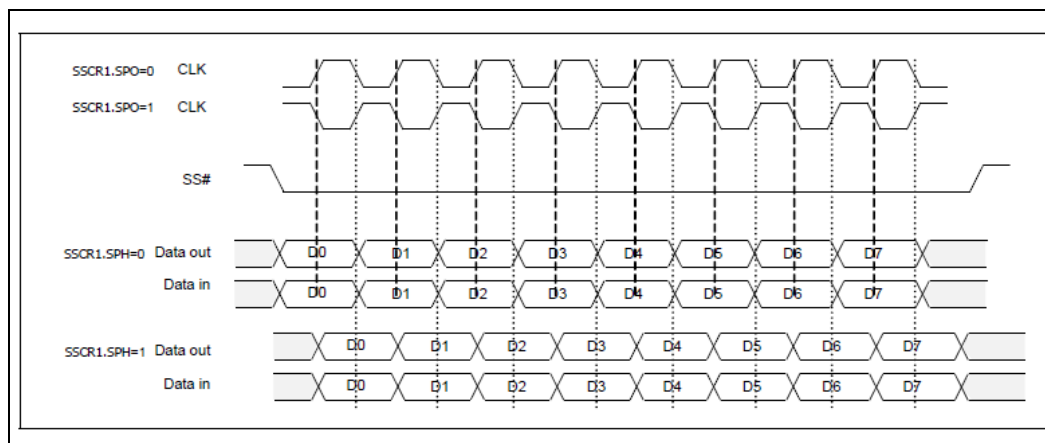
19.2.1 Clock Phase and Polarity

SPI clock phase and clock polarity overview.

- The SSCR1.SPO polarity setting bit determines whether the serial transfer occurs on the rising edge of the clock or the falling edge of the clock.
 - When SSCR1.SPO = 0, the inactive or idle state of SIO_SPI_CLK is low.
 - When SSCR1.SPO = 1, the inactive or idle state of SIO_SPI_CLK is high.
- The SSCR1.SPH phase setting bit selects the relationship of the serial clock with the slave select signal.
 - When SSCR1.SPH = 0, SIO_SPI_CLK is inactive until one cycle after the start of a frame and active until 1/2 cycle after the end of a frame.
 - When SSCR1.SPH = 1, SIO_SPI_CLK is inactive until 1/2 cycle after the start of a frame and active until one cycle after the end of a frame.

The following figure shows an 8-bit data transfer with different phase and polarity settings.

Figure 30. 8-bit Data Transfer



19.2.2 SPI Controller

The SPI unit provides one-channel, 3-wire serial input/output interface to directly connect SPI-compatible devices.

Four pins are used to transfer data between the CPU and external device:

- SCLK defines the bit rate at which serial data is driven onto, and sampled from, the bus
- SS_B or CS defines the boundaries of a basic data "unit", comprised of multiple serial bits
- MOSI or SDO is the serial data path for outbound data, from system to peripheral
- MISO or SDI is the serial data path for inbound data, from peripheral to system

Serial data is transferred between the system and an external peripheral through FIFOs in the SPI. Transfers are initiated by the host processor and data is transferred over a single transfer. Operation is full duplex. Separate FIFOs and serial data paths allow simultaneous transfers in both directions to and from the external peripheral. Transfer is started when either new data is available in the transmit FIFO or memory is available in the receive FIFO. Transfer is terminated when either new data is not available in the transmit FIFO or memory is not available in the receive FIFO.

19.2.3 Processor Initiated Data Transfer

Transmit data (from system to peripheral) is written by the host processor to the SPI Transmit FIFO. The FIFO is seen as one 32-bit location by the processor and a write to the FIFO takes the form of a single 32-bit write transaction to the data register (SSDR). The SPI moves the data from the Transmit FIFO, serializes it, and sends it over the serial wire (SDO) to the peripheral. Receive data from the peripheral (on SDI) is converted to parallel words and stored in the Receive FIFO register file. When passed, a



programmable “fullness” threshold triggers an interrupt to the Interrupt Controller (and subsequently, if enabled, to an interrupt input to the CPU). The interrupt service routine responds by identifying the source of the interrupt and then doing a read from the Receive FIFO. The SPI differentiates between the two FIFOs according to whether the transfer is a READ or a WRITE transfer. Read bursts automatically target the Receive FIFO, while write bursts write data to the Transmit FIFO. From a memory map point of view, they are at the same address. FIFOs are 8x 32bits deep.

19.2.4 Data Format

Data in the FIFOs is always stored with one sample per 32-bit word regardless of the format's data word length. Within each 32-bit field, the stored data sample is right justified, with the word's LSB in bit 0, and unused bits packed as zeroes on the left-hand (MSB) side. Logic in the SPI guarantees that data is properly transmitted on SDO according to the selected frame format and MSB first.

19.2.5 Baud Rate Generation

In master mode, the max frequency of SCLK is half the SSI BASE CLK (maximum of 32 MHz). Therefore the maximum of 16mbps is supported for SPI master transfers.

In Slave mode the max frequency is limited to 10 times less than the SSI BASE CLK (maximum of 32 MHz). Therefore the maximum of 3.2mbps is supported for SPI slave transfers.

Baud rate is configured by writing to the BAUDR register.

19.2.6 Memory Mapped IO Registers

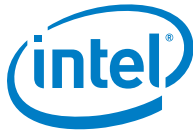
Registers listed are for SPI Master 0, starting at base address B0001000h. SPI Master 1 contains the same registers starting at base address B0001400h same registers. SPI Slave 0 contains the same registers starting at base address B0001800h. Differences between the SPIs are noted in individual registers.

Table 229. Summary of SPI Registers—0xB0001000

MEM Address	Default	Instance Name	Name
0x0	0007_0000h	CTRLR0	Control Register 0
0x4	0000_0000h	CTRLR1	Control Register 1
0x8	0000_0000h	SSIENR	SSI Enable Register
0xC	0000_0000h	MWCR	Microwire Control Register
0x10	0000_0000h	SER	Slave Enable Register
0x14	0000_0000h	BAUDR	Baud Rate Select
0x18	0000_0000h	TXFTLR	Transmit FIFO Threshold Level



MEM Address	Default	Instance Name	Name
0x1C	0000_0000h	RXFTLR	Receive FIFO Threshold Level
0x20	0000_0000h	TXFLR	Transmit FIFO Level Register
0x24	0000_0000h	RXFLR	Receive FIFO Level Register
0x28	0000_0006h	SR	Status Register
0x2C	0000_003Fh	IMR	Interrupt Mask Register
0x30	0000_0000h	ISR	Interrupt Status Register
0x34	0000_0000h	RISR	Raw Interrupt Status Register
0x38	0000_0000h	TXOICR	Transmit FIFO Overflow Interrupt Clear Register
0x3C	0000_0000h	RXOICR	Receive FIFO Overflow Interrupt Clear Register
0x40	0000_0000h	RXUICR	Receive FIFO Underflow Interrupt Clear Register
0x44	0000_0000h	MSTICR	Multi-Master Interrupt Clear Register
0x48	0000_0000h	ICR	Interrupt Clear Register
0x4C	0000_0000h	DMACR	DMA Control Register
0x50	0000_0000h	DMATDLR	DMA Transmit Data Level
0x54	0000_0000h	DMARDLR	DMA Receive Data Level
0x58	0000_0000h	IDR	Identification Register
0x5C	3332_332Ah	SSI_COMP_VERSION	coreKit Version ID register
0x60	0000_0000h	DR0	Data Register
0x64	0000_0000h	DR1	Data Register
0x68	0000_0000h	DR2	Data Register
0x6C	0000_0000h	DR3	Data Register
0x70	0000_0000h	DR4	Data Register
0x74	0000_0000h	DR5	Data Register
0x78	0000_0000h	DR6	Data Register
0x7C	0000_0000h	DR7	Data Register
0x80	0000_0000h	DR8	Data Register
0x84	0000_0000h	DR9	Data Register
0x88	0000_0000h	DR10	Data Register
0x8C	0000_0000h	DR11	Data Register
0x90	0000_0000h	DR12	Data Register
0x94	0000_0000h	DR13	Data Register
0x98	0000_0000h	DR14	Data Register
0x9C	0000_0000h	DR15	Data Register
0xA0	0000_0000h	DR16	Data Register
0xA4	0000_0000h	DR17	Data Register



MEM Address	Default	Instance Name	Name
0xA8	0000_0000h	DR18	Data Register
0xAC	0000_0000h	DR19	Data Register
0xB0	0000_0000h	DR20	Data Register
0xB4	0000_0000h	DR21	Data Register
0xB8	0000_0000h	DR22	Data Register
0xBC	0000_0000h	DR23	Data Register
0xC0	0000_0000h	DR24	Data Register
0xC4	0000_0000h	DR25	Data Register
0xC8	0000_0000h	DR26	Data Register
0xCC	0000_0000h	DR27	Data Register
0xD0	0000_0000h	DR28	Data Register
0xD4	0000_0000h	DR29	Data Register
0xD8	0000_0000h	DR30	Data Register
0xDC	0000_0000h	DR31	Data Register
0xE0	0000_0000h	DR32	Data Register
0xE4	0000_0000h	DR33	Data Register
0xE8	0000_0000h	DR34	Data Register
0xEC	0000_0000h	DR35	Data Register
0xF0	0000_0000h	RX_SAMPLE_DLY	RX Sample Delay Register

Control Register 0 (CTRLR0)

This register controls the serial data transfer. It is impossible to write to this register when the SPI bus controller is enabled. The SPI bus controller is enabled and disabled by writing to the SSIENR register.

MEM Offset (B0001000)	0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0007_0000h

Table 230. Detailed Description of Control Register 0 (CTRLR0)

Bits	Access Type	Default	Description
31:21	RO	11'b0	Reserved 2 (RSVD2) Reserved

Bits	Access Type	Default	Description
20:16	RW/L	5'h07	Data Frame Size in 32-bit mode (DFS_32) Used to select the data frame length in 32 bit mode. These bits are only valid when SSI_MAX_XFER_SIZE is configured to 32. When the data frame size is programmed to be less than 32-bits, the receive data is automatically right-justified by the receive logic, with the upper bits of the receive FIFO zero-padded. Transmit data must be right-justified by the user before writing into the transmit FIFO. The transmit logic will ignore the upper unused bits when transmitting the data.
15:12	RW/L	4'h0	Control Frame Size (CFS) Control Frame Size. Selects the length of the control word for the Microwire frame format.
11	RW/L	1'h0	Shift Register Loop (SRL) Used for testing purposes only. When internally active, connects the transmit shift register output to the receive shift register input. Can be used in both serial-slave and serial-master modes. 0 : Normal Mode Operation 1 : Test Mode Operation When the SPI bus controller is configured as a slave in loopback mode, the ss_in_n and ssi_clk signals must be provided by an external source. In this mode, the slave cannot generate these signals because there is nothing to which to loop back.
10	RW/L	1'h0	Slave Output Enable (SLV_OE) Relevant only when the SPI bus controller is configured as a serial-slave device. When configured as a serial master, this bit field has no functionality. This bit enables or disables the setting of the ssi_oe_n output from the SPI bus controller serial slave. When SLV_OE = 1, the ssi_oe_n output can never be active. When the ssi_oe_n output controls the tri-state buffer on the txd output from the slave, a high impedance state is always present on the slave txd output when SLV_OE = 1. This is useful when the master transmits in broadcast mode (master transmits data to all slave devices). Only one slave may respond with data on the master rxd line. This bit is enabled after reset and must be disabled by software (when broadcast mode is used), if you do not want this device to respond with data. 0 - Slave txd is enabled 1 - Slave txd is disabled



Bits	Access Type	Default	Description
9:8	RW/L	2'h0	Transfer Mode (TMOD) Transfer Mode. Selects the mode of transfer for serial communication. This field does not affect the transfer duplicity. Only indicates whether the receive or transmit data are valid. In transmit-only mode, data received from the external device is not valid and is not stored in the receive FIFO memory; it is overwritten on the next transfer. In receive-only mode, transmitted data are not valid. After the first write to the transmit FIFO, the same word is retransmitted for the duration of the transfer. In transmit-and-receive mode, both transmit and receive data are valid. The transfer continues until the transmit FIFO is empty. Data received from the external device are stored into the receive FIFO memory, where it can be accessed by the host processor. In eeprom-read mode, receive data is not valid while control data is being transmitted. When all control data is sent to the EEPROM, receive data becomes valid and transmit data becomes invalid. All data in the transmit FIFO is considered control data in this mode. This transfer mode is only valid when the SPI bus controller is configured as a master device. 00 - Transmit and Receive 01 - Transmit Only 10 - Receive Only 11 - EEPROM Read
7	RW/L	1'h0	Serial Clock Polarity (SCPOL) Valid when the frame format (FRF) is set to Motorola SPI. Used to select the polarity of the inactive serial clock, which is held inactive when the SPI bus controller master is not actively transferring data on the serial bus. 0 : Inactive state of serial clock is low 1 : Inactive state of serial clock is high Dependencies: When SSI_HC_FRF=1, SCPOL bit is a read-only bit with its value set by SSI_DFLT_SCPOL.
6	RW/L	1'h0	Serial Clock Phase (SCPH) Valid when the frame format (FRF) is set to Motorola SPI. The serial clock phase selects the relationship of the serial clock with the slave select signal. When SCPH = 0, data are captured on the first edge of the serial clock. When SCPH = 1, the serial clock starts toggling one cycle after the slave select line is activated, and data are captured on the second edge of the serial clock. 0: Serial clock toggles in middle of first data bit 1: Serial clock toggles at start of first data bit Dependencies: When SSI_HC_FRF=1, SCPH bit is a read-only bit, with its value set by SSI_DFLT_SCPH.



Bits	Access Type	Default	Description
5:4	RW	2'h0	Frame Format (FRF) Selects which serial protocol transfers the data. b00 -- Motorola SPI b01 - Texas Instruments SSP b10 - National Semiconductors Microwire b11 - Reserved
3:0	RO	4'b0	Reserved 1 (RSVD1) Reserved

Control Register 1 (CTRLR1)

This register exists only when the SPI bus controller is configured as a master device. When the SPI bus controller is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. Control register 1 controls the end of serial transfers when in receive-only mode. It is impossible to write to this register when the SPI bus controller is enabled. The SPI bus controller is enabled and disabled by writing to the SSIENR register.

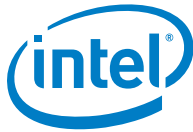
MEM Offset (B0001000)	4h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 231. Detailed Description of Control Register 1 (CTRLR1)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW/L	16'h0	Number of Data Frames (NDF) When TMOD = 10 or TMOD = 11, this register field sets the number of data frames to be continuously received by the SPI bus controller. The SPI bus controller continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 64 kB of data in a continuous transfer. When the SPI bus controller is configured as a serial slave, the transfer continues for as long as the slave is selected. Therefore, this register serves no purpose and is not present when the SPI bus controller is configured as a serial slave.

SSI Enable Register (SSIENR)

MEM Offset (B0001000)	8h
Security_PolicyGroup	



IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 232. Detailed Description of SSI Enable Register (SSIENR)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved 1 (RSVD1) Reserved
0	RW	1'h0	SSI Enable (SSIENR) Enables and disables all SPI bus controller operations. When disabled, all serial transfers are halted immediately. Transmit and receive FIFO buffers are cleared when the device is disabled. It is impossible to program some of the SPI bus controller control registers when enabled. When disabled, the ssi_sleep output is set (after delay) to inform the system that it is safe to remove the ssi_clk, thus saving power consumption in the system.

Microwire Control Register (MWCR)

This register controls the direction of the data word for the half-duplex Microwire serial protocol. It is impossible to write to this register when the SPI bus controller is enabled. The SPI bus controller is enabled and disabled by writing to the SSIENR register.

MEM Offset (B0001000) 0Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 233. Detailed Description of Microwire Control Register (MWCR)

Bits	Access Type	Default	Description
31:3	RO	29'b0	Reserved 1 (RSVD1) Reserved
2	RW/L	1'h0	Microwire Handshaking (MHS) Relevant only when the SPI bus controller is configured as a serial-master device. When configured as a serial slave, this bit field has no functionality. Used to enable and disable the 'busy/ready' handshaking interface for the Microwire protocol. When enabled, the SPI bus controller checks for a ready status from the target slave, after the transfer of the last data/control bit, before clearing the BUSY status in the SR register. 0: handshaking interface is disabled 1: handshaking interface is enabled



Bits	Access Type	Default	Description
1	RW/L	1'h0	Microwire Control Register (MDD) Defines the direction of the data word when the Microwire serial protocol is used. When this bit is set to 0, the data word is received by the SPI bus controller MacroCell from the external serial device. When this bit is set to 1, the data word is transmitted from the SPI bus controller MacroCell to the external serial device.
0	RW/L	1'h0	Microwire Transfer Mode (MWMOD) Defines whether the Microwire transfer is sequential or non-sequential. When sequential mode is used, only one control word is needed to transmit or receive a block of data words. When non-sequential mode is used, there must be a control word for each data word that is transmitted or received. 0 : non-sequential transfer 1 : sequential transfer

Slave Enable Register (SER)

This register is valid only when the SPI bus controller is configured as a master device. When the SPI bus controller is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register enables the individual slave select output lines from the SPI bus controller master. Up to 4 output signals are available per master controller. You cannot write to this register when SPI bus controller is busy.

MEM Offset (B0001000)	10h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 234. Detailed Description of Slave Enable Register (SER)

Bits	Access Type	Default	Description
31:4	RO	28'b0	Reserved 1 (RSVD1) Reserved



Bits	Access Type	Default	Description
3:0	RW/L	4'h0	Slave Select Enable Flag (SER) Each bit in this register corresponds to a slave select line (ss_x_n]) from the SPI bus controller master. When a bit in this register is set (1), the corresponding slave select line from the master is activated when a serial transfer begins. It should be noted that setting or clearing bits in this register have no effect on the corresponding slave select outputs until a transfer is started. Before beginning a transfer, you should enable the bit in this register that corresponds to the slave device with which the master wants to communicate. When not operating in broadcast mode, only one bit in this field should be set. 1: Selected 0: Not Selected

Baud Rate Select (BAUDR)

This register is valid only when the SPI bus controller is configured as a master device. When the SPI bus controller is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register derives the frequency of the serial clock that regulates the data transfer. The 16-bit field in this register defines the ssi_clk divider value. It is impossible to write to this register when the SPI bus controller is enabled. The SPI bus controller is enabled and disabled by writing to the SSIENR register.

MEM Offset (B0001000)	14h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 235. Detailed Description of Baud Rate Select (BAUDR)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW/L	16'h0	SSI Clock Divider (SCKDV) The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation: $F_{sclk\_out} = F_{ssi\_clk} / SCKDV$ Where SCKDV is any even value between 2 and 65534. For example: for $F_{ssi\_clk} = 3.6864\text{MHz}$ and $SCKDV = 2$ $F_{sclk\_out} = 3.6864 / 2 = 1.8432\text{MHz}$



Transmit FIFO Threshold Level (TXFTLR)

This register controls the threshold value for the transmit FIFO memory. The SPI bus controller is enabled and disabled by writing to the SSIENR register.

MEM Offset (B0001000)	18h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 236. Detailed Description of Transmit FIFO Threshold Level (TXFTLR)

Bits	Access Type	Default	Description
31:3	RO	29'b0	Reserved 1 (RSVD1) Reserved
2:0	RW	3'b0	Transmit FIFO Threshold (TXFTLR) Controls the level of entries (or below) at which the transmit FIFO controller triggers an interrupt. If you attempt to set register field to a value greater than or equal to the depth of the FIFO, this field is not written and retains its current value. When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered. For field decode, refer to Table 6-4 of the SPI bus controller databook.

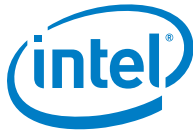
Receive FIFO Threshold Level (RXFTLR)

This register controls the threshold value for the receive FIFO memory. The SPI bus controller is enabled and disabled by writing to the SSIENR register.

MEM Offset (B0001000)	1Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 237. Detailed Description of Receive FIFO Threshold Level (RXFTLR)

Bits	Access Type	Default	Description
31:3	RO	29'b0	Reserved 1 (RSVD1) Reserved



Bits	Access Type	Default	Description
2:0	RW	3'h0	Receive FIFO Threshold (RFT) Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt. If you attempt to set this value greater than the depth of the FIFO, this field is not written and retains its current value. When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered. For field decode, refer to Table 6-5 of the SPI bus controller databook.

Transmit FIFO Level Register (TXFLR)

MEM Offset (B0001000)	20h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 238. Detailed Description of Transmit FIFO Level Register (TXFLR)

Bits	Access Type	Default	Description
31:4	RO	28'b0	Reserved 1 (RSVD1) Reserved
3:0	RO	4'h0	Transmit FIFO Level (TXTFL) Contains the number of valid data entries in the transmit FIFO.

Receive FIFO Level Register (RXFLR)

MEM Offset (B0001000)	24h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 239. Detailed Description of Receive FIFO Level Register (RXFLR)

Bits	Access Type	Default	Description
31:4	RO	28'b0	Reserved 1 (RSVD1) Reserved
3:0	RO	4'h0	Receive FIFO Level (RXFLR) Contains the number of valid data entries in the receive FIFO.



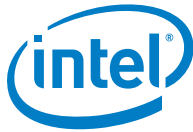
Status Register (SR)

This is a read-only register used to indicate the current transfer status, FIFO status, and any transmission/reception errors that may have occurred. The status register may be read at any time. None of the bits in this register request an interrupt.

MEM Offset (B0001000)	28h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0006h

Table 240. Detailed Description of Status Register (SR)

Bits	Access Type	Default	Description
31:7	RO	25'h0	Reserved 1 (RSVD1) Reserved
6	RO	1'h0	RSVD (RSVD) Reserved
5	RO	1'h0	Transmission Error (TXE) Set if the transmit FIFO is empty when a transfer is started. This bit can be set only when the SPI bus controller is configured as a slave device. Data from the previous transmission is resent on the txd line. This bit is cleared when read. 0 : No error 1 : Transmission error
4	RO	1'h0	Receive FIFO Full (RFF) When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0 : Receive FIFO is not full 1 : Receive FIFO is full
3	RO	1'h0	Receive FIFO Not Empty (RFNE) Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. This bit can be polled by software to completely empty the receive FIFO. 0 : Receive FIFO is empty 1 : Receive FIFO is not empty
2	RO	1'h1	Transmit FIFO Empty (TFE) When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0 : Transmit FIFO is not empty 1 : Transmit FIFO is empty



Bits	Access Type	Default	Description
1	RO	1'h1	Transmit FIFO Not Full (TFNF) Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0 : Transmit FIFO is full 1 : Transmit FIFO is not full
0	RO	1'h0	SSI Busy Flag (BUSY) When set, indicates that a serial transfer is in progress; when cleared indicates that the SPI bus controller is idle or disabled. 0 : SPI bus controller is idle or disabled 1 : SPI bus controller is actively transferring data

Interrupt Mask Register (IMR)

This read/write register masks or enables all interrupts generated by the SPI bus controller.

MEM Offset (B0001000)	2Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_003Fh

Table 241. Detailed Description of Interrupt Mask Register (IMR)

Bits	Access Type	Default	Description
31:6	RO	26'b0	Reserved 1 (RSVD1) Reserved
5	RO	1'h1	RSVD (RSVD) Reserved
4	RW	1'h1	Receive FIFO Full Interrupt Mask (RXFIM) 0 : ssi_rxf_intr interrupt is masked 1 : ssi_rxf_intr interrupt is not masked
3	RW	1'h1	Receive FIFO Overflow Interrupt Mask (RXOIM) 0 : ssi_rxo_intr interrupt is masked 1 : ssi_rxo_intr interrupt is not masked
2	RW	1'h1	Receive FIFO Underflow Interrupt Mask (RXUIM) 0 : ssi_rxu_intr interrupt is masked 1 : ssi_rxu_intr interrupt is not masked
1	RW	1'h1	Transmit FIFO Overflow Interrupt Mask (TXOIM) 0 : ssi_txo_intr interrupt is masked 1 : ssi_txo_intr interrupt is not masked



Bits	Access Type	Default	Description
0	RW	1'h1	Transmit FIFO Empty Interrupt Mask (TXEIM) 0 : ssi_txe_intr interrupt is masked 1 : ssi_txe_intr interrupt is not masked

Interrupt Status Register (ISR)

This register reports the status of the SPI bus controller interrupts after they have been masked.

MEM Offset (B0001000)	30h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

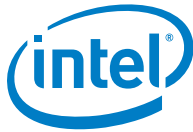
Table 242. Detailed Description of Interrupt Status Register (ISR)

Bits	Access Type	Default	Description
31:6	RO	26'b0	Reserved 1 (RSVD1) Reserved
5	RO	1'h0	RSVD (RSVD) Reserved
4	RO	1'h0	Receive FIFO Full Interrupt Status (RXFIS) 0 : ssi_rxf_intr interrupt is not active after masking 1 : ssi_rxf_intr interrupt is active after masking
3	RO	1'h0	Receive FIFO Overflow Interrupt Status (RXOIS) 0 : ssi_rxo_intr interrupt is active after masking 1 : ssi_rxo_intr interrupt is not active after masking
2	RO	1'h0	Receive FIFO Underflow Interrupt Status (RXUIS) 0 : ssi_rxu_intr interrupt is not active after masking 1 : ssi_rxu_intr interrupt is active after masking
1	RO	1'h0	Transmit FIFO Overflow Interrupt Status (TXOIS) 0 : ssi_txo_intr interrupt is not active after masking 1 : ssi_txo_intr interrupt is active after masking
0	RO	1'h0	Transmit FIFO Empty Interrupt Status (TXEIS) 0 : ssi_txe_intr interrupt is not active after masking 1 : ssi_txe_intr interrupt is active after masking

Raw Interrupt Status Register (RISR)

This register reports the status of the SPI bus controller interrupts prior to masking.

MEM Offset (B0001000)	34h
Security_PolicyGroup	



IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 243. Detailed Description of Raw Interrupt Status Register (RISR)

Bits	Access Type	Default	Description
31:6	RO	26'b0	Reserved 1 (RSVD1) Reserved
5	RO	1'h0	RSVD (RSVD) Reserved
4	RO	1'h0	Receive FIFO Full Raw Interrupt Status (RXFIR) 0 : ssi_rxf_intr interrupt is not active prior masking 1 : ssi_rxf_intr interrupt is active prior masking
3	RO	1'h0	Receive FIFO Overflow Raw Interrupt Status (RXOIR) 0 : ssi_rxo_intr interrupt is active prior masking 1 : ssi_rxo_intr interrupt is not active prior masking
2	RO	1'h0	Receive FIFO Underflow Raw Interrupt Status (RXUIR) 0 : ssi_rxu_intr interrupt is not active prior masking 1 : ssi_rxu_intr interrupt is active prior masking
1	RO	1'h0	Transmit FIFO Overflow Raw Interrupt Status (TXOIR) 0 : ssi_txo_intr interrupt is not active prior masking 1 : ssi_txo_intr interrupt is active prior masking
0	RO	1'h0	Transmit FIFO Empty Raw Interrupt Status (TXEIR) 0 : ssi_txe_intr interrupt is not active prior masking 1 : ssi_txe_intr interrupt is active prior masking

Transmit FIFO Overflow Interrupt Clear Register (TXOICR)

MEM Offset (B0001000)	38h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 244. Detailed Description of Transmit FIFO Overflow Interrupt Clear Register (TXOICR)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved 1 (RSVD1) Reserved
0	RO/C	1'h0	Clear Transmit FIFO Overflow Interrupt (TXOICR) This register reflects the status of the interrupt. A read from this register clears the ssi_txo_intr interrupt; writing has no effect.



Receive FIFO Overflow Interrupt Clear Register (RXOICR)

MEM Offset (B0001000) 3Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 245. Detailed Description of Receive FIFO Overflow Interrupt Clear Register (RXOICR)

Bits	Access Type	Default	Description
31:1	RO/C	31'b0	Reserved 1 (RSVD1) Reserved
0	RO/C	1'h0	Clear Receive FIFO Overflow Interrupt (RXOICR) This register reflects the status of the interrupt. A read from this register clears the ssi_rxo_intr interrupt; writing has no effect.

Receive FIFO Underflow Interrupt Clear Register (RXUICR)

MEM Offset (B0001000) 40h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 246. Detailed Description of Receive FIFO Underflow Interrupt Clear Register (RXUICR)

Bits	Access Type	Default	Description
31:1	RO	31'h0	Reserved 1 (RSVD1) Reserved
0	RO/C	1'h0	Clear Receive FIFO Underflow Interrupt (RXUICR) This register reflects the status of the interrupt. A read from this register clears the ssi_rxu_intr interrupt; writing has no effect.

Multi-Master Interrupt Clear Register (MSTICR)

MEM Offset (B0001000) 44h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h



Table 247. Detailed Description of Multi-Master Interrupt Clear Register (MSTICR)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved 1 (RSVD1) Reserved
0	RO	1'h0	RSVD (RSVD) Reserved

Interrupt Clear Register (ICR)

MEM Offset (B0001000)	48h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 248. Detailed Description of Interrupt Clear Register (ICR)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved 1 (RSVD1) Reserved
0	RO/C	1'h0	Interrupt Clear Register (ICR) This register is set if any of the interrupts below are active. A read clears the ssi_txo_intr, ssi_rxu_intr, ssi_rxo_intr, and the ssi_mst_intr interrupts. Writing to this register has no effect.

DMA Control Register (DMACR)

The register is used to enable the DMA Controller interface operation.

MEM Offset (B0001000)	4Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 249. Detailed Description of DMA Control Register (DMACR)

Bits	Access Type	Default	Description
31:2	RO	30'h0	Reserved 1 (RSVD1) Reserved
1	RW	1'h0	Transmit DMA Enable (TDMAE) This bit enables/disables the transmit FIFO DMA channel. 0 = Transmit DMA disabled 1 = Transmit DMA enabled



Bits	Access Type	Default	Description
0	RW	1'h0	Receive DMA Enable (RDMAE) This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled

DMA Transmit Data Level (DMATDLR)

MEM Offset (B0001000)	50h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 250. Detailed Description of DMA Transmit Data Level (DMATDLR)

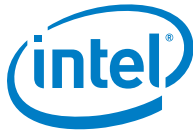
Bits	Access Type	Default	Description
31:3	RO	29'h0	Reserved 1 (RSVD1) Reserved
2:0	RW	3'h0	DMA Transmit Data Level (DMATDL) Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1. Refer to Table 6-2 for the field decode of the SPI bus controller databook.

DMA Receive Data Level (DMARDLR)

MEM Offset (B0001000)	54h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 251. Detailed Description of DMA Receive Data Level (DMARDLR)

Bits	Access Type	Default	Description
31:3	RO	29'b0	Reserved 1 (RSVD1) Reserved
2:0	RW	3'h0	Receive Data Level (DMARDL) This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and RDMAE=1.



Identification Register (IDR)

This read-only register is available for use to store a peripheral identification code.

MEM Offset (B0001000)	58h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 252. Detailed Description of Identification Register (IDR)

Bits	Access Type	Default	Description
31:0	RO	32'h0	Identification Code (IDCODE) This register contains the peripherals identification code, which is written into the register at configuration time using coreConsultant.

coreKit Version ID register (SSI_COMP_VERSION)

This read-only register stores the specific SPI bus controller component version.

MEM Offset (B0001000)	5Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	3332_332Ah

Table 253. Detailed Description of coreKit Version ID register (SSI_COMP_VERSION)

Bits	Access Type	Default	Description
31:0	RO	32'h3332332a	SSI Component Version (SSI_COMP_VERSION) Contains the hex representation of the component version. Consists of ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*. @@jstokes - NOTE : reset value will change with the release for 32b support

Data Register (DR0)

The SPI bus controller data register is a 32-bit wide that supports 32-bit transfers. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data



from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 60h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 254. Detailed Description of Data Register (DR0)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR1)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 64h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 255. Detailed Description of Data Register (DR1)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved



Bits	Access Type	Default	Description
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR2)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	68h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 256. Detailed Description of Data Register (DR2)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR3)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the



transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 6Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 257. Detailed Description of Data Register (DR3)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR4)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 70h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 258. Detailed Description of Data Register (DR4)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved



Bits	Access Type	Default	Description
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR5)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	74h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 259. Detailed Description of Data Register (DR5)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR6)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the



transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 78h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 260. Detailed Description of Data Register (DR6)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR7)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 7Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 261. Detailed Description of Data Register (DR7)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved



Bits	Access Type	Default	Description
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR8)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	80h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 262. Detailed Description of Data Register (DR8)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR9)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the



transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 84h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 263. Detailed Description of Data Register (DR9)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR10)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 88h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 264. Detailed Description of Data Register (DR10)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved



Bits	Access Type	Default	Description
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR11)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	8Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 265. Detailed Description of Data Register (DR11)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR12)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address



locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 90h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 266. Detailed Description of Data Register (DR12)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR13)

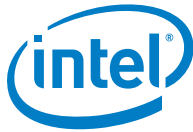
The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 94h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 267. Detailed Description of Data Register (DR13)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved



Bits	Access Type	Default	Description
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR14)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	98h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 268. Detailed Description of Data Register (DR14)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR15)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the



transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 9Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 269. Detailed Description of Data Register (DR15)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR16)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 0A0h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 270. Detailed Description of Data Register (DR16)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved



Bits	Access Type	Default	Description
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR17)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	0A4h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 271. Detailed Description of Data Register (DR17)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR18)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the



transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	0A8h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 272. Detailed Description of Data Register (DR18)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR19)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	0ACh
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 273. Detailed Description of Data Register (DR19)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved



Bits	Access Type	Default	Description
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR20)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	0B0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 274. Detailed Description of Data Register (DR20)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR21)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the



transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 0B4h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 275. Detailed Description of Data Register (DR21)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR22)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 0B8h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 276. Detailed Description of Data Register (DR22)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved



Bits	Access Type	Default	Description
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR23)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	0BCh
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 277. Detailed Description of Data Register (DR23)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR24)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the



transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 0C0h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 278. Detailed Description of Data Register (DR24)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR25)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 0C4h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 279. Detailed Description of Data Register (DR25)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved



Bits	Access Type	Default	Description
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR26)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwrdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	0C8h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 280. Detailed Description of Data Register (DR26)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR27)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from



the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	0CCh
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 281. Detailed Description of Data Register (DR27)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR28)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	0D0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 282. Detailed Description of Data Register (DR28)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved



Bits	Access Type	Default	Description
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR29)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	0D4h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 283. Detailed Description of Data Register (DR29)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR30)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the



transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	0D8h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 284. Detailed Description of Data Register (DR30)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR31)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	0DCh
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 285. Detailed Description of Data Register (DR31)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved



Bits	Access Type	Default	Description
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR32)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	0E0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 286. Detailed Description of Data Register (DR32)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR33)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the



transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 0E4h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 287. Detailed Description of Data Register (DR33)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR34)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000) 0E8h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 288. Detailed Description of Data Register (DR34)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved



Bits	Access Type	Default	Description
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

Data Register (DR35)

The SPI bus controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Note: The DR register in the SPI bus controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI bus controller are not addressable.

MEM Offset (B0001000)	0ECh
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 289. Detailed Description of Data Register (DR35)

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved 1 (RSVD1) Reserved
15:0	RW	16'h0	Data Register (DR) When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer

RX Sample Delay Register (RX_SAMPLE_DLY)

This register controls the number of ssi_clk cycles that are delayed, from the default sample time, before the actual sample of the rxd input signal occurs. It is impossible to write to this register when the SPI bus controller is enabled; the SPI bus controller is enabled and disabled by writing to the SSIENR register.

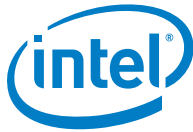
MEM Offset (B0001000)	0F0h
Security_PolicyGroup	



IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 290. Detailed Description of RX Sample Delay Register (RX_SAMPLE_DLY)

Bits	Access Type	Default	Description
31:4	RO	28'h0	Reserved 1 (RSVD1) Reserved
3:0	RW/L	4'h0	Receive Data Sample Delay (RSD) This register is used to delay the sample of the rxd input signal. Each value represents a single ssi_clk delay on the sample of the rxd signal.



20 DMA Controller

The Intel® Quark™ SE Microcontroller C1000 contains a single 8-Channel DMA controller. The DMA controller supports Single or Multi-Block transfers from Memory to Memory, Peripheral to Memory, Memory to Peripheral or Peripheral to Peripheral.

20.1 Features

The following is a list of the DMA controller features:

- 8 unidirectional channels
- Configurable channel prioritization
- Software handshaking
- Hardware handshaking interfaces
- Configurable transfer type and flow control
- Supports single-block transfers
- Supports multi-block transfers
- Scatter-Gather
- Interrupt generation per channel:
 - DMA Transfer Complete
 - Block Transfer Complete
 - Source Transaction Complete
 - Destination Transaction Complete
 - Error Response

20.2 Use

DMA transfers are initiated either through software or hardware handshaking interfaces. The handshaking interface is configurable on a per channel basis. The following hardware handshaking interfaces are available for selection.

Table 291. Hardware Handshake Interfaces

Interface ID	Peripheral
0	UART 0 TX
1	UART 0 RX
2	UART 1 TX
3	UART 1 RX
4	SPI Master 0 TX



Interface ID	Peripheral
5	SPI Master 0 RX
6	SPI Master 1 TX
7	SPI Master 1 RX
8	SPI Slave TX
9	SPI Slave RX
10	I2S TX
11	I2S RX
12	I2C Master 0 TX
13	I2C Master 0 RX
14	I2C Master 1 TX
15	I2C Master 1 RX

Transfer type and flow control are configurable on a per channel basis. The following flow control options are available depending on the transfer type.

Table 292. Transfer Type and Flow Control Options

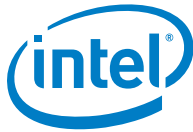
Transfer Type	Supported Flow Control Agent(s)
Memory to Memory	DMA Controller
Peripheral to Memory	DMA Controller or Peripheral
Memory to Peripheral	DMA Controller or Peripheral
Peripheral to Peripheral	DMA Controller or Source Peripheral or Destination Peripheral

Multi-block transfers are achieved through the following:

- Linked List (Block Chaining)
- Address Auto-Reloading
- Contiguous Addressing

There are five possible sources for channel interrupts. Each of these sources can be individually masked. The sources are listed below:

- DMA Transfer Complete: generated on DMA transfer completion to the Destination Peripheral.
- Block Transfer Complete: generated on DMA block transfer completion to the Destination Peripheral.



- Source Transaction Complete: generated after completion of the last AHB transfer of the requested single/burst transaction from the handshaking interface (either the hardware or software handshaking interface) on the source side.
- Destination Transaction Complete: generated after completion of the last AHB transfer of the requested single/burst transaction from the handshaking interface (either the hardware or software handshaking interface) on the destination side.
- Error Response: generated when an ERROR response is received from an AHB slave on the HRESP bus during a DMA transfer.

In the event of an ERROR response, the DMA transfer is cancelled and the corresponding channel is disabled. An Error Response interrupt will be generated if the channel is configured to do so.

20.3 Memory Mapped IO Registers

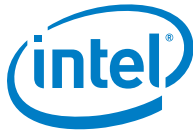
Registers listed are for the DMA Controller, starting at base address B0700000h.

Table 293. Summary of DMA Registers—0xB0700000

MEM Address	Default	Instance Name	Name
0x000	0000_0000h	SAR[0]	Channel 0 Source Address
0x058	0000_0000h	SAR[1]	Channel 0 Source Address
0x0B0	0000_0000h	SAR[2]	Channel 0 Source Address
0x108	0000_0000h	SAR[3]	Channel 0 Source Address
0x160	0000_0000h	SAR[4]	Channel 0 Source Address
0x1B8	0000_0000h	SAR[5]	Channel 0 Source Address
0x210	0000_0000h	SAR[6]	Channel 0 Source Address
0x268	0000_0000h	SAR[7]	Channel 0 Source Address
0x008	0000_0000h	DAR[0]	Channel 0 Destination Address
0x060	0000_0000h	DAR[1]	Channel 0 Destination Address
0x0B8	0000_0000h	DAR[2]	Channel 0 Destination Address
0x110	0000_0000h	DAR[3]	Channel 0 Destination Address
0x168	0000_0000h	DAR[4]	Channel 0 Destination Address
0x1C0	0000_0000h	DAR[5]	Channel 0 Destination Address
0x218	0000_0000h	DAR[6]	Channel 0 Destination Address
0x270	0000_0000h	DAR[7]	Channel 0 Destination Address
0x010	0000_0000h	LLP[0]	Channel 0 Linked List Pointer
0x068	0000_0000h	LLP[1]	Channel 0 Linked List Pointer
0x0C0	0000_0000h	LLP[2]	Channel 0 Linked List Pointer



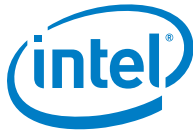
MEM Address	Default	Instance Name	Name
0x118	0000_0000h	LLP[3]	Channel 0 Linked List Pointer
0x170	0000_0000h	LLP[4]	Channel 0 Linked List Pointer
0x1C8	0000_0000h	LLP[5]	Channel 0 Linked List Pointer
0x220	0000_0000h	LLP[6]	Channel 0 Linked List Pointer
0x278	0000_0000h	LLP[7]	Channel 0 Linked List Pointer
0x018	0036_4825h	CTL_L[0]	Channel 0 Control LOWER
0x070	0036_4825h	CTL_L[1]	Channel 0 Control LOWER
0x0C8	0036_4825h	CTL_L[2]	Channel 0 Control LOWER
0x120	0036_4825h	CTL_L[3]	Channel 0 Control LOWER
0x178	0036_4825h	CTL_L[4]	Channel 0 Control LOWER
0x1D0	0036_4825h	CTL_L[5]	Channel 0 Control LOWER
0x228	0036_4825h	CTL_L[6]	Channel 0 Control LOWER
0x280	0036_4825h	CTL_L[7]	Channel 0 Control LOWER
0x01C	0000_0002h	CTL_U[0]	Channel 0 Control UPPER
0x074	0000_0002h	CTL_U[1]	Channel 0 Control UPPER
0x0CC	0000_0002h	CTL_U[2]	Channel 0 Control UPPER
0x124	0000_0002h	CTL_U[3]	Channel 0 Control UPPER
0x17C	0000_0002h	CTL_U[4]	Channel 0 Control UPPER
0x1D4	0000_0002h	CTL_U[5]	Channel 0 Control UPPER
0x22C	0000_0002h	CTL_U[6]	Channel 0 Control UPPER
0x284	0000_0002h	CTL_U[7]	Channel 0 Control UPPER
0x020	0000_0000h	SSTAT[0]	Channel 0 Source Status
0x078	0000_0000h	SSTAT[1]	Channel 0 Source Status
0x0D0	0000_0000h	SSTAT[2]	Channel 0 Source Status
0x128	0000_0000h	SSTAT[3]	Channel 0 Source Status
0x180	0000_0000h	SSTAT[4]	Channel 0 Source Status
0x1D8	0000_0000h	SSTAT[5]	Channel 0 Source Status
0x230	0000_0000h	SSTAT[6]	Channel 0 Source Status
0x288	0000_0000h	SSTAT[7]	Channel 0 Source Status
0x028	0000_0000h	DSTAT[0]	Channel 0 Destination Status
0x080	0000_0000h	DSTAT[1]	Channel 0 Destination Status
0x0D8	0000_0000h	DSTAT[2]	Channel 0 Destination Status
0x130	0000_0000h	DSTAT[3]	Channel 0 Destination Status
0x188	0000_0000h	DSTAT[4]	Channel 0 Destination Status
0x1E0	0000_0000h	DSTAT[5]	Channel 0 Destination Status



MEM Address	Default	Instance Name	Name
0x238	0000_0000h	DSTAT[6]	Channel 0 Destination Status
0x290	0000_0000h	DSTAT[7]	Channel 0 Destination Status
0x030	0000_0000h	SSTATAR[0]	Channel 0 Source Status Address
0x088	0000_0000h	SSTATAR[1]	Channel 0 Source Status Address
0x0E0	0000_0000h	SSTATAR[2]	Channel 0 Source Status Address
0x138	0000_0000h	SSTATAR[3]	Channel 0 Source Status Address
0x190	0000_0000h	SSTATAR[4]	Channel 0 Source Status Address
0x1E8	0000_0000h	SSTATAR[5]	Channel 0 Source Status Address
0x240	0000_0000h	SSTATAR[6]	Channel 0 Source Status Address
0x298	0000_0000h	SSTATAR[7]	Channel 0 Source Status Address
0x038	0000_0000h	DSTATAR[0]	Channel 0 Destination Status Address
0x090	0000_0000h	DSTATAR[1]	Channel 0 Destination Status Address
0x0E8	0000_0000h	DSTATAR[2]	Channel 0 Destination Status Address
0x140	0000_0000h	DSTATAR[3]	Channel 0 Destination Status Address
0x198	0000_0000h	DSTATAR[4]	Channel 0 Destination Status Address
0x1F0	0000_0000h	DSTATAR[5]	Channel 0 Destination Status Address
0x248	0000_0000h	DSTATAR[6]	Channel 0 Destination Status Address
0x2A0	0000_0000h	DSTATAR[7]	Channel 0 Destination Status Address
0x040	0000_0EE0h	CFG_L[0]	Channel 0 Configuration LOWER
0x098	0000_0EE0h	CFG_L[1]	Channel 0 Configuration LOWER
0x0F0	0000_0EE0h	CFG_L[2]	Channel 0 Configuration LOWER
0x148	0000_0EE0h	CFG_L[3]	Channel 0 Configuration LOWER
0x1A0	0000_0EE0h	CFG_L[4]	Channel 0 Configuration LOWER
0x1F8	0000_0EE0h	CFG_L[5]	Channel 0 Configuration LOWER
0x250	0000_0EE0h	CFG_L[6]	Channel 0 Configuration LOWER
0x2A8	0000_0EE0h	CFG_L[7]	Channel 0 Configuration LOWER
0x044	0000_0004h	CFG_U[0]	Channel 0 configuration UPPER
0x09C	0000_0004h	CFG_U[1]	Channel 0 configuration UPPER
0x0F4	0000_0004h	CFG_U[2]	Channel 0 configuration UPPER
0x14C	0000_0004h	CFG_U[3]	Channel 0 configuration UPPER
0x1A4	0000_0004h	CFG_U[4]	Channel 0 configuration UPPER
0x1FC	0000_0004h	CFG_U[5]	Channel 0 configuration UPPER
0x254	0000_0004h	CFG_U[6]	Channel 0 configuration UPPER
0x2AC	0000_0004h	CFG_U[7]	Channel 0 configuration UPPER
0x048	0000_0000h	SGR[0]	Channel 0 Source Gather



MEM Address	Default	Instance Name	Name
0x0A0	0000_0000h	SGR[1]	Channel 0 Source Gather
0x0F8	0000_0000h	SGR[2]	Channel 0 Source Gather
0x150	0000_0000h	SGR[3]	Channel 0 Source Gather
0x1A8	0000_0000h	SGR[4]	Channel 0 Source Gather
0x200	0000_0000h	SGR[5]	Channel 0 Source Gather
0x258	0000_0000h	SGR[6]	Channel 0 Source Gather
0x2B0	0000_0000h	SGR[7]	Channel 0 Source Gather
0x050	0000_0000h	DSR[0]	Channel 0 Destination Scatter
0x0A8	0000_0000h	DSR[1]	Channel 0 Destination Scatter
0x100	0000_0000h	DSR[2]	Channel 0 Destination Scatter
0x158	0000_0000h	DSR[3]	Channel 0 Destination Scatter
0x1B0	0000_0000h	DSR[4]	Channel 0 Destination Scatter
0x208	0000_0000h	DSR[5]	Channel 0 Destination Scatter
0x260	0000_0000h	DSR[6]	Channel 0 Destination Scatter
0x2B8	0000_0000h	DSR[7]	Channel 0 Destination Scatter
0x2C0	0000_0000h	RAW_TFR	Raw Status for IntTfr Interrupt
0x2C8	0000_0000h	RAW_BLOCK	Raw Status for IntBlock Interrupt
0x2D0	0000_0000h	RAW_SRC_TRAN	Raw Status for IntSrcTran Interrupt
0x2D8	0000_0000h	RAW_DST_TRAN	Raw Status for IntDstTran Interrupt
0x2E0	0000_0000h	RAW_ERR	Raw Status for IntErr Interrupt
0x2E8	0000_0000h	STATUS_TFR	Status for IntTfr Interrupt
0x2F0	0000_0000h	STATUS_BLOCK	Status for IntBlock Interrupt
0x2F8	0000_0000h	STATUS_SRC_TRAN	Status for IntSrcTran Interrupt
0x300	0000_0000h	STATUS_DST_TRAN	Status for IntDstTran Interrupt
0x308	0000_0000h	STATUS_ERR	Status for IntErr Interrupt
0x310	0000_0000h	MASK_TFR	Mask for IntTfr Interrupt
0x318	0000_0000h	MASK_BLOCK	Mask for IntBlock Interrupt
0x320	0000_0000h	MASK_SRC_TRAN	Mask for IntSrcTran Interrupt
0x328	0000_0000h	MASK_DST_TRAN	Mask for IntDstTran Interrupt
0x330	0000_0000h	MASK_ERR	Mask for IntErr Interrupt
0x338	0000_0000h	CLEAR_TFR	Clear for IntTfr Interrupt
0x340	0000_0000h	CLEAR_BLOCK	Clear for IntBlock Interrupt
0x348	0000_0000h	CLEAR_SRC_TRAN	Clear for IntSrcTran Interrupt
0x350	0000_0000h	CLEAR_DST_TRAN	Clear for IntDstTran Interrupt
0x358	0000_0000h	CLEAR_ERR	Clear for IntErr Interrupt



MEM Address	Default	Instance Name	Name
0x360	0000_0000h	STATUS_INT	Combined Interrupt Status
0x368	0000_0000h	REQ_SRC_REG	Source Software Transaction Request
0x370	0000_0000h	REQ_DST_REG	Destination Software Transaction Request register
0x378	0000_0000h	SGL_REQ_SRC_REG	Source Single Transaction Request
0x380	0000_0000h	SGL_REQ_DST_REG	Destination Single Software Transaction Request
0x388	0000_0000h	LST_SRC_REG	Source Last Transaction Request
0x390	0000_0000h	LST_DST_REG	Destination Single Transaction Request
0x398	0000_0000h	DMA_CFG_REG	DMA Configuration
0x3A0	0000_0000h	CH_EN_REG	Channel Enable
0x3A8	0000_0000h	DMA_ID_REG	DMA ID
0x3B0	0000_0000h	DMA_TEST_REG	DMA Test
0x3F8	4457_1110h	DMA_COMP_ID_L	DMA Component ID - LOWER
0x3FC	3231_382Ah	DMA_COMP_ID_U	DMA Component ID - UPPER

Channel 0 Source Address (SAR [0..7])

Source Address of DMA transfer.

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer.

While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

MEM Offset ()	[0]:0h [1]:58h [2]:0B0h [3]:108h [4]:160h [5]:1B8h [6]:210h [7]:268h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 294. Detailed Description of Channel 0 Source Address (SAR [0..7])

Bits	Access Type	Default	Description
31:0	RW	32'b0	Current Source Address of DMA transfer (SAR) Updated after each source transfer. The SINC field in the CTLO_L register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

Channel 0 Destination Address (DAR [0..7])

Destination address of DMA transfer.



The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

MEM Offset ()	[0]:8h [1]:60h [2]:0B8h [3]:110h [4]:168h [5]:1C0h [6]:218h [7]:270h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 295. Detailed Description of Channel 0 Destination Address (DAR [0..7])

Bits	Access Type	Default	Description
31:0	RW	32'b0	Current Destination address of DMA transfer (DAR) Updated after each destination transfer. The DINC field in the CTLO_L register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

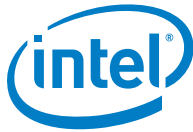
Channel 0 Linked List Pointer (LLP [0..7])

Program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled

MEM Offset ()	[0]:10h [1]:68h [2]:0C0h [3]:118h [4]:170h [5]:1C8h [6]:220h [7]:278h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 296. Detailed Description of Channel 0 Linked List Pointer (LLP [0..7])

Bits	Access Type	Default	Description
31:2	RW	30'b0	Starting Address In Memory (LOC) Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses (Hsize = 2) aligned to 32-bit boundaries and cannot be changed or programmed to anything other than 32-bit.
1:0	RO	2'b0	Reserved (RSV)



Channel 0 Control LOWER (CTL_L [0..7])

Contains fields that control the DMA transfer.

Part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

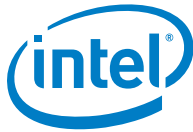
MEM Offset ()	[0]:18h [1]:70h [2]:0C8h [3]:120h [4]:178h [5]:1D0h [6]:228h [7]:280h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0036_4825h

Table 297. Detailed Description of Channel 0 Control LOWER (CTL_L [0..7])

Bits	Access Type	Default	Description
31:29	RO	3'b0	Reserved (RSV2)
28	RW	1'b0	LLP_SRC_EN (LLP_SRC_EN) Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	RW	1'b0	LLP_DST_EN (LLP_DST_EN) Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLP0.LOC is non-zero
26:25	RO	2'b0	Source AMBA Layer (SMS) Hardcoded the Master interface attached to the source of channel 0.
24:23	RO	2'b0	Destination AMBA Layer (DMS) Hardcoded the Master interface attached to the destination of channel 0



Bits	Access Type	Default	Description
22:20	RW	3'b011	Transfer Type and Flow Control (TT_FC) The following transfer types are supported for Channel 0: Code - Type - Flow Controller ----- 000 - Memory to Memory - DMAC ----- 001 - Memory to Peripheral - DMAC ----- 010 - Peripheral to Memory - DMAC ----- 011 - Peripheral to Peripheral - DMAC ----- 100 - Peripheral to Memory - Peripheral ----- 101 - Peripheral to Peripheral - Source Peripheral ----- 110 - Memory to Peripheral - Peripheral ----- 111 - Peripheral to Peripheral - Destination Peripheral -----
19	RO	1'b0	Reserved (RSV0)
18	RW	1'b1	Destination scatter enable (DST_SCATTER_EN) 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTLO_L.DINC bit indicates an incrementing or decrementing address control.
17	RW	1'b1	Source gather enable (SRC_GATHER_EN) 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTLO_L.SINC bit indicates an incrementing or decrementing address control.



Bits	Access Type	Default	Description
16:14	RW	3'b001	Source Burst Transaction Length (SRC_MSIZ) Number of data items, each of width CTL0_L.SRC_TR_WIDTH, to be read from the source every time a source burst transaction request is made from either the corresponding hardware or software handshaking interface. Value - Size(#TR_WITDH) ----- 000 - 1 001 - 4 010 - 8 011 - 16 100 - 32 101 - 64 110 - 128 111 - 256
13:11	RW	3'b001	Destination Burst Transaction Length (DEST_MSIZ) Destination Burst Transaction Length. Number of data items, each of width CTL0_L.DST_TR_WIDTH, to be written to the destination every time a destination burst transaction request is made from either the corresponding hardware or software handshaking interface. Value - Size(#TR_WITDH) ----- 000 - 1 001 - 4 010 - 8 011 - 16 100 - 32 101 - 64 110 - 128 111 - 256
10:9	RW	2'b0	Source Address Increment (SINC) Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 00 = Increment 01 = Decrement 1x = No change NOTE: Incrementing or decrementing is done for alignment to the next SRC_TR_WIDTH boundary.

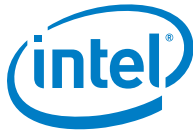


Bits	Access Type	Default	Description
8:7	RW	2'b0	Destination Address Increment (DINC) Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change 00 = Increment 01 = Decrement 1x = No change NOTE: Incrementing or decrementing is done for alignment to the next DST_TR_WIDTH boundary.
6:4	RW	3'b010	Source transfer width (SRC_TR_WIDTH) Decoding for this field: Value - Size(bits) ----- 000 - 8 001 - 16 010 - 32 011 - 64 100 - 128 101 - 256 11x - 256
3:1	RW	3'b010	Destination transfer width (DST_TR_WIDTH) Decoding for this field: Value - Size(bits) ----- 000 - 8 001 - 16 010 - 32 011 - 64 100 - 128 101 - 256 11x - 256
0	RW	1'b1	Interrupt enable (INT_EN) If set, then all interrupt-generating sources are enabled. Functions as a global mask bit for all interrupts for the channel. RAW interrupt registers still assert if INT_EN = 0.

Channel 0 Control UPPER (CTL_U [0..7])

Contains fields that control the DMA transfer.

It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, the content is written to the control register location of the LLI in system memory at the end of the block transfer.



MEM Offset ()	[0]:1Ch [1]:74h [2]:0CCh [3]:124h [4]:17Ch [5]:1D4h [6]:22Ch [7]:284h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0002h

Table 298. Detailed Description of Channel 0 Control UPPER (CTL_U [0..7])

Bits	Access Type	Default	Description
31:13	RO	19'b0	Reserved (RSV1)
12	RW	1'b0	Done bit (DONE) If status write-back is enabled, the upper word of the control register, CTLO_U[31:0], is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTLO.DONE bit to see when a block transfer is complete. The LLI CTLO.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. LLI accesses are always 32-bit accesses (Hsize = 2) aligned to 32-bit boundaries and cannot be changed or programmed to anything other than 32-bit.
11:0	RW	12'b00000000010	Block length (BLOCK_TS) When the DMAC is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of single transactions to perform for every block transfer. A single transaction is mapped to a single AMBA beat. Width: The width of the single transaction is determined by CTLO_L.SRC_TR_WIDTH.

Channel 0 Source Status (SSTAT [0..7])

This register is a temporary placeholder for the source status information on its way to the SSTAT0 register location of the LLI. The source status information should be retrieved by software from the SSTAT0 register location of the LLI, and not by a read of this register over the DMAC slave interface.

MEM Offset ()	[0]:20h [1]:78h [2]:0D0h [3]:128h [4]:180h [5]:1D8h [6]:230h [7]:288h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 299. Detailed Description of Channel 0 Source Status (SSTAT [0..7])

Bits	Access Type	Default	Description
31:0	RW	32'b0	Channel Source Status (SSTAT) Source status information retrieved by hardware from the address pointed to by the contents of the SSTATAR0 register.

Channel 0 Destination Status (DSTAT [0..7])

This register is a temporary placeholder for the destination status information on its way to the DSTAT0 register location of the LLI. The destination status information should be retrieved by software from the DSTAT0 register location of the LLI and not by a read of this register over the DMAC slave interface

MEM Offset ()	[0]:28h [1]:80h [2]:0D8h [3]:130h [4]:188h [5]:1E0h [6]:238h [7]:290h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 300. Detailed Description of Channel 0 Destination Status (DSTAT [0..7])

Bits	Access Type	Default	Description
31:0	RW	32'b0	Channel Destination Status (DSTAT) Destination status information retrieved by hardware from the address pointed to by the contents of the DSTATAR0 register.

Channel 0 Source Status Address (SSTATAR [0..7])

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of this register.

MEM Offset ()	[0]:30h [1]:88h [2]:0E0h [3]:138h [4]:190h [5]:1E8h [6]:240h [7]:298h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 301. Detailed Description of Channel 0 Source Status Address (SSTATAR [0..7])

Bits	Access Type	Default	Description
31:0	RW	32'b0	Channel Source Status Address (SSTATAR) Pointer from where hardware can fetch the source status information, which is registered in the SSTAT0 register and written out to the SSTAT0 register location of the LLI before the start of the next block.

Channel 0 Destination Status Address (DSTATAR [0..7])

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of this register.

MEM Offset ()	[0]:38h [1]:90h [2]:0E8h [3]:140h [4]:198h [5]:1F0h [6]:248h [7]:2A0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 302. Detailed Description of Channel 0 Destination Status Address (DSTATAR [0..7])

Bits	Access Type	Default	Description
31:0	RW	32'b0	Channel Destination Status Address (DSTATAR) Pointer from where hardware can fetch the destination status information, which is registered in the DSTAT0 register and written out to the DSTAT0 register location of the LLI before the start of the next block.

Channel 0 Configuration LOWER (CFG_L [0..7])

Contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. You need to program this register prior to enabling the channel.

MEM Offset ()	[0]:40h [1]:98h [2]:0F0h [3]:148h [4]:1A0h [5]:1F8h [6]:250h [7]:2A8h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0EE0h



Table 303. Detailed Description of Channel 0 Configuration LOWER (CFG_L [0..7])

Bits	Access Type	Default	Description
31	RW	1'b0	Reload destination enable (RELOAD_DST) The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	RW	1'b0	Reload source enable (RELOAD_SRC) The SAR register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:20	RO	10'b0	Reserved (RSV2)
19	RW	1'b0	Source handshake polarity (SRC_HS_POL) 0 = Active high 1 = Active low
18	RW	1'b0	Destination handshake polarity (DST_HS_POL) 0 = Active high 1 = Active low
17:12	RO	6'b0	Reserved (RSV1)
11	RW	1'b1	Source Handshake select (HS_SEL_SRC) Used to select which handshake interface is active for source requests on this channel 0 = HW handshake. SW ones are ignored 1 = SW handshake. HW ones are ignored If source peripheral is memory this bit is ignored
10	RW	1'b1	Destination Handshake select (HS_SEL_DST) Used to select which handshake interface is active for destination requests on this channel 0 = HW handshake. SW ones are ignored 1 = SW handshake. HW ones are ignored If destination peripheral is memory this bit is ignored
9	RO	1'b1	Channel FIFO empty status (FIFO_EMPTY) Indicates if there is data left in the channel FIFO. Can be used in conjunction with CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	RW	1'b0	Channel Suspend control (CH_SUSP) Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.



Bits	Access Type	Default	Description
7:5	RW	0x7	Channel Priority (CH_PRIOR) Priority value equal to 7 is the highest priority, and 0 is the lowest. This field must be programmed within the following range: 0: 1 A programmed value outside this range will cause erroneous behavior.
4:0	RO	5'b0	Reserved (RSV0)

Channel 0 configuration UPPER (CFG_U [0..7])

Contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. You need to program this register prior to enabling the channel.

MEM Offset ()	[0]:44h [1]:9Ch [2]:0F4h [3]:14Ch [4]:1A4h [5]:1FCh [6]:254h [7]:2ACh
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0004h

Table 304. Detailed Description of Channel 0 configuration UPPER (CFG_U [0..7])

Bits	Access Type	Default	Description
31:15	RO	17'h0	Reserved (RSV5)
14:11	RW	4'h0	Destination hardware interface (DEST_PER) Assigns a hardware handshaking interface (0-1) to the channel destination if the CFG0_LHS_SEL_DST field is 0; otherwise, this field is ignored. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
10:7	RW	4'h0	Source hardware interface (SRC_PER) Assigns a hardware handshaking interface (0-1) to the channel source if the CFG0_LHS_SEL_SRC field is 0; otherwise, this field is ignored. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.



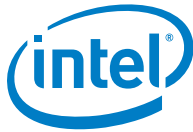
Bits	Access Type	Default	Description
6	RW	1'b0	Source Status Update Enable (SS_UPD_EN) Source status information is fetched only from the location pointed to by the SSTATAR0 register, stored in the SSTAT0 register and written out to the SSTAT0 location of the LLI if this field is high
5	RW	1'b0	Destination Status Update Enable (DS_UPD_EN) Destination status information is fetched only from the location pointed to by the DSTATAR0 register, stored in the DSTAT0 register and written out to the DSTAT0 location of the LLI if this field is high.
4:2	RW	3'b001	AHB bus protocol bus control (PROTCTL) Protection Control bits used to drive the AHB HPROT[3:1] bus. The AMBA Specification recommends that the default value of HPROT indicates a non-cached, non-buffered, privileged data access. The reset value is used to indicate such an access. HPROT[0] is tied high because all transfers are data accesses, as there are no opcode fetches. There is a one-to-one mapping of these register bits to the HPROT[3:1] master interface signals.
1	RW	1'b0	Channel FIFO mode control (FIFO_MODE) Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers. The exceptions are at the end of a burst transaction request or at the end of a block transfer.
0	RW	1'b0	Channel flow control mode (FCMODE) Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs. In this mode, the amount of data transferred from the source is limited so that it is guaranteed to be transferred to the destination prior to block termination by the destination. Data pre-fetching is disabled.

Channel 0 Source Gather (SGR [0..7])

The CTLO_L.SINC field controls whether the address increments or decrements. For a fixed-address control, then the address remains constant throughout the transfer and this register is ignored.

MEM Offset ()

[0]:48h [1]:0A0h [2]:0F8h [3]:150h [4]:1A8h
[5]:200h [6]:258h [7]:2B0h



Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 305. Detailed Description of Channel 0 Source Gather (SGR [0..7])

Bits	Access Type	Default	Description
31:25	RO	7'b0	Reserved (RSV)
24:20	RO	5'b0	Source Gather Count (SGC) Source contiguous transfer count between successive gather boundaries. Specifies the number of contiguous source transfers of CTLO_L.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary
19:0	RO	20'b0	Source Gather Interval (SGI) Specifies the source address increment/decrement in multiples of CTLO_L.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer.

Channel 0 Destination Scatter (DSR [0..7])

The CTLO_L.DINC field controls whether the address increments or decrements. For a fixed-address control, then the address remains constant throughout the transfer and this register is ignored.

MEM Offset () [0]:50h [1]:0A8h [2]:100h [3]:158h [4]:1B0h
[5]:208h [6]:260h [7]:2B8h

Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 306. Detailed Description of Channel 0 Destination Scatter (DSR [0..7])

Bits	Access Type	Default	Description
31:25	RO	7'b0	Reserved (RSV)
24:20	RO	5'b0	Destination Scatter Count (DSC) Source contiguous transfer count between successive scatter boundaries. Specifies the number of contiguous destination transfers of CTLO_L.DST_TR_WIDTH between successive scatter intervals. This is defined as a scatter boundary.
19:0	RO	20'b0	Destination Scatter Interval (DSI) Specifies the destination address increment/decrement in multiples of CTLO_L.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer.



Raw Status for IntTfr Interrupt (RAW_TFR - 0x2C0 + [0..0 * 0x100])

DMA Transfer Complete Interrupt. This interrupt is generated on DMA transfer completion to the destination peripheral.

MEM Offset ()	2C0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 307. Detailed Description of Raw Status for IntTfr Interrupt (RAW_TFR - 0x2C0 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	RW	8'b0	Raw Status for IntTfr Interrupt (RAW) Interrupt events are stored in this Raw Interrupt Status register before masking. Each bit in this register is cleared by writing a 1 to the corresponding location in the correspondent Clear register.

Raw Status for IntBlock Interrupt (RAW_BLOCK - 0x2C8 + [0..0 * 0x100])

Block Transfer Complete Interrupt. This interrupt is generated on DMA block transfer completion to the destination peripheral.

MEM Offset ()	2C8h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 308. Detailed Description of Raw Status for IntBlock Interrupt (RAW_BLOCK - 0x2C8 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	RW	8'b0	Raw Status for IntBlock Interrupt (RAW) Interrupt events are stored in this Raw Interrupt Status register before masking. Each bit in this register is cleared by writing a 1 to the corresponding location in the correspondent Clear register.

Raw Status for IntSrcTran Interrupt (RAW_SRC_TRAN - 0x2D0 + [0..0 * 0x100])

Source Transaction Complete Interrupt. Generated after completion of the last AHB transfer of the requested single/burst transaction from the handshaking interface (either the hardware or software handshaking interface) on the source side. NOTE: If the



source is memory, then IntSrcTran interrupt should be ignored, as there is no concept of a DMA transaction level for memory.

MEM Offset () 2D0h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 309. Detailed Description of Raw Status for IntSrcTran Interrupt (RAW_SRC_TRAN - 0x2D0 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	RW	8'b0	Raw Status for IntSrcTran Interrupt (RAW) Interrupt events are stored in this Raw Interrupt Status register before masking. Each bit in this register is cleared by writing a 1 to the corresponding location in the correspondent Clear register.

Raw Status for IntDstTran Interrupt (RAW_DST_TRAN - 0x2D8 + [0..0 * 0x100])

Destination Transaction Complete Interrupt. Generated after completion of the last AHB transfer of the requested single/burst transaction from the handshaking interface (either the hardware or software handshaking interface) on the destination side. NOTE: If the destination for a channel is memory, then that channel will never generate the IntDstTran interrupt. Because of this, the corresponding bit in this field will not be set.

MEM Offset () 2D8h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 310. Detailed Description of Raw Status for IntDstTran Interrupt (RAW_DST_TRAN - 0x2D8 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	RW	8'b0	Raw Status for IntDstTran Interrupt (RAW) Interrupt events are stored in this Raw Interrupt Status register before masking. Each bit in this register is cleared by writing a 1 to the corresponding location in the correspondent Clear register.



Raw Status for IntErr Interrupt (RAW_ERR - 0x2E0 + [0..0 * 0x100])

Error Interrupt. This interrupt is generated when an ERROR response is received from an AHB slave on the HRESP bus during a DMA transfer. In addition, the DMA transfer is cancelled and the channel is disabled.

MEM Offset ()	2E0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 311. Detailed Description of Raw Status for IntErr Interrupt (RAW_ERR - 0x2E0 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	RW	8'b0	Reserved (RSV)

Status for IntTfr Interrupt (STATUS_TFR - 0x2E8 + [0..0 * 0x100])

DMA Transfer Complete Interrupt status.

MEM Offset ()	2E8h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 312. Detailed Description of Status for IntTfr Interrupt (STATUS_TFR - 0x2E8 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	RO	8'b0	Status for IntTfr Interrupt (STATUS) Stores all interrupt events from channels after masking. One bit allocated per channel. Used to generate the DMAC interrupt signals.

Status for IntBlock Interrupt (STATUS_BLOCK - 0x2F0 + [0..0 * 0x100])

Block Transfer Complete Interrupt status

MEM Offset ()	2F0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

**Table 313. Detailed Description of Status for IntBlock Interrupt (STATUS_BLOCK - 0x2F0 + [0..0 * 0x100])**

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	RO	8'b0	Status for IntBlock Interrupt (STATUS) Stores all interrupt events from channels after masking. One bit allocated per channel. Used to generate the DMAC interrupt signals.

Status for IntSrcTran Interrupt (STATUS_SRC_TRAN - 0x2F8 + [0..0 * 0x100])

Source Transaction Complete Interrupt status

MEM Offset ()	2F8h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 314. Detailed Description of Status for IntSrcTran Interrupt (STATUS_SRC_TRAN - 0x2F8 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	RO	8'b0	Status for IntSrcTran Interrupt (STATUS) Stores all interrupt events from channels after masking. One bit allocated per channel. Used to generate the DMAC interrupt signals.

Status for IntDstTran Interrupt (STATUS_DST_TRAN - 0x300 + [0..0 * 0x100])

Destination Transaction Complete Interrupt status.

MEM Offset ()	300h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 315. Detailed Description of Status for IntDstTran Interrupt (STATUS_DST_TRAN - 0x300 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)



Bits	Access Type	Default	Description
7:0	RO	8'b0	Status for IntDstTran Interrupt (STATUS) Stores all interrupt events from channels after masking. One bit allocated per channel. Used to generate the DMAC interrupt signals.

Status for IntErr Interrupt (STATUS_ERR - 0x308 + [0..0 * 0x100])

Error Interrupt status.

MEM Offset ()	308h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 316. Detailed Description of Status for IntErr Interrupt (STATUS_ERR - 0x308 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	RO	8'b0	Status for IntErr Interrupt (STATUS) Stores all interrupt events from channels after masking. One bit allocated per channel. Used to generate the DMAC interrupt signals.

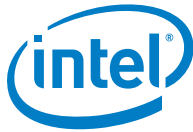
Mask for IntTfr Interrupt (MASK_TFR - 0x310 + [0..0 * 0x100])

DMA Transfer Complete Interrupt mask. The contents of the Raw Status register is masked with the contents of the Mask register.

MEM Offset ()	310h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 317. Detailed Description of Mask for IntTfr Interrupt (MASK_TFR - 0x310 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved (RSV1)
15:8	RW	8'b0	Interrupt Mask Write Enable (INT_MASK_WE) 0 = write disabled 1 = write enabled



Bits	Access Type	Default	Description
7:0	RW	8'b0	Mask for the interrupt (INT_MASK) Written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same AHB write transfer. This allows software to set a mask bit without performing a read-modified write operation. 0 = masked 1 = unmasked

Mask for IntBlock Interrupt (MASK_BLOCK - 0x318 + [0..0 * 0x100])

Block Transfer Complete Interrupt mask. The contents of the Raw Status register is masked with the contents of the Mask register.

MEM Offset ()	318h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 318. Detailed Description of Mask for IntBlock Interrupt (MASK_BLOCK - 0x318 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved (RSV1)
15:8	RW	8'b0	Interrupt Mask Write Enable (INT_MASK_WE) 0 = write disabled 1 = write enabled
7:0	RW	8'b0	Mask for the interrupt (INT_MASK) Written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same AHB write transfer. This allows software to set a mask bit without performing a read-modified write operation. 0 = masked 1 = unmasked

Mask for IntSrcTran Interrupt (MASK_SRC_TRAN - 0x320 + [0..0 * 0x100])

Source Transaction Complete Interrupt mask. The contents of the Raw Status register is masked with the contents of the Mask register.

MEM Offset ()	320h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 319. Detailed Description of Mask for IntSrcTran Interrupt (MASK_SRC_TRAN - 0x320 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved (RSV1)
15:8	RW	8'b0	Interrupt Mask Write Enable (INT_MASK_WE) 0 = write disabled 1 = write enabled
7:0	RW	8'b0	Mask for the interrupt (INT_MASK) Written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same AHB write transfer. This allows software to set a mask bit without performing a read-modified write operation. 0 = masked 1 = unmasked

Mask for IntDstTran Interrupt (MASK_DST_TRAN - 0x328 + [0..0 * 0x100])

Destination Transaction Complete Interrupt mask. The contents of the Raw Status register is masked with the contents of the Mask register.

MEM Offset ()	328h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 320. Detailed Description of Mask for IntDstTran Interrupt (MASK_DST_TRAN - 0x328 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved (RSV1)
15:8	RW	8'b0	Interrupt Mask Write Enable (INT_MASK_WE) 0 = write disabled 1 = write enabled
7:0	RW	8'b0	Mask for the interrupt (INT_MASK) Written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same AHB write transfer. This allows software to set a mask bit without performing a read-modified write operation. 0 = masked 1 = unmasked

**Mask for IntErr Interrupt (MASK_ERR - 0x330 + [0..0 * 0x100])**

Error Interrupt mask. The contents of the Raw Status register is masked with the contents of the Mask register.

MEM Offset ()	330h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 321. Detailed Description of Mask for IntErr Interrupt (MASK_ERR - 0x330 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:16	RO	16'b0	Reserved (RSV1)
15:8	RW	8'b0	Interrupt Mask Write Enable (INT_MASK_WE) 0 = write disabled 1 = write enabled
7:0	RW	8'b0	Mask for the interrupt (INT_MASK) Written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same AHB write transfer. This allows software to set a mask bit without performing a read-modified write operation. 0 = masked 1 = unmasked

Clear for IntTfr Interrupt (CLEAR_TFR - 0x338 + [0..0 * 0x100])

DMA Transfer Complete Interrupt clear.

MEM Offset ()	338h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 322. Detailed Description of Clear for IntTfr Interrupt (CLEAR_TFR - 0x338 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	WO	8'b0	Clear for Interrupt (CLEAR) 0 = no effect 1 = clear interrupt



Clear for IntBlock Interrupt (CLEAR_BLOCK - 0x340 + [0..0 * 0x100])

Block Transfer Complete Interrupt clear.

MEM Offset ()	340h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 323. Detailed Description of Clear for IntBlock Interrupt (CLEAR_BLOCK - 0x340 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	WO	8'b0	Clear for Interrupt (CLEAR) 0 = no effect 1 = clear interrupt

Clear for IntSrcTran Interrupt (CLEAR_SRC_TRAN - 0x348 + [0..0 * 0x100])

Source Transaction Complete Interrupt clear.

MEM Offset ()	348h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

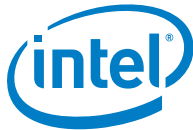
Table 324. Detailed Description of Clear for IntSrcTran Interrupt (CLEAR_SRC_TRAN - 0x348 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	WO	8'b0	Clear for Interrupt (CLEAR) 0 = no effect 1 = clear interrupt

Clear for IntDstTran Interrupt (CLEAR_DST_TRAN - 0x350 + [0..0 * 0x100])

Destination Transaction Complete Interrupt clear.

MEM Offset ()	350h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

**Table 325. Detailed Description of Clear for IntDstTran Interrupt (CLEAR_DST_TRAN - 0x350 + [0..0 * 0x100])**

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	WO	8'b0	Clear for Interrupt (CLEAR) 0 = no effect 1 = clear interrupt

Clear for IntErr Interrupt (CLEAR_ERR - 0x358 + [0..0 * 0x100])

Error Interrupt clear.

MEM Offset ()	358h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 326. Detailed Description of Clear for IntErr Interrupt (CLEAR_ERR - 0x358 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:8	RO	24'b0	Reserved (RSV)
7:0	WO	8'b0	Clear for Interrupt (STATUS) 0 = no effect 1 = clear interrupt

Combined Interrupt Status (STATUS_INT - 0x360 + [0..0 * 0x100])

The contents of each of the Status registers is ORed to produce a single bit for each interrupt type in this Combined Interrupt Status register.

MEM Offset ()	360h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 327. Detailed Description of Combined Interrupt Status (STATUS_INT - 0x360 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:5	RO	27'b0	Reserved (RSV)
4	RO	1'b0	OR of the contents of STATUS_ERR (ERR)



Bits	Access Type	Default	Description
3	RO	1'b0	OR of the contents of STATUS_DSTT (DSTT)
2	RO	1'b0	OR of the contents of STATUS_SRCT (SRCT)
1	RO	1'b0	OR of the contents of STATUS_BLOCK (BLOCK)
0	RO	1'b0	OR of the contents of STATUS_TFR (TFR)

Source Software Transaction Request (REQ_SRC_REG - 0x368 + [0..0 * 0x100])

MEM Offset ()	368h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 328. Detailed Description of Source Software Transaction Request (REQ_SRC_REG - 0x368 + [0..0 * 0x100])

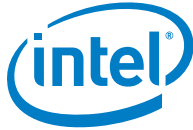
Bits	Access Type	Default	Description
31:10	RO	22'b0	Reserved (RSV1)
9:8	RW	2'b0	Source Software Transaction Request write enable (SRC_REQ_WE) 0 = write disabled 1 = write enabled
7:2	RO	6'b0	Reserved (RSV0)
1:0	RW	2'b0	Source Software Transaction Request register (SRC_REQ) This bit is written only if the corresponding channel write enable bit in the Write Enable field is asserted on the same AHB write transfer, and if the channel is enabled in the CH_EN_REG register

Destination Software Transaction Request register (REQ_DST_REG - 0x370 + [0..0 * 0x100])

MEM Offset ()	370h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 329. Detailed Description of Destination Software Transaction Request register (REQ_DST_REG - 0x370 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:10	RO	22'b0	Reserved (RSV1)



Bits	Access Type	Default	Description
9:8	RW	2'b0	Destination Software Transaction Request write enable (DST_REQ_WE) 0 = write disabled 1 = write enabled
7:2	RO	6'b0	Reserved (RSV0)
1:0	RW	2'b0	Destination Transaction Request register (DST_REQ) This bit is written only if the corresponding channel write enable bit in the Write Enable field is asserted on the same AHB write transfer, and if the channel is enabled in the CH_EN_REG register

Source Single Transaction Request (SGL_REQ_SRC_REG - 0x378 + [0..0 * 0x100])

MEM Offset ()	378h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 330. Detailed Description of Source Single Transaction Request (SGL_REQ_SRC_REG - 0x378 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:10	RO	22'b0	Reserved (RSV1)
9:8	RW	2'b0	Source Single Transaction Request write enable (SRC_SGLREQ_WE) 0 = write disabled 1 = write enabled
7:2	RO	6'b0	Reserved (RSV0)
1:0	RW	2'b0	Source Single Transaction Request register (SRC_SGLREQ) This bit is written only if the corresponding channel write enable bit in the Write Enable field is asserted on the same AHB write transfer, and if the channel is enabled in the CH_EN_REG register.

Destination Single Software Transaction Request (SGL_REQ_DST_REG - 0x380 + [0..0 * 0x100])

MEM Offset ()	380h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 331. Detailed Description of Destination Single Software Transaction Request (SGL_REQ_DST_REG - 0x380 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:10	RO	22'b0	Reserved (RSV1)
9:8	RW	2'b0	Destination Single Transaction Request write enable (DST_SGLREQ_WE) 0 = write disabled 1 = write enabled
7:2	RO	6'b0	Reserved (RSV0)
1:0	RW	2'b0	Destination Single Transaction Request register (DST_SGLREQ) This bit is written only if the corresponding channel write enable bit in the Write Enable field is asserted on the same AHB write transfer, and if the channel is enabled in the CH_EN_REG register.

Source Last Transaction Request (LST_SRC_REG - 0x388 + [0..0 * 0x100])

MEM Offset ()	388h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 332. Detailed Description of Source Last Transaction Request (LST_SRC_REG - 0x388 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:10	RO	22'b0	Reserved (RSV1)
9:8	RW	2'b0	Source Last Transaction Request write enable (LSTSRC_WE) 0 = write disabled 1 = write enabled
7:2	RO	6'b0	Reserved (RSV0)
1:0	RW	2'b0	Source Last Transaction Request register (LSTSRC) This bit is written only if the corresponding channel write enable bit in the Write Enable field is asserted on the same AHB write transfer, and if the channel is enabled in the CH_EN_REG register.

Destination Single Transaction Request (LST_DST_REG - 0x390 + [0..0 * 0x100])

MEM Offset ()	390h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

**Table 333. Detailed Description of Destination Single Transaction Request (LST_DST_REG - 0x390 + [0..0 * 0x100])**

Bits	Access Type	Default	Description
31:10	RO	22'b0	Reserved (RSV1)
9:8	RW	2'b0	Destination Last Transaction Request write enable (LSTDST_WE) 0 = write disabled 1 = write enabled
7:2	RO	6'b0	Reserved (RSV0)
1:0	RW	2'b0	Destination Last Transaction Request register (LSTDST) This bit is written only if the corresponding channel write enable bit in the Write Enable field is asserted on the same AHB write transfer, and if the channel is enabled in the CH_EN_REG register.

DMA Configuration (DMA_CFG_REG - 0x398 + [0..0 * 0x100])

Used to enable the DMA controller (DMAC), which must be done before any channel activity can begin.

If the global channel enable bit is cleared while any channel is still active, then DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DMA_EN bit returns 0.

MEM Offset ()	398h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 334. Detailed Description of DMA Configuration (DMA_CFG_REG - 0x398 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)
0	RW	1'b0	DMA global enable (DMA_EN) 0 = disabled 1 = enabled

Channel Enable (CH_EN_REG - 0x3A0 + [0..0 * 0x100])

Software can read this register in order to find out which channels are currently inactive if needs to set up a new channel. It can then enable an inactive channel with the required priority.

MEM Offset ()	3A0h
Security_PolicyGroup	

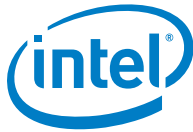


IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 335. Detailed Description of Channel Enable (CH_EN_REG - 0x3A0 + [0..0 * 0x100])

Bits	Access Type	Default	Description
31:10	RO	22'b0	Reserved (RSV1)
9:8	RW	2'b0	Channel enable register (CH_EN_WE)
7:2	RO	6'b0	Reserved (RSV0)
1:0	RW	2'b0	Channel enable register (CH_EN) Setting this bit enables a channel. Clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The CH_EN_REG.CH_EN bit is automatically cleared by hardware to disable the channel after the last AMBA transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

§



21 General Purpose I/O (GPIO)

The Intel® Quark™ SE Microcontroller C1000 contains two instances of the GPIO controller, 32 HOST GPIO's and 6 AON GPIO's. These are in addition to the 16 provided by the Sensor Subsystem.

21.1 Signal Descriptions

Please see [Chapter 2, “Physical Interfaces”](#) for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction:** The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in [Chapter 4, “Electrical Characteristics”](#)
- **Description:** A brief explanation of the signal's function

Table 336. Memory Signals

Signal Name	Direction/ Type	Description
GPIO[31:0]	I/O	General Purpose IO: 32 General Purpose IOs
GPIO[5:0] Always On	I/O	Always ON IO: 6 GPIOs capable of generating wake event in SoC Sleep. For more information, see “ Port A GPIO_AON (GPIO_SWPORTA_DR) ” in Chapter 28.2.1, “Summary of SCSS Registers—0xB0800000” .

21.2 Features

The following is a list of the GPIO controller features:

- 32 GPIOs
- Separate data register bit and data direction control bit for each GPIO
- Metastability registers for GPIO read data
- Interrupt mode supported for all GPIOs, configurable as follows:
 - Active High Level
 - Active Low Level
 - Rising Edge
 - Falling Edge
 - Both Edge



- Debounce logic for interrupt sources

21.3 Memory Mapped IO Registers

Registers listed are for GPIO, starting at base address B0000C00h.

Table 337. Summary of GPIO Registers—0xB0000C00

MEM Address	Default	Instance Name	Name
0x0	0000_0000h	GPIO_SWPORTA_DR	Port A Data
0x4	0000_0000h	GPIO_SWPORTA_DDR	Port A Data Direction
0x8	0000_0000h	GPIO_SWPORTA_CTL	Port A Data Source
0x30	0000_0000h	GPIO_INTEN	Interrupt Enable
0x34	0000_0000h	GPIO_INTMASK	Interrupt Mask
0x38	0000_0000h	GPIO_INTTYPE_LEVEL	Interrupt Type
0x3C	0000_0000h	GPIO_INT_POLARITY	Interrupt Polarity
0x40	0000_0000h	GPIO_INTSTATUS	Interrupt Status
0x44	0000_0000h	GPIO_RAW_INTSTATUS	Raw Interrupt Status
0x48	0000_0000h	GPIO_DEBOUNCE	Debounce Enable
0x4C	0000_0000h	GPIO_PORTA_EOI	Clear Interrupt
0x50	0000_0000h	GPIO_EXT_PORTA	Port A External Port
0x60	0000_0000h	GPIO_LS_SYNC	Synchronization Level
0x68	0000_0000h	GPIO_INT_BOTHEDGE	Interrupt both edge type
0x70	0003_9E73h	GPIO_CONFIG_REG2	GPIO Configuration Register 2
0x74	001F_70F6h	GPIO_CONFIG_REG1	GPIO Configuration Register 1

Port A Data (GPIO_SWPORTA_DR)

Contains the GPIO Port data bits

MEM Offset (B0000C00)	0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 338. Detailed Description of Port A Data (GPIO_SWPORTA_DR)

Bits	Access Type	Default	Description
31:0	RW	32'b0	Port Data (GPIO_SWPORTA_DR) Values written to this register are output on the I/O signals for if the corresponding data direction bits are set to Output mode and the corresponding control bit for the Port is set to Software mode. The value read back is equal to the last value written to this register.

Port A Data Direction (GPIO_SWPORTA_DDR)

Used to control the GPIO Port bits data direction

MEM Offset (B0000C00)	4h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 339. Detailed Description of Port A Data Direction (GPIO_SWPORTA_DDR)

Bits	Access Type	Default	Description
31:0	RW	32'b0	Port Data Direction (GPIO_SWPORTA_DDR) Values written to this register independently control the direction of the corresponding data bit in the Port. - 0 Input (default) - 1 Output

Port A Data Source (GPIO_SWPORTA_CTL)

Used to control the GPIO Port Data Source

MEM Offset (B0000C00)	8h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 340. Detailed Description of Port A Data Source (GPIO_SWPORTA_CTL)

Bits	Access Type	Default	Description
31:1	RO	31'h0000_0000	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
0	RW	1'b0	Port A Data Source (GPIO_SWPORTA_CTL) The data and control source for a signal can come from either software or hardware; this bit selects between them. The default source is configurable through the GPIO_DFLT_SRC_A configuration parameter. 0 Software mode (default) 1 Hardware mode

Interrupt Enable (GPIO_INTEN)

Used to configured Port A bits as interrupt sources.

MEM Offset (B0000C00)	30h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 341. Detailed Description of Interrupt Enable (GPIO_INTEN)

Bits	Access Type	Default	Description
31:0	RW	32'b0	Interrupt Enable (GPIO_INTEN) Allows each bit of Port A to be configured for interrupts. By default the generation of interrupts is disabled. Whenever a 1 is written to a bit of this register, it configures the corresponding bit on Port A to become an interrupt; otherwise, Port A operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of Port A if the corresponding data direction register is set to Output. 0 Configure Port A bit as normal GPIO signal (default) 1 Configure Port A bit as interrupt

Interrupt Mask (GPIO_INTMASK)

Controls masking for Port A bits configured as interrupt sources.

MEM Offset (B0000C00)	34h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

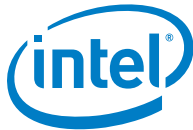


Table 342. Detailed Description of Interrupt Mask (GPIO_INTMASK)

Bits	Access Type	Default	Description
31:0	RW	32'b0	Interrupt Mask (GPIO_INTMASK) Controls whether an interrupt on Port A can create an interrupt for the interrupt controller by not masking it. By default, all interrupts bits are unmasked. Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through. The unmasked status can be read as well as the resultant status after masking. 0 Interrupt bits are unmasked (default) 1 Mask interrupt

Interrupt Type (GPIO_INTTYPE_LEVEL)

Controls the type of interrupt associated with Port A bits configured as interrupt source.

MEM Offset (B0000C00)	38h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 343. Detailed Description of Interrupt Type (GPIO_INTTYPE_LEVEL)

Bits	Access Type	Default	Description
31:0	RW	32'b0	Interrupt Type (GPIO_INTTYPE_LEVEL) Controls the type of interrupt that can occur on Port A. Whenever a 0 is written to a bit of this register, it configures the interrupt type to be level-sensitive; otherwise, it is edge-sensitive. 0 Level-sensitive (default) 1 Edge-sensitive

Interrupt Polarity (GPIO_INT_POLARITY)

Controls the interrupt polarity associated with Port A bits configured as interrupt sources.

MEM Offset (B0000C00)	3Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 344. Detailed Description of Interrupt Polarity (GPIO_INT_POLARITY)

Bits	Access Type	Default	Description
31:0	RW	32'b0	Interrupt Polarity (GPIO_INT_POLARITY) Controls the polarity of edge or level sensitivity that can occur on input of Port A. Whenever a 0 is written to a bit of this register, it configures the interrupt type to falling-edge or active-low sensitive; otherwise, it is rising-edge or active-high sensitive. 0 Active-low (default) 1 Active-high

Interrupt Status (GPIO_INTSTATUS)

Stores the interrupt status after masking for Port A bits configured as interrupt sources.

MEM Offset (B0000C00)	40h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 345. Detailed Description of Interrupt Status (GPIO_INTSTATUS)

Bits	Access Type	Default	Description
31:0	RO	32'b0	Interrupt Status (GPIO_INTSTATUS) After mask. See GPIO_RAW_INTSTATUS for raw interrupt values and GPIO_INTMASK for interrupt mask configuration.

Raw Interrupt Status (GPIO_RAW_INTSTATUS)

MEM Offset (B0000C00)	44h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

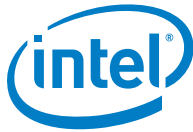
Table 346. Detailed Description of Raw Interrupt Status (GPIO_RAW_INTSTATUS)

Bits	Access Type	Default	Description
31:0	RO	32'b0	Raw Interrupt Status (GPIO_RAW_INTSTATUS) Raw interrupt of status of Port A (premasking bits).

Debounce Enable (GPIO_DEBOUNCE)

Controls the debounce logic associated to a Port A bit configured as interrupt source.

MEM Offset (B0000C00)	48h
Security_PolicyGroup	



IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 347. Detailed Description of Debounce Enable (GPIO_DEBOUNCE)

Bits	Access Type	Default	Description
31:0	RW	32'b0	Debounce Enable (GPIO_DEBOUNCE) Controls whether an external signal that is the source of an interrupt needs to be debounced to remove any spurious glitches. Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed. 0 No debounce (default) 1 Enable debounce

Clear Interrupt (GPIO_PORTA_EOI)

Controls edge-type interrupt clearing.

MEM Offset (B0000C00) 4Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 348. Detailed Description of Clear Interrupt (GPIO_PORTA_EOI)

Bits	Access Type	Default	Description
31:0	RO	32'b0	Clear Interrupt (GPIO_PORTA_EOI) Controls the clearing of edge type interrupts from Port A. When a 1 is written into a corresponding bit of this register, the interrupt is cleared. All interrupts are cleared when Port A is not configured for interrupts. 0 No interrupt clear (default) 1 Clear interrupt

Port A External Port (GPIO_EXT_PORTA)

Used by the software to read values from the GPIO Port bits.

MEM Offset (B0000C00) 50h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h



Table 349. Detailed Description of Port A External Port (GPIO_EXT_PORTA)

Bits	Access Type	Default	Description
31:0	RO	32'b0	External Port (GPIO_EXT_PORTA) When the Port is configured as Input, then reading this location reads the values on the external signal. When the data direction is set as Output, reading this location reads the Port data register contents.

Synchronization Level (GPIO_LS_SYNC)

Controls if a level-sensitive interrupt type will be synchronized to the system clock.

MEM Offset (B0000C00)	60h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 350. Detailed Description of Synchronization Level (GPIO_LS_SYNC)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)
0	RW	1'b0	Synchronization Level (GPIO_LS_SYNC) Writing a 1 to this register results in all level-sensitive interrupts being synchronized to the system clock. 0 Not Synchronized (default) 1 Synchronized

Interrupt both edge type (GPIO_INT_BOTHEDGE)

Controls the edge type of interrupt that can occur on Port A.

MEM Offset (B0000C00)	68h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 351. Detailed Description of Interrupt both edge type (GPIO_INT_BOTHEDGE)

Bits	Access Type	Default	Description
31:0	RW	32'b0	Interrupt both edge type (GPIO_PWIDTH_A) Controls the edge type of interrupt that can occur on Port A. Whenever a particular bit is programmed to 1, it enables the generation of interrupts on both the rising edge and the falling edge of an external input signal corresponding to that bit on port A. The values programmed in the registers gpio_inttype_level and gpio_int_polarity for this particular bit are not considered when the corresponding bit of this register is set to 1. Whenever a particular bit is programmed to 0, the interrupt type depends on the value of the corresponding bits in the gpio_inttype_level and gpio_int_polarity registers. 0 - Active-low (default) 1 - Active-high



22 Timers and Pulse Width Modulation (PWM)

The Timer and Pulse Width Modulation (PWM) block allows individual control of the frequency and duty cycle of four output signals. The PWM block also supports use as a Timer block for the purposes of generating periodic interrupts.

22.1 Signal Descriptions

Please see [Chapter 2, “Physical Interfaces”](#) for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction:** The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in [Chapter 4, “Electrical Characteristics”](#)
- **Description:** A brief explanation of the signal's function

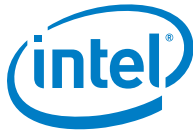
Table 352. Memory Signals

Signal Name	Direction/ Type	Description
PWM[0]	O	Output 0: <i>PWM Output 0</i>
PWM[1]	O	Output 1: <i>PWM Output 1</i>
PWM[2]	O	Output 2: <i>PWM Output 2</i>
PWM[3]	O	Output 3: <i>PWM Output 3</i>

22.2 Features

The following is a list of the PWM features:

- Four counters capable of operating in PWM mode or Timer mode
- PWM mode
 - Configurable High and Low times for each PWM Output
 - Minimum High and Low time of 2 32MHz clock periods (8MHz)
 - Maximum High and Low time of 2^{32} 32MHz clock periods (< 1Hz)
 - High and Low time granularity of a single 32MHz clock period
 - Interrupt generation always on both the rising and falling edges of the PWM Output
 - Interrupt Control per PWM Output:



- Interrupt Generation only on both edges of the PWM Output
 - Interrupt Mask Capability
- Timer mode
 - 32-bit Timer operating at 32MHz
 - Timer Periods from 1 32MHz clock period (31.25ns) to $2^{32}-1$ 32MHz clock periods (134s)
 - Interrupt Control per Timer:
 - Interrupt Generation on Timer Expiry
 - Interrupt Mask Capability

22.2.1 PMW Signaling

The Timer and PWM block supports the generation of PWM Output signals with configurable low and high times, which allows both the duty cycle and frequency to be set. The following figures show some example PWM Output signals.

Figure 31. Duty Cycle of 20%

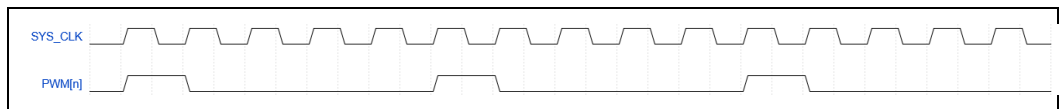


Figure 32. Duty Cycle of 50%

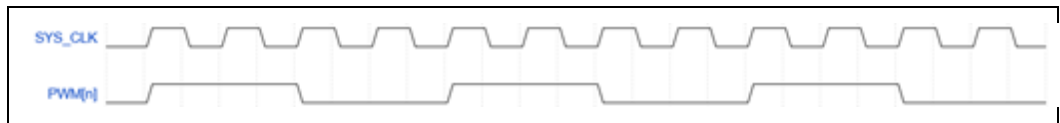


Figure 33. Duty Cycle of 80%



See [Chapter 22.3.1, “PWM Mode”](#) for details on configuring the low and high times.

22.2.2 Functional Operation

Each counter is identical, has an associated PWM Output, and can be individually configured with the following options:

- Enable
- PWM Mode or Timer Mode
- PWM Duty Cycle and Frequency
- Timer Timeout Period
- Interrupt Masking



In PWM mode, the high and low times can be configured as follows. This assumes a nominal system clock frequency of 32MHz. The values, in nanoseconds, will differ if the system clock frequency is changed.

Table 353. PWM Timing

Characteristic	Value (System Clock Cycles)	Value (time)
Low Time Granularity	1	31.25ns
Low Time Range	2 to 4294967296 (2^{32})	62.5ns to 134.22s
High Time Granularity	1	31.25ns
High Time Range	2 to 4294967296 (2^{32})	62.5ns to 134.22s

See [Chapter 22.3.1, "PWM Mode"](#) for details on configuring the low and high times.

PWM mode supports the following maskable interrupt source:

- Both edges of the PWM Output signal

In Timer mode, the timeout period can be configured as follows. This assumes a nominal system clock frequency of 32MHz. The values, in nanoseconds, will differ if the system clock frequency is changed.

Table 354. Timer Period

Characteristic	Value (System Clock Cycles)	Value (time)
Timeout Period Granularity	1	31.25ns
Timeout Period Range	0 to 4294967295 ($2^{32} - 1$)	0 to 134.22s

See [Chapter 22.3.2, "Timer Mode"](#) for details on configuring the timeout period.

Timer Mode supports the following maskable interrupt source:

- Timer Expiry

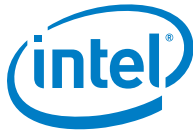
Interrupts are cleared by reading the Timer N End Of Interrupt register.

22.3 Use

22.3.1 PWM Mode

Once enabled, the counter runs in free running mode and the associated PWM Output is set to 0.

The Low Time is determined by the Timer N Load Count register value which is loaded into counter upon enable, once the counter decrements to 0 the associated PWM.



Output toggles from 0 to 1 and the counter is loaded with the Timer N Load Count 2 register value which determines the High time.

When the counter subsequently decrements to 0 the associated PWM Output toggles from 1 to 0 and the timer is re-loaded with the Timer N Load Count register value and the process repeats.

22.3.2 Timer Mode

Once enabled, the counter also runs in free running mode.

In the case of Timer mode there are two modes of timer operation as defined below:

- Free Running where the Timer N Load Count register value is used for the initial timeout value and also the reload value for subsequent timeout events. This enables periodic timer operation.
- Free Running where the Timer N Load Count register value is used for the initial timeout value however the subsequent reload value after the initial timeout event is set to $2^{32}-1$. This allows sufficient time for firmware to disable the timer after the initial timeout, thus enabling one shot timer operation.

In Timer mode the PWM Outputs are unused and associated pins can be freed up for alternative functions by reconfiguring the pin muxing.

22.4 Memory Mapped IO Registers

Registers listed are for PWM, starting at base address B0000800h.

Table 355. Summary of PWM Registers—0xB0000800

MEM Address	Default	Instance Name	Name
0x0	0000_0000h	Timer1LoadCount	Timer 1 Load Count
0x4	0000_0000h	Timer1CurrentValue	Timer 1 Current Value
0x8	0000_0000h	Timer1ControlReg	Timer 1 Control
0xC	0000_0000h	Timer1EOI	Timer 1 End Of Interrupt
0x10	0000_0000h	Timer1IntStatus	Timer 1 Interrupt Status
0x14	0000_0000h	Timer2LoadCount	Timer 2 Load Count
0x18	0000_0000h	Timer2CurrentValue	Timer 2 Current Value
0x1C	0000_0000h	Timer2ControlReg	Timer 2 Control
0x20	0000_0000h	Timer2EOI	Timer 2 End Of Interrupt
0x24	0000_0000h	Timer2IntStatus	Timer 2 Interrupt Status
0x28	0000_0000h	Timer3LoadCount	Timer 3 Load Count
0x2C	0000_0000h	Timer3CurrentValue	Timer 3 Current Value



MEM Address	Default	Instance Name	Name
0x30	0000_0000h	Timer3ControlReg	Timer 3 Control
0x34	0000_0000h	Timer3EOI	Timer 3 End Of Interrupt
0x38	0000_0000h	Timer3IntStatus	Timer 3 Interrupt Status
0x3C	0000_0000h	Timer4LoadCount	Timer 4 Load Count
0x40	0000_0000h	Timer4CurrentValue	Timer 4 Current Value
0x44	0000_0000h	Timer4ControlReg	Timer 4 Control
0x48	0000_0000h	Timer4EOI	Timer 4 End Of Interrupt
0x4C	0000_0000h	Timer4IntStatus	Timer 4 Interrupt Status
0xA0	0000_0000h	TimersIntStatus	Timers Interrupt Status
0xA4	0000_0000h	TimersEOI	Timers End Of Interrupt
0xA8	0000_0000h	TimersRawIntStatus	Timers Raw (unmasked) Interrupt Status
0xAC	3230_392Ah	TimersCompVersion	Timers Component Version
0xB0	0000_0000h	Timer1LoadCount2	Timer 1 Load Count 2
0xB4	0000_0000h	Timer2LoadCount2	Timer 2 Load Count 2
0xB8	0000_0000h	Timer3LoadCount2	Timer 3 Load Count 2
0xBC	0000_0000h	Timer4LoadCount2	Timer 4 Load Count 2

Timer 1 Load Count (Timer1LoadCount)

MEM Offset (B0000800)	0B0000800h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 356. Detailed Description of Timer 1 Load Count (Timer1LoadCount)

Bits	Access Type	Default	Description
31:0	RW	32'h0	Timer Load Count (TimerLoadCount) In PWM mode, this register field controls the low period of the corresponding PWM output signal. In Timer mode, this is the value that the timer counter starts counting down from, and controls the high and low periods the PWM output signal.

Timer 1 Current Value (Timer1CurrentValue)

MEM Offset (B0000800)	0B0000804h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

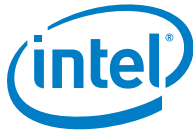


Table 357. Detailed Description of Timer 1 Current Value (Timer1CurrentValue)

Bits	Access Type	Default	Description
31:0	RO	32'h0	Timer Current Value (TimerCurrentValue) In both PWM and Timer mode, reading this register field returns the current value of the counter controlling the PWM/Timer. If reading from this register outside of an interrupt service routine, software should first perform 2 dummy writes to another PWM/Timer register.

Timer 1 Control (Timer1ControlReg)

MEM Offset (B0000800)	0B0000808h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 358. Detailed Description of Timer 1 Control (Timer1ControlReg)

Bits	Access Type	Default	Description
31:4	RO	28'h0	Reserved (RSVD1) Reserved
3	RW	1'h0	Timer PWM (TIMER_PWM) Select between PWM mode and Timer mode. 1 - PWM Mode 0 - Timer Mode
2	RW	1'h0	Timer Interrupt Mask (TIMER_INTERRUPT_MASK) Set to b1 to mask the interrupt from PWM/Timer
1	RW	1'h0	Timer Mode (TIMER_MODE) Select between free running and user defined count mode. 1 - user-defined count mode 0 - free-running mode NOTE: Must be operated in user-defined count mode (that is, this field must be set to b1).
0	RW	1'h0	Timer Enable (TIMER_ENABLE) 0 - Disable PWM/Timer 1 - Enable PWM/Timer

Timer 1 End Of Interrupt (Timer1EOI)

MEM Offset (B0000800)	0B000080Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits



Default

0000_0000h

Table 359. Detailed Description of Timer 1 End Of Interrupt (Timer1EOI)

Bits	Access Type	Default	Description
31:1	RO	31'h0	Reserved (RSVD1) Reserved
0	RO	1'h0	Timer End-of-Interrupt (TIMER_END_OF_INTERRUPT) Reading from this register returns b0, and clears the interrupt form PWM/Timer.

Timer 1 Interrupt Status (Timer1IntStatus)

MEM Offset (B0000800)

0B0000810h

Security_PolicyGroup

IntelRsvd

False

Size

32 bits

Default

0000_0000h

Table 360. Detailed Description of Timer 1 Interrupt Status (Timer1IntStatus)

Bits	Access Type	Default	Description
31:1	RO	31'h0	Reserved (RSVD1) Reserved
0	RO	1'h0	Timer Interrupt Status (TIMER_INTERRUPT_STATUS) A read of this register returns the post masking interrupt status of PWM/Timer. If reading from this register outside of an interrupt service routine, software should first perform 2 dummy writes to another PWM/Timer register.

Timer 2 Load Count (Timer2LoadCount)

MEM Offset (B0000800)

0B0000814h

Security_PolicyGroup

IntelRsvd

False

Size

32 bits

Default

0000_0000h



Table 361. Detailed Description of Timer 2 Load Count (Timer2LoadCount)

Bits	Access Type	Default	Description
31:0	RW	32'h0	Timer Load Count (TimerLoadCount) In PWM mode, this register field controls the low period of the corresponding PWM output signal. In Timer mode, this is the value that the timer counter starts counting down from, and controls the high and low periods the PWM output signal.

Timer 2 Current Value (Timer2CurrentValue)

MEM Offset (B0000800)	0B0000818h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 362. Detailed Description of Timer 2 Current Value (Timer2CurrentValue)

Bits	Access Type	Default	Description
31:0	RO	32'h0	Timer Current Value (TimerCurrentValue) In both PWM and Timer mode, reading this register field returns the current value of the counter controlling the PWM/Timer. If reading from this register outside of an interrupt service routine, software should first perform 2 dummy writes to another PWM/Timer register.

Timer 2 Control (Timer2ControlReg)

MEM Offset (B0000800)	0B000081Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 363. Detailed Description of Timer 2 Control (Timer2ControlReg)

Bits	Access Type	Default	Description
31:4	RO	28'h0	Reserved (RSVD1) Reserved
3	RW	1'h0	Timer PWM (TIMER_PWM) Select between PWM mode and Timer mode. 1 - PWM Mode 0 - Timer Mode



Bits	Access Type	Default	Description
2	RW	1'h0	Timer Interrupt Mask (TIMER_INTERRUPT_MASK) Set to b1 to mask the interrupt from PWM/Timer
1	RW	1'h0	Timer Mode (TIMER_MODE) Select between free running and user defined count mode. 1 - user-defined count mode 0 - free-running mode NOTE: Must be operated in user-defined count mode (that is, this field must be set to b1).
0	RW	1'h0	Timer Enable (TIMER_ENABLE) 0 - Disable PWM/Timer 1 - Enable PWM/Timer

Timer 2 End Of Interrupt (Timer2EOI)

MEM Offset (B0000800)	0B0000820h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 364. Detailed Description of Timer 2 End Of Interrupt (Timer2EOI)

Bits	Access Type	Default	Description
31:1	RO	31'h0	Reserved (RSVD1) Reserved
0	RO	1'h0	Timer End-of-Interrupt (TIMER_END_OF_INTERRUPT) Reading from this register returns b0, and clears the interrupt form PWM/Timer.

Timer 2 Interrupt Status (Timer2IntStatus)

MEM Offset (B0000800)	0B0000824h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 365. Detailed Description of Timer 2 Interrupt Status (Timer2IntStatus)

Bits	Access Type	Default	Description
31:1	RO	31'h0	Reserved (RSVD1) Reserved



Bits	Access Type	Default	Description
0	RO	1'h0	Timer Interrupt Status (TIMER_INTERRUPT_STATUS) A read of this register returns the post masking interrupt status of PWM/Timer. If reading from this register outside of an interrupt service routine, software should first perform 2 dummy writes to another PWM/Timer register.

Timer 3 Load Count (Timer3LoadCount)

MEM Offset (B0000800)	0B0000828h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 366. Detailed Description of Timer 3 Load Count (Timer3LoadCount)

Bits	Access Type	Default	Description
31:0	RW	32'h0	Timer Load Count (TimerLoadCount) In PWM mode, this register field controls the low period of the corresponding PWM output signal. In Timer mode, this is the value that the timer counter starts counting down from, and controls the high and low periods the PWM output signal.

Timer 3 Current Value (Timer3CurrentValue)

MEM Offset (B0000800)	0B000082Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 367. Detailed Description of Timer 3 Current Value (Timer3CurrentValue)

Bits	Access Type	Default	Description
31:0	RO	32'h0	Timer Current Value (TimerCurrentValue) In both PWM and Timer mode, reading this register field returns the current value of the counter controlling the PWM/Timer. If reading from this register outside of an interrupt service routine, software should first perform 2 dummy writes to another PWM/Timer register.

Timer 3 Control (Timer3ControlReg)

MEM Offset (B0000800)	0B0000830h



Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 368. Detailed Description of Timer 3 Control (Timer3ControlReg)

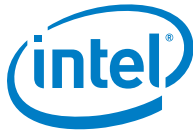
Bits	Access Type	Default	Description
31:4	RO	28'h0	Reserved (RSVD1) Reserved
3	RW	1'h0	Timer PWM (TIMER_PWM) Select between PWM mode and Timer mode. 1 - PWM Mode 0 - Timer Mode
2	RW	1'h0	Timer Interrupt Mask (TIMER_INTERRUPT_MASK) Set to b1 to mask the interrupt from PWM/Timer
1	RW	1'h0	Timer Mode (TIMER_MODE) Select between free running and user defined count mode. 1 - user-defined count mode 0 - free-running mode NOTE: Must be operated in user-defined count mode (that is, this field must be set to b1).
0	RW	1'h0	Timer Enable (TIMER_ENABLE) 0 - Disable PWM/Timer 1 - Enable PWM/Timer

Timer 3 End Of Interrupt (Timer3EOI)

MEM Offset (B0000800) 0B0000834h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 369. Detailed Description of Timer 3 Control (Timer3ControlReg)

Bits	Access Type	Default	Description
31:1	RO	31'h0	Reserved (RSVD1) Reserved
0	RO	1'h0	Timer End-of-Interrupt (TIMER_END_OF_INTERRUPT) Reading from this register returns b0, and clears the interrupt form PWM/Timer.

**Timer 3 Interrupt Status (Timer3IntStatus)**

MEM Offset (B0000800) 0B0000838h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 370. Detailed Description of Timer 3 Interrupt Status (Timer3IntStatus)

Bits	Access Type	Default	Description
31:1	RO	31'h0	Reserved (RSVD1) Reserved
0	RO	1'h0	Timer Interrupt Status (TIMER_INTERRUPT_STATUS) A read of this register returns the post masking interrupt status of PWM/Timer. If reading from this register outside of an interrupt service routine, software should first perform 2 dummy writes to another PWM/Timer register.

Timer 4 Load Count (Timer4LoadCount)

MEM Offset (B0000800) 0B000083Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 371. Detailed Description of Timer 4 Load Count (Timer4LoadCount)

Bits	Access Type	Default	Description
31:0	RW	32'h0	Timer Load Count (TimerLoadCount) In PWM mode, this register field controls the low period of the corresponding PWM output signal. In Timer mode, this is the value that the timer counter starts counting down from, and controls the high and low periods the PWM output signal.

Timer 4 Current Value (Timer4CurrentValue)

MEM Offset (B0000800) 0B0000840h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h



Table 372. Detailed Description of Timer 4 Current Value (Timer4CurrentValue)

Bits	Access Type	Default	Description
31:0	RO	32'h0	Timer Current Value (TimerCurrentValue) In both PWM and Timer mode, reading this register field returns the current value of the counter controlling the PWM/Timer. If reading from this register outside of an interrupt service routine, software should first perform two dummy writes to another PWM/Timer register.

Timer 4 Control (Timer4ControlReg)

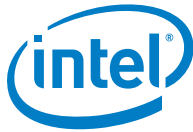
MEM Offset (B0000800)	0B0000844h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 373. Detailed Description of Timer 4 Control (Timer4ControlReg)

Bits	Access Type	Default	Description
31:4	RO	28'h0	Reserved (RSVD1) Reserved
3	RW	1'h0	Timer PWM (TIMER_PWM) Select between PWM mode and Timer mode. 1 - PWM Mode 0 - Timer Mode
2	RW	1'h0	Timer Interrupt Mask (TIMER_INTERRUPT_MASK) Set to b1 to mask the interrupt from PWM/Timer
1	RW	1'h0	Timer Mode (TIMER_MODE) Select between free running and user defined count mode. 1 - user-defined count mode 0 - free-running mode NOTE: Must be operated in user-defined count mode (that is, this field must be set to b1).
0	RW	1'h0	Timer Enable (TIMER_ENABLE) 0 - Disable PWM/Timer 1 - Enable PWM/Timer

Timer 4 End Of Interrupt (Timer4EOI)

MEM Offset (B0000800)	0B0000848h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits



Default

0000_0000h

Table 374. Detailed Description of Timer 4 End Of Interrupt (Timer4EOI)

Bits	Access Type	Default	Description
31:1	RO	31'h0	Reserved (RSVD1) Reserved
0	RO	1'h0	Timer End-of-Interrupt (TIMER_END_OF_INTERRUPT) Reading from this register returns b0, and clears the interrupt form PWM/Timer.

Timer 4 Interrupt Status (Timer4IntStatus)

MEM Offset (B0000800) 0B000084Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 375. Detailed Description of Timer 4 Interrupt Status (Timer4IntStatus)

Bits	Access Type	Default	Description
31:1	RO	31'h0	Reserved (RSVD1) Reserved
0	RO	1'h0	Timer Interrupt Status (TIMER_INTERRUPT_STATUS) A read of this register returns the post masking interrupt status of PWM/Timer. If reading from this register outside of an interrupt service routine, software should first perform 2 dummy writes to another PWM/Timer register.

Timers Interrupt Status (TimersIntStatus)

MEM Offset (B0000800) 0B00008A0h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 376. Detailed Description of Timers Interrupt Status (TimersIntStatus)

Bits	Access Type	Default	Description
31:4	RO	28'h0	Reserved (RSVD1) Reserved



Bits	Access Type	Default	Description
3:0	RO	4'h0	Timers Interrupt Status (TIMERS_INTERRUPT_STATUS) A read of this register returns the post masking interrupt status of all PWM/Timers. Bit position corresponds to PWM/Timer number. If reading from this register outside of an interrupt service routine, software should first perform 2 dummy writes to another PWM/Timer register.

Timers End Of Interrupt (TimersEOI)

MEM Offset (B0000800)	0B00008A4h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 377. Detailed Description of Timers End Of Interrupt (TimersEOI)

Bits	Access Type	Default	Description
31:4	RO	28'h0	Reserved (RSVD1) Reserved
3:0	RO	4'h0	Timers End-of-Interrupt Status (TIMERS_END_OF_INTERRUPT) A read of this register returns all '0's, and clears all active interrupts from all PWM/Timers.

Timers Raw (unmasked) Interrupt Status (TimersRawIntStatus)

MEM Offset (B0000800)	0B00008A8h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 378. Detailed Description of Timers Raw (unmasked) Interrupt Status (TimersRawIntStatus)

Bits	Access Type	Default	Description
31:4	RO	28'h0	Reserved (RSVD1) Reserved



Bits	Access Type	Default	Description
3:0	RO	4'h0	Timers Raw Interrupt Status (TIMERS_RAW_INTERRUPT_STATUS) A read of this register returns the pre masking interrupt status of all PWM/Timers. Bit position corresponds to PWM/Timer number. If reading from this register outside of an interrupt service routine, software should first perform 2 dummy writes to another PWM/Timer register.

Timers Component Version (TimersCompVersion)

MEM Offset (B0000800)	0B00008ACh
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	3230_392Ah

Table 379. Detailed Description of Timers Component Version (TimersCompVersion)

Bits	Access Type	Default	Description
31:0	RO	32'h3230392a	Timers Component Version (TIMERS_COMPONENT_VERSION) A read of this register returns an ASCII string representing the version number of the DW_apb_timers IP.

Timer 1 Load Count 2 (Timer1LoadCount2)

MEM Offset (B0000800)	0B00008B0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 380. Detailed Description of Timer 1 Load Count 2 (Timer1LoadCount2)

Bits	Access Type	Default	Description
31:0	RW	32'h0	Timer Load Count 2 (TimerLoadCount2) In PWM mode, this register field controls the high period of the corresponding PWM output signal. In Timer mode, this register has no functional use.

Timer 2 Load Count 2 (Timer2LoadCount2)

MEM Offset (B0000800)	0B00008B4h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits



Default

0000_0000h

Table 381. Detailed Description of Timer 2 Load Count 2 (Timer2LoadCount2)

Bits	Access Type	Default	Description
31:0	RW	32'h0	Timer Load Count 2 (TimerLoadCount2) In PWM mode, this register field controls the high period of the corresponding PWM output signal. In Timer mode, this register has no functional use.

Timer 3 Load Count 2 (Timer3LoadCount2)

MEM Offset (B0000800)

0B00008B8h

Security_PolicyGroup

IntelRsvd

False

Size

32 bits

Default

0000_0000h

Table 382. Detailed Description of Timer 3 Load Count 2 (Timer3LoadCount2)

Bits	Access Type	Default	Description
31:0	RW	32'h0	Timer Load Count 2 (TimerLoadCount2) In PWM mode, this register field controls the high period of the corresponding PWM output signal. In Timer mode, this register has no functional use.

Timer 4 Load Count 2 (Timer4LoadCount2)

MEM Offset (B0000800)

0B00008BCh

Security_PolicyGroup

IntelRsvd

False

Size

32 bits

Default

0000_0000h

Table 383. Detailed Description of Timer 4 Load Count 2 (Timer4LoadCount2)

Bits	Access Type	Default	Description
31:0	RW	32'h0	Timer Load Count 2 (TimerLoadCount2) In PWM mode, this register field controls the high period of the corresponding PWM output signal. In Timer mode, this register has no functional use.



23 Watchdog Timer

The Watchdog Timer can be used to trigger a Warm Reset in the event that the Intel® Quark™ SE Microcontroller C1000 becomes unresponsive. Note the Watchdog Timer will pause automatically when the Intel® Quark™ SE Microcontroller enters in C2 power mode or while debugging.

23.1 Features

The following is a list of the Watchdog (WDT) features:

- Timer can be disabled (default state) or locked enabled
- Selectable Timeout Value that ranges from ~2ms to ~60s (at 32MHz)
- Capability to have a different Initial Timeout Value versus the Reload Timeout Value
- 2 Timeout Response Modes

23.1.1 WDT Enable

The WDT_CR.WDT_EN register field must be set to 1 to enable the WDT. Once set to 1, the WDT_EN field can only be set back to 0 by an Intel® Quark™ SE Microcontroller C1000 reset.

23.1.2 WDT Timeout Capabilities

The timer uses a 32-bit down-counter which is loaded with the programmed Timeout Value.

The Initial Timeout Value is selected by the WDT_TORR.TOP_INIT register field, this value gets loaded into the timer when the WDT is first enabled. The Reload Timeout Value is selected by the WDT_TORR.TOP register field, this value gets loaded into the timer on subsequent reloads of the timer.

The values below are based off a 32 MHz System Clock and must be adjusted if the frequency is adjusted (see [Clocking Section](#)).

Table 384. WDT Timeout Selection

TOP_INIT / TOP	Clock Cycles	Value (at 32MHz)
N = 0 to 15	2^{16+N}	$(2^{16-N} / 32\text{MHz})\text{s}$ (2.048ms for N=0)



23.2 Use

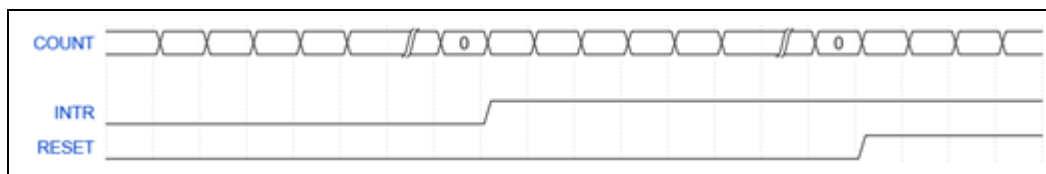
When enabled the timer starts counting down from the programmed Timeout Value. If the processor fails to reload the counter before it reaches zero (timeout), the WDT does one of two things, depending on the programmed Response Mode.

Table 385. WDT Response Mode

Response Mode	Behaviour
0	The WDT will request a microcontroller Warm Reset on a timeout.
1	The WDT will generate an Interrupt on first timeout. If Interrupt has not been cleared by the second timeout the WDT will then request a microcontroller Warm Reset. NOTE: See the following figure.

Note: When the counter reaches zero it wraps to the programmed Timeout Value and continue decrementing.

Figure 34. WDT Behaviour for Response Mode of 1



The counter is reloaded by writing 76h to the Counter Restart Register. This will also clear the WDT Interrupt.

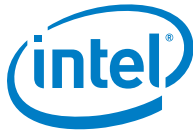
The WDT Interrupt may also be cleared by reading the Interrupt Clear Register, however, this will not reload the counter.

23.3 Memory Mapped IO Registers

Registers listed are for the WDT, starting at base address B0000000h.

Table 386. Summary of WDT Registers—0xB0000000

MEM Address	Default	Instance Name	Name
0x0	0000_0002h	WDT_CR	Control Register
0x4	0000_0000h	WDT_TORR	Timeout Range Register
0x8	0000_FFFFh	WDT_CCVR	Current Counter Value Register
0xC	0000_0000h	WDT_CRR	Current Restart Register
0x10	0000_0000h	WDT_STAT	Interrupt Status Register



MEM Address	Default	Instance Name	Name
0x14	0000_0000h	WDT_EOI	Interrupt Clear Register
0xE4	0000_0000h	WDT_COMP_PARAM_5	Component Parameters
0xE8	0000_0000h	WDT_COMP_PARAM_4	Component Parameters
0xEC	0000_0000h	WDT_COMP_PARAM_3	Component Parameters
0xF0	0000_FFFFh	WDT_COMP_PARAM_2	Component Parameters
0xF4	1000_0242h	WDT_COMP_PARAM_1	Component Parameters Register 1
0xF8	3130_372Ah	WDT_COMP_VERSION	Component Version Register
0xFC	4457_0120h	WDT_COMP_TYPE	Component Type Register

Control Register (WDT_CR)

MEM Offset (B00000000)	0B0000000h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0002h

Table 387. Detailed Description of Control Register (WDT_CR)

Bits	Access Type	Default	Description
31:6	RO	26'h0	Reserved (RSVD1) Reserved
5	RW	1'h0	Scratch Pad (NO_NAME) Scratch Pad R/W Register Bit, this bit has no functional effect.
4:2	RW	3'h0	Reset Pulse Width (RST_PULSE_WIDTH) 000 - 2 system clock cycles 001 - 4 system clock cycles 010 - 8 system clock cycles 011 - 16 system clock cycles 100 - 32 system clock cycles 101 - 64 system clock cycles 110 - 128 system clock cycles 111 - 256 system clock cycles
1	RW	1'h1	Response Mode (RMOD) 0 = Trigger a microcontroller Reset 1 = First generate Interrupt and if not cleared trigger a microcontroller Reset
0	RW	1'h0	WDT Enable (WDT_ENABLE) 0 = Watchdog Timer Disable 1 = Watchdog Timer Enable



Timeout Range Register (WDT_TORR)

MEM Offset (B0000000) 0B0000004h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 388. Detailed Description of Timeout Range Register (WDT_TORR)

Bits	Access Type	Default	Description
31:8	RO	24'h0	Reserved (RSVD1) Reserved
7:4	RW	4'h0	Timeout Period for Initialization (TOP_INIT) Used to select the timeout period that the Watchdog Timer starts from when enabled, subsequent restarts (kicks) use the period in the TOP field. This register should be written after reset and before the Watchdog Timer is enabled.
3:0	RW	4'h0	Timeout Period (TOP) This field is used to select the timeout period from which the Watchdog Timer restarts. A change of the timeout period takes effect only after the next restart (kick).

Current Counter Value Register (WDT_CCVR)

MEM Offset (B0000000) 0B00000008h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_FFFFh

Table 389. Detailed Description of Current Counter Value Register (WDT_CCVR)

Bits	Access Type	Default	Description
31:0	RO	32'hFFFF	Current Counter Value Register (WDT_CCVR) This register when read is the current value of the internal counter.

Current Restart Register (WDT_CRR)

MEM Offset (B0000000) 0B0000000Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h



Table 390. Detailed Description of Current Restart Register (WDT_CRR)

Bits	Access Type	Default	Description
31:0	WO	32'h0	Current Restart Register (WDT_CRR) This register is used to restart (kick) the Watchdog Timer. As a safety feature to prevent accidental restarts, the value 0x76 must be written. A restart also clears the Watchdog Timer interrupt. Reading this register returns zero.

Interrupt Status Register (WDT_STAT)

MEM Offset (B0000000)	0B0000010h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 391. Detailed Description of Interrupt Status Register (WDT_STAT)

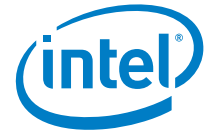
Bits	Access Type	Default	Description
31:1	RO	31'h0	Reserved (RSVD1) Reserved
0	RO	1'h0	Interrupt Status Register (WDT_STAT) This register shows the interrupt status of the Watchdog Timer: 0 = interrupt is active 1 = interrupt is inactive

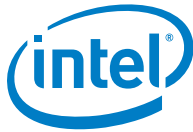
Interrupt Clear Register (WDT_EOI)

MEM Offset (B0000000)	0B0000014h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 392. Detailed Description of Interrupt Clear Register (WDT_EOI)

Bits	Access Type	Default	Description
31:1	RO	31'h0	Reserved (RSVD1) Reserved
0	RO	1'h0	Interrupt Clear Register (WDT_EOI) Reading this register clears the Watchdog Timer interrupt. This can be used to clear the interrupt without restarting the Watchdog Timer





24 Real Time Clock

The Intel® Quark™ SE Microcontroller C1000 contains a Real Time Clock for the purpose of keeping track of time. The RTC operates from 1 Hz to 32.768 kHz.

The RTC supports alarm functionality that allows scheduling an Interrupt / Wake Event for a future time.

The RTC operates in all Intel® Quark™ SE microcontroller Power States. The RTC is powered from the same battery supply as the rest of the Intel® Quark™ SE Microcontroller C1000 and does not have its own dedicated supply.

24.1 Signal Descriptions

Please see [Chapter 2, “Physical Interfaces”](#) for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction:** The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in [Chapter 4, “Electrical Characteristics”](#)
- **Description:** A brief explanation of the signal's function

Table 393. Memory Signals

Signal Name	Direction/ Type	Description
OSC32_IN	I Analog	Crystal Input: This signal is connected to the 32.768 kHz Crystal.
OSC32_OUT	O Analog	Crystal Output: This signal is connected to the 32.768 kHz Crystal.

24.1.1 Features

The following is a list of the RTC features:

- Programmable 32 bit binary Counter
- Counter increments on successive edges of a Counter Clock from 1 Hz to 32.768 kHz (derived from the 32.768 kHz Crystal Oscillator clock)
- Comparator for Interrupt / Wake Event generation based on the programmed Match Value
- Supports Interrupt / Wake Event generation when only the Counter Clock is running (Fabric Clock is off)



24.1.2 RTC Clock

The RTC clock is the output of a 4-bit prescaler (see [Chapter 7, "Clocking"](#)) that is driven by the output of the 32.768 kHz Crystal Oscillator.

This allows a range of clock frequencies to be generated as shown in the table below:

Table 394. RTC Clock Scaling

Output Clock Frequency	32.768 kHz	16.384 kHz	8.192 kHz	4.096 kHz	2.048 kHz	1.024 kHz	512 Hz	256 Hz	128 Hz	64 Hz	32 Hz	16 Hz	8 Hz	4 Hz	2 Hz	1 Hz
Scaling Factor	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

24.1.3 Counter Functionality

The RTC contains a single 32bit up-counter. The counter starts to increment when the RTC is taken out of reset. The counter increments on successive edges of the RTC clock.

The counter Start Value is loaded by writing a 32bit value to the Counter Load Register. The Counter supports loading a Start Value while it is incrementing.

When the counter reaches its max value ($2^{32}-1$) it wraps to 0 and continues incrementing.

The RTC supports reading the Counter via the read-only Counter Value Register.

24.2 Use

24.2.1 Clock and Calendar

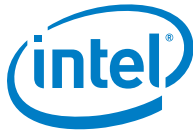
The 32bit counter is intended to provide Clock and Calendar functionality. The capabilities differ depending on the chosen frequency of the RTC clock as described in the examples below.

Using a 1 Hz RTC clock the following capabilities are exposed:

- Counter increments every second
- Counter wraps in $2^{32}-1$ seconds (~136 years)
- Counter can be used to store Time and Date in the Unix Time format defined as the number of seconds since 00:00:00 UTC on 1 January 1970 (the epoch)

Using a 32.68 kHz RTC clock the following capabilities are exposed:

- Counter increments every 30.5 microsecond (~1.51 days)



- Counter wraps in $2^{32}-1 * 30.5$ microsecond (~136 years)

24.2.2 Alarm

Alarm functionality is provided by the Match Value Register. The interrupt generation logic asserts the interrupt (if enabled) when the counter reaches this Match Value.

The RTC allows the user to disable interrupt generation and also to mask a generated interrupt.

Additionally the RTC supports generation of an interrupt when only the RTC clock is running, this allows the interrupt to be generated when in the Deep Sleep state.

24.2.3 Wake Event

The RTC supports waking the Intel® Quark™ SE Microcontroller C1000 from Low Power States, including Deep Sleep. Note that only Level interrupt are supported. Edge interrupt are not supported. The Intel® Quark™ SE Microcontroller C1000 use the RTC interrupt as the source of this wake event, so interrupt generation must be enabled to facilitate this RTC wake capability.

24.3 Memory Mapped IO Registers

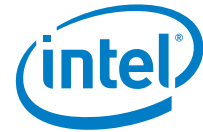
Registers listed are for RTC, starting at base address B000400h.

Table 395. Summary of RTC Registers—0xB0000400

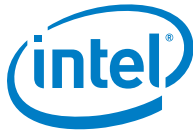
MEM Address	Default	Instance Name	Name
0x0	0000_0000h	RTC_CCVR	Current Counter Value Register
0x4	0000_0000h	RTC_CMR	Counter Match Register
0x8	0000_0000h	RTC_CLR	Counter Load Register
0xC	0000_0000h	RTC_CCR	Counter Control Register
0x10	0000_0000h	RTC_STAT	Interrupt Status Register
0x14	0000_0000h	RTC_RSTAT	Interrupt Raw Status Register
0x18	0000_0000h	RTC_EOI	End of Interrupt Register
0x1C	3230_332Ah	RTC_COMP_VERSION	Component Version Register

Current Counter Value Register (RTC_CCVR)

MEM Offset (B0000400)	0B0000400h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

**Table 396. Detailed Description of Current Counter Value Register (RTC_CCVR)**

Bits	Access Type	Default	Description
31:0	RO	32'h0	Current Counter Value (RTC_CCVR) When read, this register returns the current value of the internal counter

**Counter Match Register (RTC_CMCR)**

MEM Offset (B0000400)	0B0000404h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 397. Detailed Description of Counter Match Register (RTC_CMCR)

Bits	Access Type	Default	Description
31:0	RW	32'h0	Counter Match (RTC_CMCR) When the internal counter matches the value written to this register an interrupt is generated, provided interrupt generation is enabled

Counter Load Register (RTC_CLR)

MEM Offset (B0000400)	0B0000408h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 398. Counter Load Register (RTC_CLR)

Bits	Access Type	Default	Description
31:0	RW	32'h0	Counter Load (RTC_CLR) The value written into this register is loaded into the counter.

Counter Control Register (RTC_CCR)

MEM Offset (B0000400)	0B000040Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 399. Detailed Description of Counter Control Register (RTC_CCR)

Bits	Access Type	Default	Description
31:4	RO	28'h0	Reserved (RSVD1) Reserved



Bits	Access Type	Default	Description
3	RW	1'h0	Wrap Enable (RTC_WEN) This allows the user to force the counter to wrap when a match occurs instead of waiting for the max count: 0 - Wrap Disabled 1 - Wrap Enabled
2	RW	1'h0	Counter Enable (RTC_EN) Allows the user to control counting in the counter 0 - Counter Disabled 1 - Counter Enabled
1	RW	1'h0	Interrupt Mask (RTC_MASK) Allows the user to mask a generated interrupt 0 - Interrupt Un-Masked 1 - Interrupt Masked
0	RW	1'h0	Interrupt Enable (RTC_IEN) Allows the user to disable interrupt generation 0 - Interrupt Disabled 1 - Interrupt Enabled

Interrupt Status Register (RTC_STAT)

MEM Offset (B0000400)	0B0000410h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 400. Detailed Description of Interrupt Status Register (RTC_STAT)

Bits	Access Type	Default	Description
31:1	RO	31'h0	Reserved (RSVD1) Reserved
0	RO	1'h0	Interrupt Status (RTC_STAT) This register is the masked interrupt status 0 - Masked Interrupt is Inactive 1 - Masked Interrupt is Active

Interrupt Raw Status Register (RTC_RSTAT)

MEM Offset (B0000400)	0B0000414h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

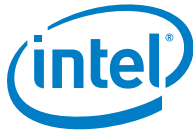


Table 401. Detailed Description of Interrupt Raw Status Register (RTC_RSTAT)

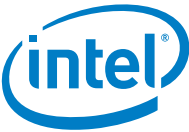
Bits	Access Type	Default	Description
31:1	RO	31'h0	Reserved (RSVD1) Reserved
0	RO	1'h0	Interrupt Raw Status (RTC_RSTAT) This register is the raw interrupt status. 0 - Raw Interrupt is Inactive 1 - Raw Interrupt is Active

End of Interrupt Register (RTC_EOI)

MEM Offset (B0000400)	0B0000418h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 402. Detailed Description of End of Interrupt Register (RTC_EOI)

Bits	Access Type	Default	Description
31:1	RO	31'h0	Reserved (RSVD1) Reserved
0	RO	1'h0	End of Interrupt (RTC_EOI) Reading this register will clear the match interrupt.

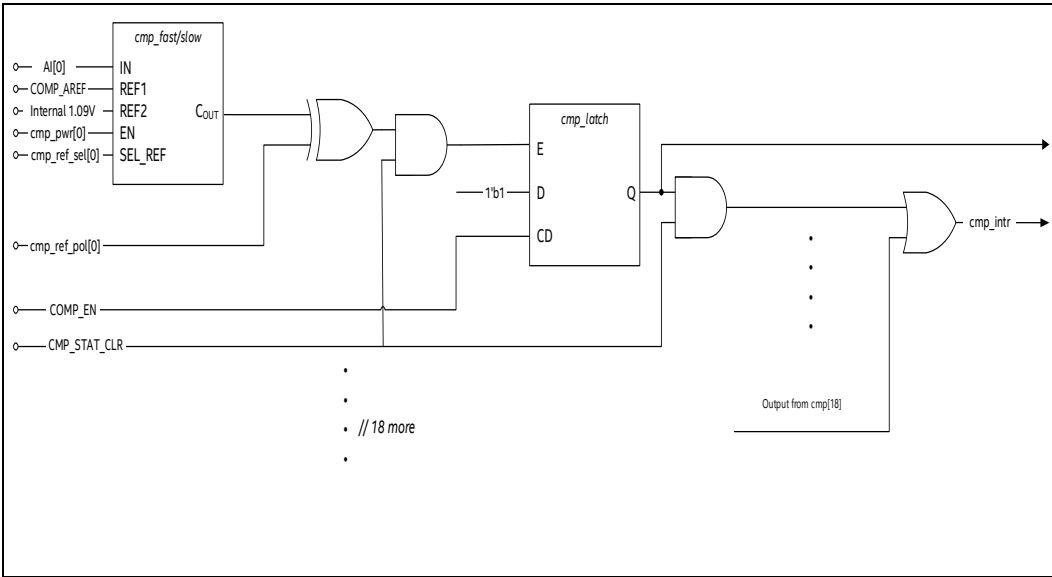


25 Comparators

The Intel® Quark™ SE Microcontroller C1000 supports 19 low power comparators which can be used to wake the system from low power states. Two types of comparators are supported, a low power and high performance version.

Each comparator can be powered down to achieve even lower power. Comparator reference supply is selectable between the Internal 1.09V reference and an external user supplied reference. The default configuration uses the external Reference Voltage. Refer to [Chapter 27.2.1 Summary of SCSS Registers](#) for more details on the register map.

Figure 35. Comparators



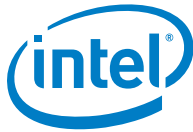
25.1 Signal Descriptions

Table 403. Memory Signals

Signal Name	Direction/Type	Description
AI[18:0]	I	External Comparator input
COMP_AREF	I	External Comparator reference voltage

25.2 Features

The following is a list of comparator features:



- 1.8V – 3.63 AVDD operation
- 1.2V – 1.98V DVDD operation
- Fast asynchronous comparator
- 1 positive and 2 negative inputs with selectable digital input
- Rail to rail input range
- CMPLP
 - <3.8us propagation delay
 - <600nA static current
 - <10mV hysteresis
 - <22nA power down current
- CMPHP
 - <0.25us propagation delay
 - <9.8uA static current
 - <4.6mV hysteresis
 - <2.7nA power down current
 - 2.0V – 3.63V AVCC operation
 - 1.2V – 1.98V DVCC operation

25.3 Use

The 19 comparators can be used in the following ways:

- To generate an interrupt to the processor
- To generate a wake event to cause the PMU to exit a deep sleep condition

The following sequence should be applied when setting up the comparator control to generate an interrupt or wake event:

1. Set CMP_REF_SEL for each comparator
2. Set CMP_REF_POL for each comparator
3. Set CMP_PWR for each comparator to '1'
4. Set CMP_EN for each comparator to '1'

The following sequence should be used when responding to an interrupt being asserted:

1. Read CMP_STAT_CLR for each comparator
2. Clear CMP_STAT_CLR for each firing comparator by writing a '1'



26 Mailbox

The Mailbox provides inter-processor communication via a mailbox-interrupt mechanism. The mechanism allows for a flexible software protocol to communicate information between the processors. The Mailbox is located in a memory space that is accessible by all processors in the system.

26.1 Features

The Mailbox presents 8 uni-directional communication channels. The channel allocation is described in the following table.

Table 404. Mailbox Channel Allocation

Channel Number	Source Processor	Destination Processor
0	Host	Sensor
1	Host	Sensor
2	Host	Sensor
3	Host	Sensor
4	Sensor	Host
5	Sensor	Host
6	Sensor	Host
7	Sensor	Host

This configuration supports flexible bi-directional communication between the Host Processor and the Sensor Processor. Each channel presents an identical programming model to all processors, along with a dedicated level sensitive interrupt that is routed in the Intel® Quark™ SE Microcontroller C1000 to the destination processor.

Each channel contains the base set of registers shown in the following table.

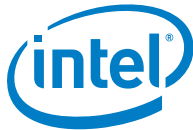


Table 405. Mailbox Channel Registers

Register Name	Register Description	Write Ownership
CHn_CTRL	Mailbox Channel N Control Word The Control Word (Bits 30 to 0) format/encoding is completely flexible and can be defined at the Mailbox software protocol level. For example, the Control Word could be a Message Identifier. A write of 1 to Bit 31 of this register will trigger the channel interrupt and set the corresponding flag in the CHn_STS register. The Payload Data, if any, should be populated in advance of writing to this register. This bit is cleared when a write is issued to CHn_STS[0] The source processor should not re-write the Control Word or any of the Payload Data if the status flag in CHn_STS is asserted.	Source Processor
CHn_DATA0	Mailbox Channel N Payload Data Word 0 1st 32bits of Data Payload	Source Processor
CHn_DATA1	Mailbox Channel N Payload Data Word 1 2nd 32bits of Data Payload	Source Processor
CHn_DATA2	Mailbox Channel N Payload Data Word 2 3rd 32bits of Data Payload	Source Processor
CHn_DATA3	Mailbox Channel N Payload Data Word 3 4th 32bits of Data Payload	Source Processor
CHn_STS[1:0]	Mailbox Channel N Status Bit[1] : This registers contains a single interrupt flag that represents the state of the channel interrupt. The Flag is set when a write to bit[31] of the CHn_CTRL occurs. The interrupt (and correspondingly the flag) is cleared by writing 1 to this bit. Bit[0] : This registers contains a single status flag that represents the state of the channel. The Flag is set when a write to bit[31] of the CHn_CTRL occurs. The status (and correspondingly the flag) is cleared by writing 1 to this status flag.	Destination Processor
CHALL_STS[15:0]	A read only register showing all status bits of the mailboxes CHn_STS[1:0]	Destination Processor

Note: The Write Ownership is not enforced by hardware and thus relies on correct software programming to enforce this.

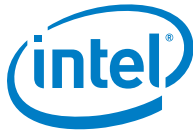
26.2 Use

Several uses are possible with the channel allocation described previously. The following table describes some of the possible uses.



Table 406. Mailbox Example Uses

Use Case	Description
Case 0	Message without Data from Host to Sensor, no response required (Posted): Host Processor programs CH0_CTRL register with appropriate Message ID. Writing 1 to the CH0_CTRL[31] causes the interrupt to assert and is reflected in both CHn_STS[1:0] bits. Sensor Processor receives interrupt from the mailbox The Interrupt handler reads the CHALL_STS[15:0] bits for all channels to ascertain which channel interrupt is set. The Interrupt handler writes a 1 to the CHn_STS[1] to clear the interrupt Sensor Processor reads the CHALL_STS[15:0] bits for all channels to ascertain which channel status is set. Sensor Processor reads the Message ID from the CH0_CTRL register Sensor Processor clears the Channel status by writing 1 to the flag in CH0_STS[0]
Case 1	Message with 128bits of Data from Sensor to Host, response required (Non-Posted): Sensor Processor programs the data into the CH2_DATA[0-3] registers. Sensor Processor programs CH2_CTRL register with appropriate Message ID Writing 1 to the CH0_CTRL[31] causes the interrupt to assert and is reflected in both CHn_STS[1:0] bits. Host Processor receives interrupt from Channel 2 The Interrupt handler reads the CHALL_STS[15:0] bits for all channels to ascertain which channel interrupt is set. The Interrupt handler writes a 1 to the CHn_STS[1] to clear the interrupt Host Processor reads the CHALL_STS[15:0] bits for all channels to ascertain which channel status is set. Host Processor reads the Message ID from the CH2_CTRL register Host Processor reads the data from the CH2_Data[0-3] registers Host Processor clears the Channel status by writing 1 to the flag in CH0_STS[0] Host Processor programs CH0_CTRL register with appropriate Response ID Sensor Processor receives interrupt from Channel 0 The Interrupt handler reads the CHALL_STS[15:0] bits for all channels to ascertain which channel interrupt is set. The Interrupt handler writes a 1 to the CHn_STS[1] to clear the interrupt Sensor Processor reads the Response ID from the CH0_CTRL register Sensor Processor clears the Channel status by writing 1 to the flag in CH0_STS[0]



Use Case	Description
Case 2	Message with greater than 128bits of Data from Sensor to Host, response required (Non-Posted): In this case the Mailbox data is stored in a memory location accessible by both processors and the data in the CH2_DATA[0-3] registers is a pointer/descriptor to that memory. Sensor Processor programs the memory pointer/descriptor into the CH2_DATA[0-3] registers. Sensor Processor programs CH2_CTRL register with appropriate Message ID Writing 1 to the CH0_CTRL[31] causes the interrupt to assert and is reflected in both CHn_STS[1:0] bits. Host Processor receives interrupt from Channel 2 Host Processor reads the Message ID from the CH2_CTRL register Host Processor reads the pointer/descriptor from the CH2_Data[0-3] registers Once the Host Processor has processed the data it clears the Channel 2 interrupt by writing 1 to the flag in CH2_STS Host Processor programs CH0_CTRL register with appropriate Response ID Sensor Processor receives interrupt from Channel 0 Sensor Processor reads the Response ID from the CH0_CTRL register Sensor Processor clears the Channel status by writing 1 to the flag in CH0_STS[0]



27 Interrupt Routing

The Interrupt Routing consists of several elements:

- Internal Host Processor Interrupts
- Internal Sensor Processor Interrupts
- Microcontroller Interrupts with configurable routing to either Processor
- Capability for microcontroller Interrupts to trigger a Processor Halt for Debug

27.1 Interrupt Routing

27.1.1 Host Processor Interrupts

The Interrupt Vector Assignments for the Host Processor are described in the following table.

Table 407. Host Processor Interrupt Vector Assignments

Vector No.	Description	Type
0	Divide Error	Exception
1	Debug Exception	Exception/Trap
2	NMI Interrupt	Interrupt
3	Breakpoint	Trap
4	Overflow	Trap
5	BOUND Range Exceeded	Exception
6	Invalid Opcode	Exception
7	Device Not Available	Exception
8	Double Fault	Abort
9	Intel Reserved.	N/A
10	Invalid TSS	Exception
11	Segment Not Present	Exception
12	Stack-Segment Fault	Exception
13	General Protection Fault	Exception
14	Page Fault	Exception
15	Intel Reserved.	N/A
16	Floating-Point Error	Exception
17	Alignment Check	Exception



Vector No.	Description	Type
18-31	Intel Reserved.	N/A
32-255	User Defined Interrupts	Interrupt

Interrupt Vectors 0 to 31 are due to events internal to the Host Processor, interrupts due to microcontroller events are routed through the User Defined Interrupts.

The User Defined Interrupts are delivered to the Host Processor via the IO APIC which maps particular Interrupt Inputs (IRQs) to configured Interrupt Vectors before presenting the interrupt to the Processor. The microcontroller Interrupt table shows the IRQ number into the IO APIC rather than the Interrupt Vector, which can be configured in the range 32 to 255.

27.1.2 Sensor Processor Interrupts

The Interrupt Vector Assignments for the Sensor Processor are described in the following table.

Table 408. Sensor Processor Interrupt Vector Assignments

Vector No.	Description	Type
0	Reset	Exception
1	Memory Error	Exception
2	Instruction Error	Exception
3	Machine Check Exception	Exception
4	Instruction TLB Miss	Exception
5	Data TLB Miss	Exception
6	Protection Violation	Exception
7	Privilege Violation	Exception
8	Software Interrupt	Exception
9	Trap	Trap
10	Extension Instruction Exception	Exception
11	Divide by Zero	Exception
12	Data Cache Consistency Error	Exception
13	Misaligned Data Access	Exception
14	Reserved.	N/A
15	Reserved.	N/A
16	Timer 0	Interrupt
17	Timer 1	Interrupt
18-67	User Defined Interrupts	Interrupt

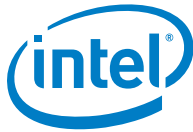


Interrupt Vectors 0 to 17 are due to events internal to the Sensor Processor, interrupts due to microcontroller events (including Sensor Subsystem Peripherals) are routed through the User Defined Interrupts.

27.1.3 Intel® Quark™ SE Microcontroller C1000 Interrupts and Routing

Table 409. Intel® Quark™ SE Microcontroller C1000 Interrupt List and Routing Capability

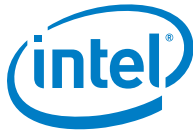
Interrupt Source	Description	Host Processor IRQ No.	Sensor Processor Interrupt Vector No.	Host Processor Halt for Debug	Sensor Processor Halt for Debug
SS ADC_ERR	Sensor Subsystem ADC Rx Fifo Error Interrupt	N/A	18	Y	Y
SS ADC_IRQ	Sensor Subsystem ADC Data Available Interrupt	N/A	19	Y	Y
SS GPIO_INTR_0	Sensor Subsystem GPIO Single Interrupt 0	N/A	20	Y	Y
SS GPIO_INTR_1	Sensor Subsystem GPIO Single Interrupt 1	N/A	21	Y	Y
SS I2C 0 ERR	Sensor Subsystem I2C 0 Error Interrupt	N/A	22	Y	Y
SS I2C 0 RX_AVAIL	Sensor Subsystem I2C 0 Data Available Interrupt	N/A	23	Y	Y
SS I2C 0 TX_REQ	Sensor Subsystem I2C 0 Data Required Interrupt	N/A	24	Y	Y
SS I2C 0 STOP_DET	Sensor Subsystem I2C 0 Stop Detect Interrupt	N/A	25	Y	Y
SS I2C 1 ERR	Sensor Subsystem I2C 1 Error Interrupt	N/A	26	Y	Y
SS I2C 1 RX_AVAIL	Sensor Subsystem I2C 1 Data Available Interrupt	N/A	27	Y	Y
SS I2C 1 TX_REQ	Sensor Subsystem I2C 1 Data Required Interrupt	N/A	28	Y	Y
SS I2C 1 STOP_DET	Sensor Subsystem I2C 1 Stop Detect Interrupt	N/A	29	Y	Y
SS SPI 0 ERR_INT	Sensor Subsystem SPI 0 Error Interrupt	N/A	30	Y	Y
SS SPI 0 RX_AVAIL	Sensor Subsystem SPI 0 Data Available Interrupt	N/A	31	Y	Y
SS SPI 0 TX_REQ	Sensor Subsystem SPI 0 Data Required Interrupt	N/A	32	Y	Y
SS SPI 1 ERR_INT	Sensor Subsystem SPI 1 Error Interrupt	N/A	33	Y	Y



Interrupt Source	Description	Host Processor IRQ No.	Sensor Processor Interrupt Vector No.	Host Processor Halt for Debug	Sensor Processor Halt for Debug
SS SPI 1 RX_AVAIL	Sensor Subsystem SPI 1 Data Available Interrupt	N/A	34	Y	Y
SS SPI 1 TX_REQ	Sensor Subsystem SPI 1 Data Required Interrupt	N/A	35	Y	Y
I2C MST 0	I2C Master 0 Single Interrupt	0	36	Y	Y
I2C MST 1	I2C Master 1 Single Interrupt	1	37	Y	Y
SPI MST 0	SPI Master 0 Single Interrupt	2	38	Y	Y
SPI MST 1	SPI Master 1 Single Interrupt	3	39	Y	Y
SPI SLV	SPI Slave Single Interrupt	4	40	Y	Y
UART 0	UART 0 Single Interrupt	5	41	Y	Y
UART 1	UART 1 Single Interrupt	6	42	Y	Y
I2S	I2S Single Interrupt	7	43	Y	Y
GPIO	GPIO Single Interrupt	8	44	Y	Y
PWM/Timer	PWM/Timer Single Interrupt	9	45	Y	Y
USB	USB Single Interrupt	10	46	Y	Y
RTC	RTC Single Interrupt	11	47	Y	Y
Watchdog	PWM/Timer Single Interrupt	12	48	Y	Y
DMA Channel 0	DMA Channel 0 Single Interrupt	13	49	Y	Y
DMA Channel 1	DMA Channel 1 Single Interrupt	14	50	Y	Y
DMA Channel 2	DMA Channel 2 Single Interrupt	15	51	Y	Y
DMA Channel 3	DMA Channel 3 Single Interrupt	16	52	Y	Y
DMA Channel 4	DMA Channel 4 Single Interrupt	17	53	Y	Y
DMA Channel 5	DMA Channel 5 Single Interrupt	18	54	Y	Y
DMA Channel 6	DMA Channel 6 Single Interrupt	19	55	Y	Y
DMA Channel 7	DMA Channel 7 Single Interrupt	20	56	Y	Y



Interrupt Source	Description	Host Processor IRQ No.	Sensor Processor Interrupt Vector No.	Host Processor Halt for Debug	Sensor Processor Halt for Debug
Mailbox[7:0]	8 Mailbox Channel Interrupts Routed to Single Interrupt with 8bit Mask per Destination	21	57	Y	Y
Comparators [18:0]	19 Comparators Routed to Single Interrupt with 19bit Mask per Destination	22	58	Y	Y
System/PMU	System and Power Management Single Interrupt	23	59	Y	Y
DMA Error[7:0]	8 DMA Channel Error Interrupts Routed to Single Interrupt with 8bit Mask per Destination	24	60	Y	Y
Int. SRAM Controller	Internal SRAM Memory Protection Error Single Interrupt	25	61	Y	Y
Int. Flash Controller 0	Internal Flash Controller 0 Memory Protection Error Single Interrupt	26	62	Y	Y
Int. Flash Controller 1	Internal Flash Controller 0 Memory Protection Error Single Interrupt	27	63	Y	Y
AON Timer	Always-On Timer Interrupt	28	64	Y	Y
ADC Power	ADC power sequence done	29	65	Y	Y
ADC Calibration	ADC calibration done	30	66	Y	Y
AON GPIO	Always-On GPIO Interrupt	31	67	Y	Y



28 System Control Subsystem

The System Control Subsystem (SCSS) contains functional blocks that control power sequencing, clock generation, reset generation, interrupt routing and pin muxing.

28.1 Features

The following is a list of the System Control Subsystem (SCSS) features:

- Clock Generation and Control
- Reset Generation
- Interrupt Routing
- Pin Mux Control
- Microcontroller Configuration Registers
- Always-On Counter
- Always-On Periodic Timer

28.2 Memory Mapped IO Registers

Registers listed are for the SCSS, starting at base address B0800000h.

28.2.1 Summary of SCSS Registers—0xB0800000

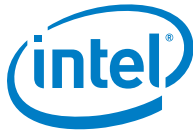
Hybrid Oscillator Configuration 0 (OSCO_CFG0)

MEM Offset (00000000)	0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 410. Detailed Description of Hybrid Oscillator Configuration 0 (OSC_CFG0)

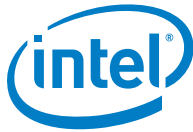
Bits	Access Type	Default	Description
31:24	RW/P/L	8'h0	Test Mode Inputs (OSC0_HYB_SET_REG4) OSC_CFG0[31:28]: Unused OSC_CFG0[27]: 0b: Gate output of silicon oscillator with LOCK signal 1b: Bypass LOCK and give out silicon oscillator output directly OSC_CFG0[26:25]: Silicon Oscillator Counter Test Mode Bits 32/16/8 MHz 00b: Count value = 44/22/6 (default) 01b: Count value = 68/34/17 10b: Count value = 24/12/3 11b: No output



Bits	Access Type	Default	Description
23:16	RW/P/L	8'h0	Test Mode Inputs (OSC0_HYB_SET_REG3) OSC0_CFG0[23]: 0b: Decrease RDAC code for retention mode 1b: Disable this option and feed the same code OSC0_CFG0[22:21]: Crystal Oscillator Counter Test Bits 00b: Count value: 3327 (default) 01b: Count value: 1279 10b: Count value: 7423 11b: Count value: 5375 OSC0_CFG0[20:19]: 00b: Default bias current to Gm MOS in crystal oscillator 01b: Increase bias current by 23% 10b: Decrease bias current by 23% 11b: Increase bias current by 46% OSC0_CFG0[18:17]: 00b: Default fixed cap in cap trim array crystal oscillator 01b: Increase fixed cap by 19% 10b: Decrease fixed cap by 38% 11b: Increase fixed cap by 38% OSC0_CFG0[16]: Unused



Bits	Access Type	Default	Description
15:8	RW/P/L	8'h0	Test Mode Inputs (OSC0_HYB_SET_REG2) OSC0_CFG0[15:14]: 00b: Default POR generation in silicon oscillator 01b: Delay POR generation in silicon oscillator 10b: Generate POR signal earlier than default 11b: Default start up of PTAT current reference OSC0_CFG0[13:12]: 00b: Default bias current to biasgen block for VREF generation 01b: Zero bias current 10b: Make the bias current 1.5 times its default value 11b: Make the bias current 0.5 times its default value OSC0_CFG0[11:10]: 00b: Default bias current to biasgen block amp 01b: Zero bias current 10b: Make the bias current 1.5 times its default value 11b: Make the bias current 0.5 times its default value OSC0_CFG0[9:8]: 00b: Default bias current to comparator 01b: Zero bias current 10b: Make the bias current 1.5 times its default value 11b: Make the bias current 0.5 times its default value



Bits	Access Type	Default	Description
7:0	RW/P/L	8'h0	Test Mode Inputs (OSC0_HYB_SET_REG1) OSC0_CFG0[7]: 0b: Gate output of crystal oscillator with LOCK 1b: Bypass LOCK and give out clock output directly OSC0_CFG0[6]: 0b: Default start up of PTAT current reference 1b: External start up for PTAT current reference OSC0_CFG0[5]: 0b: Default start up of compensated current reference 1b: External start up for compensated current reference OSC0_CFG0[4]: 0b: Default start up of PTAT current reference 1b: Select external start up for PTAT current reference OSC0_CFG0[3]: 0b: Default start up of compensated current reference 1b: Select external start up for compensated current reference OSC0_CFG0[2]: 0b: Cut start up current of both current references 1b: Disable cutting the start up branch current OSC0_CFG0[1]: 0b: Normal operation of silicon oscillator 1b: Trimming operation of silicon oscillator OSC0_CFG0[0]: 0b: Silicon oscillator works in normal mode (supply = 1.8V) 1b: Silicon oscillator works in retention mode (supply = 1.2V)

Hybrid Oscillator Status 1 (OSC0_STAT1)

MEM Offset (00000000) 4h
Security_PolicyGroup
IntelRsvd False



Size 32 bits
Default 0000_0000h

Table 411. Detailed Description of Hybrid Oscillator Status 1 (OSC0_STAT1)

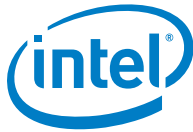
Bits	Access Type	Default	Description
31:2	RO	30'h0000_0000	RSVD (RSVD) Reserved
1	RO/V	1'h0	Crystal Oscillator Lock (OSC0_LOCK_XTAL) High output indicates crystal oscillator output is stable
0	RO/V	1'h0	Silicon Oscillator Lock (OSC0_LOCK_SI) High output indicates silicon oscillator output is stable

Hybrid Oscillator Configuration 1 (OSC0_CFG1)

MEM Offset (00000000) 8h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0302h

Table 412. Detailed Description of Hybrid Oscillator Configuration 1 (OSC0_CFG1)

Bits	Access Type	Default	Description	ResetSignal
31:30	RO	2'h0	RSVD (RSVD) Reserved	
29:20	RW/P/L	10'h0	Trim Code (OSC0_FTRIMOTP) 10-bit trim code	



Bits	Access Type	Default	Description	ResetSignal
19:16	RW/P/L	4'h0	Crystal oscillator trim (OSCO_FADJ_XTAL) Load cap corresponding to each trim code. 10 pF is the default load cap and the corresponding default trim code is 0000. 0111b: 5.55 pF 0110b: 6.18 pF 0101b: 6.82 pF 0100b: 7.45 pF 0011b: 8.08 pF 0010b: 8.71 pF 0001b: 9.34 pF 0000b: 10 pF 1111b: 10.61 pF 1110b: 11.24 pF 1101b: 11.88 pF 1100b: 12.51 pF 1011b: 13.14 pF 1010b: 13.77 pF 1001b: 14.4 pF 1000b: 15.03 pF	
15	RO	1'h0	RSVD (RSVD) Reserved	
14:13	RW/P/L	2'h0	Hybrid Oscillator Temperature Control (OSCO_TEMPCOMPPRG) Bits to control the temperature compensation of silicon oscillator 00b: Default temperature compensation 01b: Default temperature compensation 10b: Reduce PTAT current in temperature compensation 11b: Increase PTAT current in temperature compensation	
12:10	RW/P/L	3'h0	Hybrid Oscillator Bias Current Control (OSCO_IBIASPRG) Bits to control the bias current of the silicon oscillator	
9:8	RW/P	2'h3	Silicon Oscillator Frequency Selection (OSCO_SI_FREQ_SEL) 00b: 32 MHz 01b: 16 MHz 10b: 8 MHz 11b: 4 MHz	
7:5	RW/P/L	3'h0	Silicon Oscillator Start-Up (OSCO_START_UP) Bits to control the start-up of silicon oscillator core	



Bits	Access Type	Default	Description	ResetSignal
4	RW/P/L	1'h0	Crystal Oscillator Bypass Mode Enable (OSCO_BYP_XTAL) Enable bypass mode for crystal oscillator 0b: Disable 1b: Enable	
3	RW/P	1'h0	Hybrid Oscillator Mode Select (OSCO_MODE_SEL) Selects between crystal and silicon oscillator output 0b: Silicon oscillator output 1b: Crystal oscillator output	
2	RW/V/L	1'h0	Hybrid Oscillator Power-Down Control (OSCO_PD) 0b: Hybrid Oscillator in active mode 1b: Hybrid Oscillator in power down mode	pwr_rst_n
1	RW/P	1'h1	Silicon Oscillator Enable (OSCO_EN_SI_OSC) Enables the Silicon Oscillator 0b: Silicon Oscillator Disabled 1b: Silicon Oscillator Enabled	
0	RW/P	1'h0	Crystal Oscillator Enable (OSCO_EN_CRYSTAL) Enables the Crystal Oscillator 0b: Crystal Oscillator Disabled 1b: Crystal Oscillator Enabled	

RTC Oscillator Status (OSC1_STAT0)

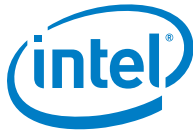
MEM Offset (00000000)	0Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 413. RTC Oscillator Status (OSC1_STAT0)

Bits	Access Type	Default	Description
31:1	RO	31'h0000_0000	RSVD (RSVD) Reserved
0	RO/V	1'h0	RTC Oscillator Lock (OSC1_LOCK_XTAL_OSC) High output indicates RTC Oscillator clock output has stabilized.

RTC Oscillator Configuration (OSC1_CFG0)

MEM Offset (00000000)	10h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits



Default

0000_0000h

Table 414. Detailed Description of RTC Oscillator Configuration (OSC1_CFG0)

Bits	Access Type	Default	Description	ResetSignal
31:18	RO	14'h0000	RSVD (RSVD) Reserved	
17:10	RW/P/L	8'h0	Debug mode test bits (OSC1_XTAL_32K_SET_REG2) OSC1_CFG0[17:10] Unused	
9:2	RW/P/L	8'h0	(OSC1_XTAL_32K_SET_REG1) Reserved	
1	RW/V/L	1'h0	RTC Oscillator Power-Down Control (OSC1_PD) 0b: RTC Oscillator in active mode 1b: RTC Oscillator in power down mode	pwr_rst_n
0	RW/P/L	1'h0	RTC Oscillator Bypass Mode Enable (OSC1_BYP_XTAL_UP) Enable bypass mode for RTC oscillator 0b: Disable 1b: Enable	

USB Phase Lock Loop (PLL) Configuration (USB_PLL_CFG0)**MEM Offset (00000000)**

14h

Security_PolicyGroup**IntelRsvd**

False

Size

32 bits

Default

0000_3012h

Please note that for a correct functioning of the USB the **USB_PLL_CFG0** register has to be set to:**0x3104**

Table 415. Detailed Description of USB Phase Lock Loop (PLL) Configuration (USB_PLL_CFG0)

Bits	Access Type	Default	Description
31:15	RO	17'h00000	RSVD (RSVD) Reserved
14	RO/V	1'h0	PLL Lock (USB_PLL_LOCK) High output indicates PLL output has locked



Bits	Access Type	Default	Description
13:11	RW/L	3'h6	Reference Frequency (USB_PLL_BW) Controls the reference clock frequency. 001b : 0.5-1.0 MHz 010b : 1-2 MHz 011b : 2-4 MHz 100b : 4-8 MHz 101b : 8-16 MHz 110b : 16-32 MHz
10	RW/L	1'h0	PLL Divide Mode (USB_PLL_DIVMODE) Controls if PLL output is VCO divided by 6 or divided by 8. 0b : VCO output divided by 8 1b : VCO output divided by 6
9:3	RW/L	7'h02	PLL Feedback Divider (USB_PLL_N) Controls the PLL Feedback Divider. Increases in steps of 8. 1111111b: Divide by 1024 0000000b: Divide by 8
2:1	RW/L	2'h1	PLL Input Clock Divider (USB_PLL_REFCLKDIV) Controls the PLL Input Clock Divider. 00b: divide by 1 01b: divide by 2 10b: divide by 4 11b: divide by 1
0	RW	1'h0	PLL Power-Down Control (USB_PLL_PDLD) 0b: PLL in power-down mode 1b: PLL in active mode

Peripheral Clock Gate Control (CCU_PERIPH_CLK_GATE_CTL)

MEM Offset (00000000)	18h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	003F_FFFFh

Table 416. Detailed Description of Peripheral Clock Gate Control (CCU_PERIPH_CLK_GATE_CTL)

Bits	Access Type	Default	Description
31:22	RO	10'h000	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
21	RW/P	1'b1	I2S PCLK Clock Gate Enable (CCU_I2S_PCLK_EN_SW) 1b: enable 0b: disable
20	RW/P	1'b1	I2C Master 1 PCLK Clock Gate Enable (CCU_I2C_M1_PCLK_EN_SW) 1b: enable 0b: disable
19	RW/P	1'b1	I2C master 0 PCLK Clock Gate Enable (CCU_I2C_M0_PCLK_EN_SW) 1b: enable 0b: disable
18	RW/P	1'b1	UART B PCLK Clock Gate Enable (CCU_UARTB_PCLK_EN_SW) 1b: enable 0b: disable
17	RW/P	1'b1	UART A PCLK Clock Gate Enable (CCU_UARTA_PCLK_EN_SW) 1b: enable 0b: disable
16	RW/P	1'b1	SPI slave PCLK Clock Gate Enable (CCU_SPI_PCLK_EN_SW) 1b: enable 0b: disable
15	RW/P	1'b1	SPI master 1 PCLK Clock Gate Enable (CCU_SPI_M1_PCLK_EN_SW) 1b: enable 0b: disable
14	RW/P	1'b1	SPI master 0 PCLK Clock Gate Enable (CCU_SPI_M0_PCLK_EN_SW) 1b: enable 0b: disable
13	RW/P	1'b1	GPIO PCLK Clock Gate Enable (CCU_GPIO_PCLK_EN_SW) 1b: enable 0b: disable
12	RW/P	1'b1	PWM PCLK Clock Gate Enable (CCU_PWM_PCLK_EN_SW) 1b: enable 0b: disable



Bits	Access Type	Default	Description
11	RW/P	1'b1	RTC PCLK Clock Gate Enable (CCU_RTC_PCLK_EN_SW) 1b: enable 0b: disable
10	RW/P	1'b1	Watch Dog Timer Clock Gate Enable (CCU_WDT_PCLK_EN_SW) 1b: enable 0b: disable
9	RW/P	1'b1	I2S Clock Enable (CCU_I2S_CLK_EN) 1b: enable 0b: disable
8	RW/P	1'b1	GPIO Debounce Clock Enable (CCU_PERIPH_GPIO_DB_CLK_EN) 1b: enable 0b: disable
7	RW/P	1'b1	GPIO interrupt Clock Enable (CCU_GPIO_INTR_CLK_EN) 1b: enable 0b: disable
6	RW/P	1'b1	SPI Master 1 clock enable (CCU_SPI_M1_CLK_EN) 1b: enable 0b: disable
5	RW/P	1'b1	SPI Master 0 clock enable (CCU_SPI_M0_CLK_EN) 1b: enable 0b: disable
4	RW/P	1'b1	SPI Slave Clock Enable (CCU_SPI_S_CLK_EN) 1b: enable 0b: disable
3	RW/P	1'b1	I2C Master 1 Clock enable (CCU_I2C_M1_CLK_EN) 1b: enable 0b: disable
2	RW/P	1'b1	I2C Master 0 Clock enable (CCU_I2C_M0_CLK_EN) 1b: enable 0b: disable
1	RW/P	1'b1	Peripheral clock enable (CCU_PERIPH_CLK_EN) 1b: enable 0b: disable
0	RW/P	1'b1	PERIPH_PCLK_EN (PERIPH_PCLK_EN) 1b: enable 0b: disable

**Peripheral Clock Divider Control 0 (CCU_PERIPH_CLK_DIV_CTL0)**

MEM Offset (00000000) 1Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0001h

Table 417. Detailed Description of Peripheral Clock Divider Control 0 (CCU_PERIPH_CLK_DIV_CTL0)

Bits	Access Type	Default	Description
31:3	RO	29'h0000_0000	RSVD (RSVD) Reserved
2:1	RW/P	2'h0	Peripheral Clock Divider (CCU_PERIPH_PCLK_DIV) 00b: divide by 1 01b: divide by 2 10b: divide by 4 11b: divide by 8
0	RW/P	1'b1	Peripheral Clock divider enable (CCU_PERIPH_PCLK_DIV_EN) This bit must be written from 0 -> 1 to apply the value

Peripheral Clock Divider Control 1 (CCU_GPIO_DB_CLK_CTL)

MEM Offset (00000000) 20h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0003h

Table 418. Detailed Description of Peripheral Clock Divider Control 1 (CCU_GPIO_DB_CLK_CTL)

Bits	Access Type	Default	Description
31:5	RO	27'h0000000	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
4:2	RW/P	3'h0	GPIO debounce clock divider (CCU_GPIO_DB_CLK_DIV) 000b: divide by 1 001b: divide by 2 010b: divide by 4 011b: divide by 8 100b: divide by 16 101b: divide by 32 110b: divide by 64 111b: divide by 128
1	RW/P	1'b1	GPIO debounce clock divider enable (CCU_GPIO_DB_CLK_DIV_EN) This bit must be written from 0 -> 1 to apply the value
0	RW/P	1'b1	GPIO Debounce Clock Enable - Sensor Subsystem (CCU_GPIO_DB_CLK_EN) 1b: enable 0b: disable

External Clock Control (CCU_EXT_CLOCK_CTL)

MEM Offset (00000000)	24h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0007h

Table 419. Detailed Description of External Clock Control (CCU_EXT_CLOCK_CTL)

Bits	Access Type	Default	Description
31:5	RO	27'h0000000	RSVD (RSVD) Reserved
4:3	RW/P	2'h0	External clock divider (CCU_EXT_CLK_DIV) 00b: divide by 1 01b: divide by 2 10b: divide by 4 11b: divide by 8
2	RW/P	1'b1	External clock divider enable (CCU_EXT_CLK_DIV_EN) This bit must be written from 0 -> 1 to apply the value



Bits	Access Type	Default	Description
1	RW/P	1'b1	External Clock Enable (CCU_EXT_CLK_EN) 1b: enable 0b: disable
0	RW/P	1'b1	External RTC enable (CCU_EXT_RTC_EN) 1b: enable 0b: disable

Sensor Subsystem Peripheral Clock Gate Control (CCU_SS_PERIPH_CLK_GATE_CTL)

MEM Offset (00000000) 28h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_00FFh

Table 420. Detailed Description of Sensor Subsystem Peripheral Clock Gate Control (CCU_SS_PERIPH_CLK_GATE_CTL)

Bits	Access Type	Default	Description
31:8	RO	24'h000000	RSVD (RSVD) Reserved
7	RW/P	1'b1	ADC Clock Enable - Sensor Subsystem (CCU_ADC_CLK_EN) 1b: enable 0b: disable
6	RW/P	1'b1	GPIO Debounce Clock Enable - Sensor Subsystem (CCU_SS_GPIO_DB_CLK_EN) 1b: enable 0b: disable
5	RW/P	1'b1	GPIO interrupt Clock Enable - Sensor Subsystem (CCU_SS_GPIO_INTR_CLK_EN) 1b: enable 0b: disable
4	RW/P	1'b1	SPI Master 1 clock enable - Sensor Subsystem (CCU_SS_SPI_M1_CLK_EN) 1b: enable 0b: disable
3	RW/P	1'b1	SPI Master 0 clock enable - Sensor Subsystem (CCU_SS_SPI_M0_CLK_EN) 1b: enable 0b: disable



Bits	Access Type	Default	Description
2	RW/P	1'b1	I2C Master 1 Clock enable - Sensor Subsystem (CCU_SS_I2C_M1_CLK_EN) 1b: enable 0b: disable
1	RW/P	1'b1	I2C Master 0 Clock enable - Sensor Subsystem (CCU_SS_I2C_M0_CLK_EN) 1b: enable 0b: disable
0	RW/P	1'b1	Sensor Clock enable (CCU_SENSOR_CLK_EN) 1b: enable 0b: disable

System Low Power Clock Control (CCU_LP_CLK_CTL)

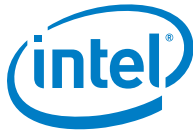
MEM Offset (00000000)	2Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 421. Detailed Description of System Low Power Clock Control (CCU_LP_CLK_CTL)

Bits	Access Type	Default	Description
31:2	RO	30'h0000_0000	RSVD (RSVD) Reserved
1	RW/P	1'b0	CCU Host C2 Low Power Enable (CCU_C2_LP_EN) When enabled, hardware will gate the clock to the Host Processor, including Local and I/O APICs, whenever the Host Processor enters C2. When disabled, the clock to the Host Processor is never gated and only functional clock gating within the Host Processor is enabled during C2. 0b : Host C2 Low Power Disabled 1b : Host C2 Low Power Enabled
0	RW/P	1'b0	CCU SS Low Power Sensing Enable (CCU_SS_LPS_EN) 1b: enable 0b: disable

AHB Control (CCU_MLAYER_AHB_CTL)

MEM Offset (00000000)	34h



Security_PolicyGroup
IntelRsvd
Size
Default

False
32 bits
0000_38DDh

Table 422. Detailed Description of AHB Control (CCU_MLAYER_AHB_CTL)

Bits	Access Type	Default	Description
31:17	RO	15'h0000	RSVD (RSVD) Reserved
10:8	RO	3'h0	RSVD (RSVD) Reserved
7	RW/P	1'b1	External SRAM Clock enable (CCU_EXT_SRAM_CLK_EN) 1b: enable 0b: disable
6	RW/P	1'b1	DMA Clock enable (CCU_DMA_CLK_EN) 1b: enable 0b: disable
5	RO	1'h0	RSVD (RSVD) Reserved
4	RW/P	1'b1	SRAM Clock Enable (CCU_SRAM_CLK_EN) 1b: enable 0b: disable
3	RW/P	1'b1	FLASH 1 Clock Enable (CCU_FLASH1_CLK_EN) 1b: enable 0b: disable
2	RW/P	1'b1	FLASH 0 Clock Enable (CCU_FLASH0_CLK_EN) 1b: enable 0b: disable
1	RW/P	1'b0	USB Clock Enable (CCU_USB_CLK_EN) 1b: enable 0b: disable

System Clock Control (CCU_SYS_CLK_CTL)

MEM Offset (00000000)
Security_PolicyGroup
IntelRsvd
Size
Default

38h
False
32 bits
0000_0087h

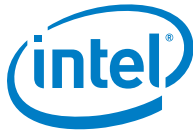


Table 423. Detailed Description of System Clock Control (CCU_SYS_CLK_CTL)

Bits	Access Type	Default	Description
31:10	RO	22'h000000	RSVD (RSVD) Reserved
9:8	RW/P	2'h0	System Clock Divider (CCU_SYS_CLK_DIV) 00b: divide by 1 01b: divide by 2 10b: divide by 4 11b: divide by 8
7	RW/P	1'b1	System Clock Divider Enable (CCU_SYS_CLK_DIV_EN) This bit must be written from 0 -> 1 to apply the value
6:3	RW/P/L	4'h0	RTC Clock Divider (CCU_RTC_CLK_DIV) 0000b: divide by 1 0001b: divide by 2 0010b: divide by 4 0011b: divide by 8 0100b: divide by 16 0101b: divide by 32 0110b: divide by 64 0111b: divide by 128 1000b: divide by 256 1001b: divide by 512 1010b: divide by 1024 1011b: divide by 2048 1100b: divide by 4096 1101b: divide by 8192 1110b: divide by 16384 1111b: divide by 32768
2	RW/P/L	1'b1	RTC Clock Divider Enable (CCU_RTC_CLK_DIV_EN) This bit must be written from 0 -> 1 to apply the value
1	RW/P/L	1'b1	RTC Clock Enable (CCU_RTC_CLK_EN) 1b: enable 0b: disable
0	RW/P	1'b1	Select Clock (CCU_SYS_CLK_SEL) 0b: 32 kHz RTC Crystal Oscillator 1b: 32 MHz Hybrid Oscillator

Clocks Lock (OSC_LOCK_0)**MEM Offset (00000000)**

3Ch



Security_PolicyGroup

IntelRsvd

False

Size

32 bits

Default

0000_0000h

Table 424. Detailed Description of Clocks Lock (OSC_LOCK_0)

Bits	Access Type	Default	Description	ResetSignal
31	RW/1S	1'h0	Test Mode Input 4 Lock (OSC0_HYB_SET_REG4_LOCK) 1b: Lock	pwr_rst_n
30	RW/1S	1'h0	Test Mode Input 3 Lock (OSC0_HYB_SET_REG3_LOCK) 1b: Lock	pwr_rst_n
29	RW/1S	1'h0	Test Mode Input 2 Lock (OSC0_HYB_SET_REG2_LOCK) 1b: Lock	pwr_rst_n
28	RW/1S	1'h0	Test Mode Input 1 Lock (OSC0_HYB_SET_REG1_LOCK) 1b: Lock	pwr_rst_n
27	RW/1S	1'h0	10 bit trim code from OTP Lock (OSC0_FTRIMOTP_LOCK) 1b: Lock	pwr_rst_n
26	RW/1S	1'h0	Crystal oscillator trim Lock (OSC0_FADJ_XTAL_LOCK) 1b: Lock	pwr_rst_n
25	RW/1S	1'h0	Oscillator 0 Temperature Control Lock (OSC0_TEMPCOMPPRG_LOCK) 1b: Lock	pwr_rst_n
24	RW/1S	1'h0	Oscillator 0 bias current Control Lock (OSC0_IBIASPRG_LOCK) 1b: Lock	pwr_rst_n
23	RW/1S	1'h0	Oscillator 0 start-up Lock (OSC0_START_UP_LOCK) 1b: Lock	pwr_rst_n
22	RW/1S	1'h0	Oscillator 0 Bypass Mode Enable Lock (OSC0_BYP_XTAL_LOCK) 1b: Lock	pwr_rst_n
21	RO	1'h0	RSVD (RSVD) Reserved	
20	RW/1S	1'h0	Debug mode test bits Reg 2 Lock (OSC1_XTAL_32K_SET_REG2_LOCK) 1b: Lock	pwr_rst_n



Bits	Access Type	Default	Description	ResetSignal
19	RW/1S	1'h0	Debug mode test bits Reg 1 Lock (OSC1_XTAL_32K_SET_REG1_LOCK) 1b: Lock	pwr_rst_n
18	RW/1S	1'h0	RTC Enable Bypass mode Lock (OSC1_BYP_XTAL_UP_LOCK) 1b: Lock	pwr_rst_n
17	RW/1S	1'h0	Program reference frequency Lock (USB_PLL_BW_LOCK) 1b: Lock	pwr_rst_n
16	RW/1S	1'h0	PLL Program the clkdiv68 Lock (USB_PLL_DIVMODE_LOCK) 1b: Lock	pwr_rst_n
15	RW/1S	1'h0	PLL feedback programmable divider Lock (USB_PLL_N_LOCK) 1b: Lock	pwr_rst_n
14	RW/1S	1'h0	PLL Input clock divider setting Lock (USB_PLL_REFCLKDIV_LOCK) 1b: Lock	pwr_rst_n
13	RW/1S	1'h0	RTC Divider Lock (RTC_DIV_LOCK) 1b: Lock	pwr_rst_n
12	RW/1S	1'h0	OSC1 Power-Down Lock (OSC1_PD_LOCK) 1b: Lock	pwr_rst_n
11:0	RO	12'h000	RSVD (RSVD) Reserved	

General Purpose Sticky Scratchpad 0 (GPS0)

MEM Offset (00000000)	100h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 425. Detailed Description of General Purpose Sticky Scratchpad 0 (GPS0)

Bits	Access Type	Default	Description
31:0	RW/P	32'h0	Sticky Scratchpad 0 (GPS0) Cleared on POR or COLD reset

General Purpose Sticky Scratchpad 1 (GPS1)

MEM Offset (00000000)	104h
Security_PolicyGroup	
IntelRsvd	False



Size 32 bits
Default 0000_0000h

Table 426. Detailed Description of General Purpose Sticky Scratchpad 1 (GPS1)

Bits	Access Type	Default	Description
31:0	RW/P	32'h0	Sticky scratchpad 1 (GPS1) Cleared on POR or COLD reset

General Purpose Sticky Scratchpad 2 (GPS2)

MEM Offset (00000000) 108h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 427. Detailed Description of General Purpose Sticky Scratchpad 2 (GPS2)

Bits	Access Type	Default	Description
31:0	RW/P	32'h0	Sticky scratchpad 2 (GPS2) Cleared on POR or COLD reset

General Purpose Sticky Scratchpad 3 (GPS3)

MEM Offset (00000000) 10Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 428. Detailed Description of General Purpose Sticky Scratchpad 3 (GPS3)

Bits	Access Type	Default	Description
31:0	RW/P	32'h0	Sticky scratchpad 3 (GPS3) Cleared on POR or COLD reset

General Purpose Scratchpad 0 (GP0)

MEM Offset (00000000) 114h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h



Table 429. Detailed Description of General Purpose Scratchpad 0 (GP0)

Bits	Access Type	Default	Description
31:0	RW	32'h0	General Purpose Scratchpad 0 (GP0) Cleared on POR or COLD or WARM reset

General Purpose Scratchpad 1 (GP1)

MEM Offset (00000000)	118h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 430. Detailed Description of General Purpose Scratchpad 1 (GP1)

Bits	Access Type	Default	Description
31:0	RW	32'h0	General Purpose Scratchpad 1 (GP1) Cleared on POR or COLD or WARM reset

General Purpose Scratchpad 2 (GP2)

MEM Offset (00000000)	11Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 431. Detailed Description of General Purpose Scratchpad 2 (GP2)

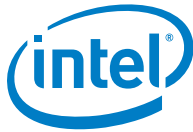
Bits	Access Type	Default	Description
31:0	RW	32'h0	General Purpose Scratchpad 2 (GP2) Cleared on POR or COLD or WARM reset

General Purpose Scratchpad 3 (GP3)

MEM Offset (00000000)	120h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 432. Detailed Description of General Purpose Scratchpad 3 (GP3)

Bits	Access Type	Default	Description
31:0	RW	32'h0	General Purpose Scratchpad 3 (GP3) Cleared on POR or COLD or WARM reset

**Identification (ID)**

MEM Offset (00000000) 128h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0010h

Table 433. Detailed Description of Identification (ID)

Bits	Access Type	Default	Description
31:8	RO	24'h000000	RSVD (RSVD) Reserved
7:0	RO	8'h10	Major Revision ID (ID) Identifies microcontroller revision. 10h : Revision 1.0

Revision (REV)

MEM Offset (00000000) 12Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 434. Detailed Description of Revision (REV)

Bits	Access Type	Default	Description
31:8	RO	24'h000000	RSVD (RSVD) Reserved
7:0	RO	8'h00	Minor Revision ID (REV) Read-Only Revision register at fixed location in Memory map

Write-One-to-Set Scratchpad (WO_SP)

MEM Offset (00000000) 130h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h



Table 435. Detailed Description of Write-One-to-Set Scratchpad (WO_SP)

Bits	Access Type	Default	Description
31:0	RW/1S	32'h0	Write-One-to-Set (WO_SP) This field provides Read/Write-One-to-Set behavior on a per bit basis.

Write-One-to-Set Sticky Scratchpad (WO_ST)

MEM Offset (00000000)	134h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 436. Detailed Description of Write-One-to-Set Sticky Scratchpad (WO_ST)

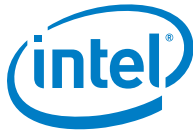
Bits	Access Type	Default	Description	ResetSignal
31:0	RW/1S	32'h0	Write-One-to-Set (WO_ST) This field provides sticky Read/Write-One-to-Set behavior on a per bit basis. Sticky.	pwr_rst_n

Memory Control (MEM_CTRL)

MEM Offset (00000000)	200h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0801h

Table 437. Detailed Description of Memory Control (MEM_CTRL)

Bits	Access Type	Default	Description
31:12	RO	20'h00000	RSVD (RSVD) Reserved
11	RW	1'h1	External SRAM IO Disable (SRAM_OUTPUT_DISABLE) 0b: External SRAM IO Enabled 1b: External SRAM IO Disabled
10:1	RO	10'h000	RSVD (RSVD) Reserved
0	RW	1'b1	External SRAM Power Down (MEMCTL_SM_CS2_N) 0b: External SRAM Power Down Disabled 1b: External SRAM Power Down Enabled

**Comparator enable (CMP_EN)**

MEM Offset (00000000) 300h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 438. Detailed Description of Comparator enable (CMP_EN)

Bits	Access Type	Default	Description
31:19	RO	13'h0000	RSVD (RSVD) Reserved
18:0	RW/P	19'h0	Comparator enable (CMP_EN) 0b comparator will not fire. 1b comparator will fire.

Comparator reference select (CMP_REF_SEL)

MEM Offset (00000000) 304h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 439. Detailed Description of Comparator reference select (CMP_REF_SEL)

Bits	Access Type	Default	Description
31:19	RO	13'h0000	RSVD (RSVD) Reserved
18:0	RW/P	19'h0	Comparator reference select (CMP_REF_SEL) 0b: Selects Reference from external voltage reference (CMP_AREF pad). 1b: Selects Reference from internal voltage reference output of voltage regulator (1.09V typ).

Comparator Reference Polarity Select (CMP_REF_POL)

MEM Offset (00000000) 308h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h



Table 440. Detailed Description of Comparator Reference Polarity Select (CMP_REF_POL)

Bits	Access Type	Default	Description
31:19	RO	13'h0000	RSVD (RSVD) Reserved
18:0	RW/P	19'h0	Comparator Reference Polarity Select (CMP_REF_POL) 0b: Comparator monitors if Analog input voltage is greater than voltage reference. 1b: Comparator monitors if Analog input voltage is lesser than voltage reference.

Comparator Power Enable (CMP_PWR)

MEM Offset (00000000) 30Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 441. Detailed Description of Comparator Power Enable (CMP_PWR)

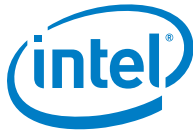
Bits	Access Type	Default	Description
31:19	RO	13'h0000	RSVD (RSVD) Reserved
18:0	RW/P	19'h0	Comparator Power Enable (CMP_PWR) Each bit of this register manages over one out of nineteen comparators. For each comparator: 1b: enable 0b: disable

Comparator Status Clear (CMP_STAT_CLR)

MEM Offset (00000000) 328h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 442. Detailed Description of Comparator Status Clear (CMP_STAT_CLR)

Bits	Access Type	Default	Description
31:19	RO	13'h0000	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
18:0	RW/1C/V/P	19'h0	Comparator Status Clear (CMP_STAT_CLR) The current status of the latched value of the comparator. Software must clear the latch before another interrupt. Each bit of this register manages over one out of nineteen comparators. For each comparator: 1b: clear

Sensor Subsystem Interrupt Routing Mask 0 (INT_SS_ADC_ERR_MASK)

MEM Offset (00000000)	400h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 443. Detailed Description of Sensor Subsystem Interrupt Routing Mask 0 (INT_SS_ADC_ERR_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	ADC Error SS Halt Mask - Sensor Subsystem (INT_SS_ADC_ERR_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	ADC Error Host Halt Mask - Sensor Subsystem (INT_SS_ADC_ERR_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	ADC Error SS Mask - Sensor Subsystem (INT_SS_ADC_ERR_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	ADC Error Host Mask - Sensor Subsystem (INT_SS_ADC_ERR_HOST_MASK)

Sensor Subsystem Interrupt Routing Mask 1 (INT_SS_ADC_IRQ_MASK)

MEM Offset (00000000)	404h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h



Table 444. Detailed Description of Sensor Subsystem Interrupt Routing Mask 1 (INT_SS_ADC_IRQ_MASK)

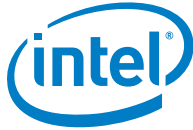
Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	ADC Request SS Halt Mask - Sensor Subsystem (INT_SS_ADC_IRQ_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	ADC Request Host Halt Mask - Sensor Subsystem (INT_SS_ADC_IRQ_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	ADC Request SS Mask - Sensor Subsystem (INT_SS_ADC_IRQ_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	ADC Request Host Mask - Sensor Subsystem (INT_SS_ADC_IRQ_HOST_MASK)

Sensor Subsystem Interrupt Routing Mask 2 (INT_SS_GPIO_0_INTR_MASK)

MEM Offset (00000000)	408h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 445. Detailed Description of Sensor Subsystem Interrupt Routing Mask 2 (INT_SS_GPIO_0_INTR_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	GPIO SS Halt Interrupt Mask - Sensor Subsystem (INT_SS_GPIO_0_INTR_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	GPIO Host Halt Interrupt Mask - Sensor Subsystem (INT_SS_GPIO_0_INTR_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
8	RW/P/L	1'b1	GPIO SS Interrupt Mask - Sensor Subsystem (INT_SS_GPIO_0_INTR_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	GPIO Host Interrupt Mask - Sensor Subsystem (INT_SS_GPIO_0_INTR_HOST_MASK)

Sensor Subsystem Interrupt Routing Mask 3 (INT_SS_GPIO_1_INTR_MASK)

MEM Offset (00000000)	40Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 446. Detailed Description of Sensor Subsystem Interrupt Routing Mask 3 (INT_SS_GPIO_1_INTR_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	GPIO SS Halt Interrupt Mask - Sensor Subsystem (INT_SS_GPIO_1_INTR_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	GPIO Host Halt Interrupt Mask - Sensor Subsystem (INT_SS_GPIO_1_INTR_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	GPIO SS Interrupt Mask - Sensor Subsystem (INT_SS_GPIO_1_INTR_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	GPIO Host Interrupt Mask - Sensor Subsystem (INT_SS_GPIO_1_INTR_HOST_MASK)

Sensor Subsystem Interrupt Routing Mask 4 (INT_SS_I2C_0_ERR_MASK)

MEM Offset (00000000)	410h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h



Table 447. Detailed Description of Sensor Subsystem Interrupt Routing Mask 4 (INT_SS_I2C_0_ERR_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	I2C0 Error SS Halt Mask - Sensor Subsystem (INT_SS_I2C_0_ERR_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	I2C0 Error Host Halt Mask - Sensor Subsystem (INT_SS_I2C_0_ERR_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	I2C0 Error SS Mask - Sensor Subsystem (INT_SS_I2C_0_ERR_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	I2C0 Error Host Mask - Sensor Subsystem (INT_SS_I2C_0_ERR_HOST_MASK)

Sensor Subsystem Interrupt Routing Mask 5 (INT_SS_I2C_0_RX_AVAIL_MASK)

MEM Offset (00000000)	414h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 448. Detailed Description of Sensor Subsystem Interrupt Routing Mask 5 (INT_SS_I2C_0_RX_AVAIL_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	I2C0 Receive Available SS Halt Mask - Sensor Subsystem (INT_SS_I2C_0_RX_AVAIL_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	I2C0 Receive Available Host Halt Mask - Sensor Subsystem (INT_SS_I2C_0_RX_AVAIL_HOST_HALT_MASK)



Bits	Access Type	Default	Description
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	I2C0 Receive Available SS Mask - Sensor Subsystem (INT_SS_I2C_0_RX_AVAIL_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	I2C0 Receive Available Host Mask - Sensor Subsystem (INT_SS_I2C_0_RX_AVAIL_HOST_MASK)

Sensor Subsystem Interrupt Routing Mask 6 (INT_SS_I2C_0_TX_REQ_MASK)

MEM Offset (00000000)	418h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 449. Detailed Description of Sensor Subsystem Interrupt Routing Mask 6 (INT_SS_I2C_0_TX_REQ_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	I2C0 Transmission SS Halt Request Mask - Sensor Subsystem (INT_SS_I2C_0_TX_REQ_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	I2C0 Transmission Host Halt Request Mask - Sensor Subsystem (INT_SS_I2C_0_TX_REQ_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	I2C0 Transmission SS Request Mask - Sensor Subsystem (INT_SS_I2C_0_TX_REQ_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	I2C0 Transmission Host Request Mask - Sensor Subsystem (INT_SS_I2C_0_TX_REQ_HOST_MASK)

Sensor Subsystem Interrupt Routing Mask 7 (INT_SS_I2C_0_STOP_DET_MASK)

MEM Offset (00000000)	41Ch



Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0101_0101h

Table 450. Detailed Description of Sensor Subsystem Interrupt Routing Mask 7 (INT_SS_I2C_0_STOP_DET_MASK)

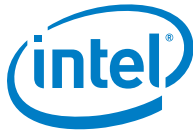
Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	I2C0 Stop Detect SS Halt Mask - Sensor Subsystem (INT_SS_I2C_0_STOP_DET_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	I2C0 Stop Detect Host Halt Mask - Sensor Subsystem (INT_SS_I2C_0_STOP_DET_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	I2C0 Stop Detect SS Mask - Sensor Subsystem (INT_SS_I2C_0_STOP_DET_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	I2C0 Stop Detect Host Mask - Sensor Subsystem (INT_SS_I2C_0_STOP_DET_HOST_MASK)

Sensor Subsystem Interrupt Routing Mask 8 (INT_SS_I2C_1_ERR_MASK)

MEM Offset (00000000) 420h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0101_0101h

Table 451. Detailed Description of Detailed Description of Sensor Subsystem Interrupt Routing Mask 8 (INT_SS_I2C_1_ERR_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	I2C1 Error SS Halt Mask - Sensor Subsystem (INT_SS_I2C_1_ERR_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
16	RW/P/L	1'b1	I2C1 Error Host Halt Mask - Sensor Subsystem (INT_SS_I2C_1_ERR_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	I2C1 Error SS Mask - Sensor Subsystem (INT_SS_I2C_1_ERR_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	I2C1 Error Host Mask - Sensor Subsystem (INT_SS_I2C_1_ERR_HOST_MASK)

Sensor Subsystem Interrupt Routing Mask 9 (INT_SS_I2C_1_RX_AVAIL_MASK)

MEM Offset (00000000)	424h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 452. Detailed Description of Sensor Subsystem Interrupt Routing Mask 9 (INT_SS_I2C_1_RX_AVAIL_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	I2C1 Receive Available SS Halt Mask - Sensor Subsystem (INT_SS_I2C_1_RX_AVAIL_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	I2C1 Receive Available Host Halt Mask - Sensor Subsystem (INT_SS_I2C_1_RX_AVAIL_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	I2C1 Receive Available SS Mask - Sensor Subsystem (INT_SS_I2C_1_RX_AVAIL_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
0	RW/P/L	1'b1	I2C1 Receive Available Host Mask - Sensor Subsystem (INT_SS_I2C_1_RX_AVAIL_HOST_MASK)

Sensor Subsystem Interrupt Routing Mask 10 (INT_SS_I2C_1_TX_REQ_MASK)

MEM Offset (00000000)	428h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 453. Detailed Description of Sensor Subsystem Interrupt Routing Mask 10 (INT_SS_I2C_1_TX_REQ_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	I2C1 Transmission Host Halt Request Mask - Sensor Subsystem (INT_SS_I2C_1_TX_REQ_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	I2C1 Transmission Host Halt Request Mask - Sensor Subsystem (INT_SS_I2C_1_TX_REQ_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	I2C1 Transmission SS Request Mask - Sensor Subsystem (INT_SS_I2C_1_TX_REQ_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	I2C1 Transmission Host Request Mask - Sensor Subsystem (INT_SS_I2C_1_TX_REQ_HOST_MASK)

Sensor Subsystem Interrupt Routing Mask 11 (INT_SS_I2C_1_STOP_DET_MASK)

MEM Offset (00000000)	42Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

**Table 454. Detailed Description of Sensor Subsystem Interrupt Routing Mask 11
(INT_SS_I2C_1_STOP_DET_MASK)**

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	2C1 Stop Detect SS Halt Mask - Sensor Subsystem (INT_SS_I2C_1_STOP_DET_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	I2C1 Stop Detect Host Halt Mask - Sensor Subsystem (INT_SS_I2C_1_STOP_DET_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	I2C1 Stop Detect SS Mask - Sensor Subsystem (INT_SS_I2C_1_STOP_DET_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	I2C1 Stop Detect Host Mask - Sensor Subsystem (INT_SS_I2C_1_STOP_DET_HOST_MASK)

Sensor Subsystem Interrupt Routing Mask 12 (INT_SS_SPI_0_ERR_INT_MASK)

MEM Offset (00000000)	430h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

**Table 455. Detailed Description of Sensor Subsystem Interrupt Routing Mask 12
(INT_SS_SPI_0_ERR_INT_MASK)**

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	SPIO Error SS Halt Mask - Sensor Subsystem (INT_SS_SPI_0_ERR_SS_HALT_INT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	SPIO Error Host Halt Mask - Sensor Subsystem (INT_SS_SPI_0_ERR_HOST_HALT_INT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
8	RW/P/L	1'b1	SPIO Error SS Mask - Sensor Subsystem (INT_SS_SPI_0_ERR_SS_INT_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	SPIO Error Host Mask - Sensor Subsystem (INT_SS_SPI_0_ERR_HOST_INT_MASK)

Sensor Subsystem Interrupt Routing Mask 13 (INT_SS_SPI_0_RX_AVAIL_MASK)

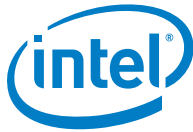
MEM Offset (00000000)	434h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 456. Detailed Description of Sensor Subsystem Interrupt Routing Mask 13 (INT_SS_SPI_0_RX_AVAIL_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	SPIO Receive Available SS Halt Mask - Sensor Subsystem (INT_SS_SPI_0_RX_AVAIL_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	SPIO Receive Available Host Halt Mask - Sensor Subsystem (INT_SS_SPI_0_RX_AVAIL_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	SPIO Receive Available SS Mask - Sensor Subsystem (INT_SS_SPI_0_RX_AVAIL_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	SPIO Receive Available Host Mask - Sensor Subsystem (INT_SS_SPI_0_RX_AVAIL_HOST_MASK)

Sensor Subsystem Interrupt Routing Mask 14 (INT_SS_SPI_0_TX_REQ_MASK)

MEM Offset (00000000)	438h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits



Default

0101_0101h

Table 457. Detailed Description of Sensor Subsystem Interrupt Routing Mask 14 (INT_SS_SPI_0_TX_REQ_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	SPIO Transmission Request SS Halt Mask - Sensor Subsystem (INT_SS_SPI_0_TX_REQ_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	SPIO Transmission Request Host Halt Mask - Sensor Subsystem (INT_SS_SPI_0_TX_REQ_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	SPIO Transmission Request SS Mask - Sensor Subsystem (INT_SS_SPI_0_TX_REQ_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	SPIO Transmission Request Host Mask - Sensor Subsystem (INT_SS_SPI_0_TX_REQ_HOST_MASK)

Sensor Subsystem Interrupt Routing Mask 15 (INT_SS_SPI_1_ERR_INT_MASK)

MEM Offset (00000000)	43Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 458. Detailed Description of Sensor Subsystem Interrupt Routing Mask 15 (INT_SS_SPI_1_ERR_INT_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	SPI1 Error SS Halt Mask - Sensor Subsystem (INT_SS_SPI_1_ERR_SS_HALT_INT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	SPI1 Error Host Halt Mask - Sensor Subsystem (INT_SS_SPI_1_ERR_HOST_HALT_INT_MASK)



Bits	Access Type	Default	Description
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	SPI1 Error SS Mask - Sensor Subsystem (INT_SS_SPI_1_ERR_SS_INT_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	SPI1 Error Host Mask - Sensor Subsystem (INT_SS_SPI_1_ERR_HOST_INT_MASK)

Sensor Subsystem Interrupt Routing Mask 16 (INT_SS_SPI_1_RX_AVAIL_MASK)

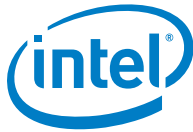
MEM Offset (00000000)	440h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 459. Detailed Description of Sensor Subsystem Interrupt Routing Mask 16 (INT_SS_SPI_1_RX_AVAIL_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	SPI1 Receive Available SS Halt Mask - Sensor Subsystem (INT_SS_SPI_1_RX_AVAIL_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	SPI1 Receive Available Host Halt Mask - Sensor Subsystem (INT_SS_SPI_1_RX_AVAIL_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	SPI1 Receive Available SS Mask - Sensor Subsystem (INT_SS_SPI_1_RX_AVAIL_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	SPI1 Receive Available Host Mask - Sensor Subsystem (INT_SS_SPI_1_RX_AVAIL_HOST_MASK)

Sensor Subsystem Interrupt Routing Mask 17 (INT_SS_SPI_1_TX_REQ_MASK)

MEM Offset (00000000)	444h
Security_PolicyGroup	



IntelRsvd False
Size 32 bits
Default 0101_0101h

Table 460. Detailed Description of Sensor Subsystem Interrupt Routing Mask 17 (INT_SS_SPI_1_TX_REQ_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	SPI1 Transmission Request SS Halt Mask - Sensor Subsystem (INT_SS_SPI_1_TX_REQ_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	SPI1 Transmission Request Host Halt Mask - Sensor Subsystem (INT_SS_SPI_1_TX_REQ_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	SPI1 Transmission Request SS Mask - Sensor Subsystem (INT_SS_SPI_1_TX_REQ_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	SPI1 Transmission Request Host Mask - Sensor Subsystem (INT_SS_SPI_1_TX_REQ_HOST_MASK)

Host Processor Interrupt Routing Mask 0 (INT_I2C_MST_0_MASK)

MEM Offset (00000000) 448h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0101_0101h

Table 461. Detailed Description of Host Processor Interrupt Routing Mask 0 (INT_I2C_MST_0_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	I2C Master 0 SS Halt interrupt mask (INT_I2C_MST_0_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
16	RW/P/L	1'b1	I2C Master 0 Host Halt interrupt mask (INT_I2C_MST_0_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	I2C Master 0 SS interrupt mask (INT_I2C_MST_0_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	I2C Master 0 Host interrupt mask (INT_I2C_MST_0_HOST_MASK)

Host Processor Interrupt Routing Mask 1 (INT_I2C_MST_1_MASK)

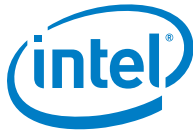
MEM Offset (00000000)	44Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 462. Detailed Description of Host Processor Interrupt Routing Mask 1 (INT_I2C_MST_1_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	I2C Master 1 SS Halt interrupt mask (INT_I2C_MST_1_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	I2C Master 1 Host Halt interrupt mask (INT_I2C_MST_1_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	I2C Master 1 SS interrupt mask (INT_I2C_MST_1_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	I2C Master 1 Host interrupt mask (INT_I2C_MST_1_HOST_MASK)

Host Processor Interrupt Routing Mask 2 (INT_SPI_MST_0_MASK)

MEM Offset (00000000)	454h
Security_PolicyGroup	



IntelRsvd False
Size 32 bits
Default 0101_0101h

Table 463. Detailed Description of Host Processor Interrupt Routing Mask 2 (INT_SPI_MST_0_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	SPI Master 0 Host interrupt mask (INT_SPI_MST_0_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	SPI Master 0 SS interrupt mask (INT_SPI_MST_0_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	SPI Master 0 Host Halt interrupt mask (INT_SPI_MST_0_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	SPI Master 0 SS Halt interrupt mask (INT_SPI_MST_0_HOST_MASK)

Host Processor Interrupt Routing Mask 3 (INT_SPI_MST_1_MASK)

MEM Offset (00000000) 458h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0101_0101h

Table 464. Detailed Description of Host Processor Interrupt Routing Mask 3 (INT_SPI_MST_1_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	SPI Master 1 Host interrupt mask (INT_SPI_MST_1_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	SPI Master 1 SS interrupt mask (INT_SPI_MST_1_HOST_HALT_MASK)



Bits	Access Type	Default	Description
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	SPI Master 1 Host Halt interrupt mask (INT_SPI_MST_1_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	SPI Master 1 SS Halt interrupt mask (INT_SPI_MST_1_HOST_MASK)

Host Processor Interrupt Routing Mask 4 (INT_SPI_SLV_MASK)

MEM Offset (00000000)	45Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 465. Detailed Description of Host Processor Interrupt Routing Mask 4 (INT_SPI_SLV_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	SPI Slave SS Halt interrupt mask (INT_SPI_SLV_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	SPI Slave Host Halt interrupt mask (INT_SPI_SLV_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	SPI Slave SS interrupt mask (INT_SPI_SLV_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	SPI Slave Host interrupt mask (INT_SPI_SLV_HOST_MASK)

Host Processor Interrupt Routing Mask 5 (INT_UART_0_MASK)

MEM Offset (00000000)	460h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits



Default

0101_0101h

Table 466. Detailed Description of Host Processor Interrupt Routing Mask 5 (INT_UART_0_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	UART0 SS Halt interrupt mask (INT_UART_0_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	UART0 Master Halt interrupt mask (INT_UART_0_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	UART0 SS interrupt mask (INT_UART_0_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	UART0 Master interrupt mask (INT_UART_0_HOST_MASK)

Host Processor Interrupt Routing Mask 6 (INT_UART_1_MASK)

MEM Offset (00000000)	464h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 467. Detailed Description of Host Processor Interrupt Routing Mask 6 (INT_UART_1_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	UART1 SS Halt interrupt mask (INT_UART_1_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	UART1 Master Halt interrupt mask (INT_UART_1_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
8	RW/P/L	1'b1	UART1 SS interrupt mask (INT_UART_1_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	UART1 Master interrupt mask (INT_UART_1_HOST_MASK)

Host Processor Interrupt Routing Mask 7 (INT_I2S_MASK)

MEM Offset (00000000)	468h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 468. Detailed Description of Host Processor Interrupt Routing Mask 7 (INT_I2S_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	I2S SS Halt interrupt mask (INT_I2S_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	I2S Host Halt interrupt mask (INT_I2S_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	I2S SS interrupt mask (INT_I2S_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	I2S Host interrupt mask (INT_I2S_HOST_MASK)

Host Processor Interrupt Routing Mask 8 (INT_GPIO_MASK)

MEM Offset (00000000)	46Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

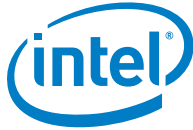


Table 469. Detailed Description of Host Processor Interrupt Routing Mask 8 (INT_GPIO_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	General Purpose I/O SS Halt interrupt Mask (INT_GPIO_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	General Purpose I/O Host Halt interrupt Mask (INT_GPIO_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	General Purpose I/O SS interrupt Mask (INT_GPIO_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	General Purpose I/O host interrupt Mask (INT_GPIO_HOST_MASK)

Host Processor Interrupt Routing Mask 9 (INT_PWM_TIMER_MASK)

MEM Offset (00000000)	470h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 470. Detailed Description of Host Processor Interrupt Routing Mask 9 (INT_PWM_TIMER_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	PWM Timer SS Halt interrupt mask (INT_PWM_TIMER_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	PWM Timer Host Halt interrupt mask (INT_PWM_TIMER_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
8	RW/P/L	1'b1	PWM Timer SS interrupt mask (INT_PWM_TIMER_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	PWM Timer Host interrupt mask (INT_PWM_TIMER_HOST_MASK)

Host Processor Interrupt Routing Mask 10 (INT_USB_MASK)

MEM Offset (00000000)	474h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 471. Detailed Description of Host Processor Interrupt Routing Mask 10 (INT_USB_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	USB SS Halt interrupt mask (INT_USB_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	USB Host Halt interrupt mask (INT_USB_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	USB SS interrupt mask (INT_USB_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	USB Host interrupt mask (INT_USB_HOST_MASK)

Host Processor Interrupt Routing Mask 11 (INT_RTC_MASK)

MEM Offset (00000000)	478h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

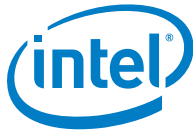


Table 472. Detailed Description of Host Processor Interrupt Routing Mask 11 (INT_RTC_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	RTC SS Halt interrupt mask (INT_RTC_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	RTC Host Halt interrupt mask (INT_RTC_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	RTC SS interrupt mask (INT_RTC_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	RTC Host interrupt mask (INT_RTC_HOST_MASK)

Host Processor Interrupt Routing Mask 12 (INT_WATCHDOG_MASK)

MEM Offset (00000000)	47Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 473. Detailed Description of Host Processor Interrupt Routing Mask 12 (INT_WATCHDOG_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	Watchdog SS Halt interrupt mask (INT_WATCHDOG_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	Watchdog Host Halt interrupt mask (INT_WATCHDOG_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	Watchdog SS interrupt mask (INT_WATCHDOG_SS_MASK)



Bits	Access Type	Default	Description
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	Watchdog Host interrupt mask (INT_WATCHDOG_HOST_MASK)

Host Processor Interrupt Routing Mask 13 (INT_DMA_CHANNEL_0_MASK)

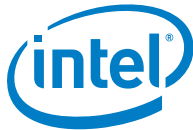
MEM Offset (00000000)	480h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 474. Detailed Description of Host Processor Interrupt Routing Mask 13 (INT_DMA_CHANNEL_0_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	DMA channel 0 SS Halt interrupt mask (INT_DMA_CHANNEL_0_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	DMA channel 0 Host Halt interrupt mask (INT_DMA_CHANNEL_0_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	DMA channel 0 SS interrupt mask (INT_DMA_CHANNEL_0_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	DMA channel 0 Host interrupt mask (INT_DMA_CHANNEL_0_HOST_MASK)

Host Processor Interrupt Routing Mask 14 (INT_DMA_CHANNEL_1_MASK)

MEM Offset (00000000)	484h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

**Table 475. Detailed Description of Host Processor Interrupt Routing Mask 14
(INT_DMA_CHANNEL_1_MASK)**

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	DMA channel 1 SS Halt interrupt mask (INT_DMA_CHANNEL_1_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	DMA channel 1 Host Halt interrupt mask (INT_DMA_CHANNEL_1_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	DMA channel 1 SS interrupt mask (INT_DMA_CHANNEL_1_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	DMA channel 1 Host interrupt mask (INT_DMA_CHANNEL_1_HOST_MASK)

Host Processor Interrupt Routing Mask 15 (INT_DMA_CHANNEL_2_MASK)

MEM Offset (00000000)	488h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

**Table 476. Detailed Description of Host Processor Interrupt Routing Mask 15
(INT_DMA_CHANNEL_2_MASK)**

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	DMA channel 2 SS Halt interrupt mask (INT_DMA_CHANNEL_2_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	DMA channel 2 Host Halt interrupt mask (INT_DMA_CHANNEL_2_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
8	RW/P/L	1'b1	DMA channel 2 SS interrupt mask (INT_DMA_CHANNEL_2_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	DMA channel 2 Host interrupt mask (INT_DMA_CHANNEL_2_HOST_MASK)

Host Processor Interrupt Routing Mask 16 (INT_DMA_CHANNEL_3_MASK)

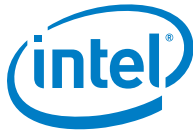
MEM Offset (00000000)	48Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 477. Detailed Description of Host Processor Interrupt Routing Mask 16 (INT_DMA_CHANNEL_3_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	DMA channel 3 SS Halt interrupt mask (INT_DMA_CHANNEL_3_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	DMA channel 3 Host Halt interrupt mask (INT_DMA_CHANNEL_3_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	DMA channel 3 SS interrupt mask (INT_DMA_CHANNEL_3_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	DMA channel 3 Host interrupt mask (INT_DMA_CHANNEL_3_HOST_MASK)

Host Processor Interrupt Routing Mask 17 (INT_DMA_CHANNEL_4_MASK)

MEM Offset (00000000)	490h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

**Table 478. Detailed Description of Host Processor Interrupt Routing Mask 17
(INT_DMA_CHANNEL_4_MASK)**

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	DMA channel 4 SS Halt interrupt mask (INT_DMA_CHANNEL_4_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	DMA channel 4 Host Halt interrupt mask (INT_DMA_CHANNEL_4_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	DMA channel 4 SS interrupt mask (INT_DMA_CHANNEL_4_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	DMA channel 4 Host interrupt mask (INT_DMA_CHANNEL_4_HOST_MASK)

Host Processor Interrupt Routing Mask 18 (INT_DMA_CHANNEL_5_MASK)

MEM Offset (00000000)	494h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

**Table 479. Detailed Description of Host Processor Interrupt Routing Mask 18
(INT_DMA_CHANNEL_5_MASK)**

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	DMA channel 5 SS Halt interrupt mask (INT_DMA_CHANNEL_5_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	DMA channel 5 Host Halt interrupt mask (INT_DMA_CHANNEL_5_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
8	RW/P/L	1'b1	DMA channel 5 SS interrupt mask (INT_DMA_CHANNEL_5_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	DMA channel 5 Host interrupt mask (INT_DMA_CHANNEL_5_HOST_MASK)

Host Processor Interrupt Routing Mask 19 (INT_DMA_CHANNEL_6_MASK)

MEM Offset (00000000)	498h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 480. Detailed Description of Host Processor Interrupt Routing Mask 19 (INT_DMA_CHANNEL_6_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	DMA channel 6 SS Halt interrupt mask (INT_DMA_CHANNEL_6_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	DMA channel 6 Host Halt interrupt mask (INT_DMA_CHANNEL_6_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	DMA channel 6 SS interrupt mask (INT_DMA_CHANNEL_6_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	DMA channel 6 Host interrupt mask (INT_DMA_CHANNEL_6_HOST_MASK)

Host Processor Interrupt Routing Mask 20 (INT_DMA_CHANNEL_7_MASK)

MEM Offset (00000000)	49Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

**Table 481. Detailed Description of Host Processor Interrupt Routing Mask 20 (INT_DMA_CHANNEL_7_MASK)**

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	DMA channel 7 SS Halt interrupt mask (INT_DMA_CHANNEL_7_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	DMA channel 7 Host Halt interrupt mask (INT_DMA_CHANNEL_7_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	DMA channel 7 SS interrupt mask (INT_DMA_CHANNEL_7_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	DMA channel 7 Host interrupt mask (INT_DMA_CHANNEL_7_HOST_MASK)

Host Processor Interrupt Routing Mask 21 (INT_MAILBOX_MASK)

MEM Offset (00000000)	4A0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	FFFF_FFFFh

Table 482. Detailed Description of Host Processor Interrupt Routing Mask 21 (INT_MAILBOX_MASK)

Bits	Access Type	Default	Description
31:24	RW/P/L	8'hff	Mailbox SS Halt interrupt mask - 8 bits (INT_MAILBOX_SS_HALT_MASK)
23:16	RW/P/L	8'hff	Mailbox Host Halt interrupt mask - 8 bits (INT_MAILBOX_HOST_HALT_MASK)
15:8	RW/P/L	8'hff	Mailbox SS interrupt mask - 8 bits (INT_MAILBOX_SS_MASK)
7:0	RW/P/L	8'hff	Mailbox Host interrupt mask - 8 bits (INT_MAILBOX_HOST_MASK)

Host Processor Interrupt Routing Mask 22 (INT_COMPARATORS_SS_HALT_MASK)

MEM Offset (00000000)	4A4h
Security_PolicyGroup	



IntelRsvd False
Size 32 bits
Default 0007_FFFFh

Table 483. Detailed Description of Host Processor Interrupt Routing Mask 22 (INT_COMPARATORS_SS_HALT_MASK)

Bits	Access Type	Default	Description
31:19	RO	13'h0000	RSVD (RSVD) Reserved
18:0	RW/P/L	19'h7fff	Comparators SS Halt interrupt mask (INT_COMPARATORS_SS_HALT_MASK)

Host Processor Interrupt Routing Mask 23 (INT_COMPARATORS_HOST_HALT_MASK)

MEM Offset (00000000) 4A8h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0007_FFFFh

Table 484. Detailed Description of Host Processor Interrupt Routing Mask 22 (INT_COMPARATORS_SS_HALT_MASK)

Bits	Access Type	Default	Description
31:19	RO	13'h0000	RSVD (RSVD) Reserved
18:0	RW/P/L	19'h7fff	Comparators Host Halt interrupt mask (INT_COMPARATORS_HOST_HALT_MASK)

Host Processor Interrupt Routing Mask 24 (INT_COMPARATORS_SS_MASK)

MEM Offset (00000000) 4ACh
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0007_FFFFh

Table 485. Detailed Description of Host Processor Interrupt Routing Mask 24 (INT_COMPARATORS_SS_MASK)

Bits	Access Type	Default	Description
31:19	RO	13'h0000	RSVD (RSVD) Reserved
18:0	RW/P/L	19'h7fff	Comparators SS interrupt mask (INT_COMPARATORS_SS_MASK)

**Host Processor Interrupt Routing Mask 25 (INT_COMPARATORS_HOST_MASK)**

MEM Offset (00000000) 4B0h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0007_FFFFh

Table 486. Detailed Description of Host Processor Interrupt Routing Mask 25 (INT_COMPARATORS_HOST_MASK)

Bits	Access Type	Default	Description
31:19	RO	13'h0000	RSVD (RSVD) Reserved
18:0	RW/P/L	19'h7ffff	Comparators Host interrupt mask (INT_COMPARATORS_HOST_MASK)

Host Processor Interrupt Routing Mask 26 (INT_HOST_BUS_ERR_MASK)

MEM Offset (00000000) 4B4h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0101_0101h

Table 487. Detailed Description of Host Processor Interrupt Routing Mask 26 (INT_HOST_BUS_ERR_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	Host Processor Bus Error SS Halt mask (INT_HOST_BUS_ERR_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	Host Processor Bus Error Host Halt mask (INT_HOST_BUS_ERR_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	Host Processor Bus Error SS mask (INT_HOST_BUS_ERR_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	Host Processor Bus Error Host mask (INT_HOST_BUS_ERR_HOST_MASK)



Host Processor Interrupt Routing Mask 27 (INT_DMA_ERROR_MASK)

MEM Offset (00000000)	4B8h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	FFFF_FFFFh

Table 488. Detailed Description of Host Processor Interrupt Routing Mask 27 (INT_DMA_ERROR_MASK)

Bits	Access Type	Default	Description
31:24	RW/P/L	8'hff	DMA Error SS Halt Mask - 8 bits (INT_DMA_ERROR_SS_HALT_MASK)
23:16	RW/P/L	8'hff	DMA Error Host Halt Mask - 8 bits (INT_DMA_ERROR_HOST_HALT_MASK)
15:8	RW/P/L	8'hff	DMA Error SS Mask - 8 bits (INT_DMA_ERROR_SS_MASK)
7:0	RW/P/L	8'hff	DMA Error Host Mask - 8 bits (INT_DMA_ERROR_HOST_MASK)

Host Processor Interrupt Routing Mask 28 (INT_SRAM_CONTROLLER_MASK)

MEM Offset (00000000)	4BCh
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 489. Detailed Description of Host Processor Interrupt Routing Mask 28 (INT_SRAM_CONTROLLER_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	SRAM Controller SS Halt mask (INT_SRAM_CONTROLLER_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	SRAM Controller Host Halt mask (INT_SRAM_CONTROLLER_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	SRAM Controller SS mask (INT_SRAM_CONTROLLER_SS_MASK)



Bits	Access Type	Default	Description
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	SRAM Controller Host mask (INT_SRAM_CONTROLLER_HOST_MASK)

Host Processor Interrupt Routing Mask 29 (INT_FLASH_CONTROLLER_0_MASK)

MEM Offset (00000000)	4C0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 490. Detailed Description of Host Processor Interrupt Routing Mask 29 (INT_FLASH_CONTROLLER_0_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	Flash Controller 0 SS Halt interrupt mask (INT_FLASH_CONTROLLER_0_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	Flash Controller 0 Host Halt interrupt mask (INT_FLASH_CONTROLLER_0_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	Flash Controller 0 SS interrupt mask (INT_FLASH_CONTROLLER_0_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	Flash Controller 0 Host interrupt mask (INT_FLASH_CONTROLLER_0_HOST_MASK)

Host Processor Interrupt Routing Mask 30 (INT_FLASH_CONTROLLER_1_MASK)

MEM Offset (00000000)	4C4h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h



Table 491. Detailed Description of Host Processor Interrupt Routing Mask 30 (INT_FLASH_CONTROLLER_1_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	Flash Controller 1 SS Halt interrupt mask (INT_FLASH_CONTROLLER_1_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	Flash Controller 1 Host Halt interrupt mask (INT_FLASH_CONTROLLER_1_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	Flash Controller 1 SS interrupt mask (INT_FLASH_CONTROLLER_1_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	Flash Controller 1 Host interrupt mask (INT_FLASH_CONTROLLER_1_HOST_MASK)

Host Processor Interrupt Routing Mask 31 (INT_AON_TIMER_MASK)

MEM Offset (00000000)	4C8h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 492. Detailed Description of Host Processor Interrupt Routing Mask 30 (INT_FLASH_CONTROLLER_1_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	Always-On Timer SS Halt Interrupt Mask (INT_AON_TIMER_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	Always-On Timer Host Halt Interrupt Mask (INT_AON_TIMER_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
8	RW/P/L	1'b1	Always-On Timer SS Interrupt Mask (INT_AON_TIMER_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	Always-On Timer Host Interrupt Mask (INT_AON_TIMER_HOST_MASK)

Host Processor Interrupt Routing Mask 32 (INT_ADC_PWR_MASK)

MEM Offset (00000000)	4CCh
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 493. Detailed Description of Host Processor Interrupt Routing Mask 32 (INT_ADC_PWR_MASK)

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	ADC Power int SS Halt Interrupt Mask (INT_ADC_PWR_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	ADC Power int Host Halt Interrupt Mask (INT_ADC_PWR_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	ADC Power int SS Interrupt Mask (INT_ADC_PWR_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	ADC Power int Host Interrupt Mask (INT_ADC_PWR_HOST_MASK)

Host Processor Interrupt Routing Mask 33 (INT_ADC_CALIB_MASK)

MEM Offset (00000000)	4D0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h



Table 494. Detailed Description of Host Processor Interrupt Routing Mask 33 (INT_ADC_CALIB_MASK)

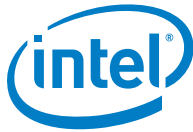
Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	ADC calib int SS Halt Interrupt Mask (INT_ADC_CALIB_SS_HALT_MASK)
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	ADC calib int Host Halt Interrupt Mask (INT_ADC_CALIB_HOST_HALT_MASK)
15:9	RO	7'h00	RSVD (RSVD) Reserved
8	RW/P/L	1'b1	ADC calib int SS Interrupt Mask (INT_ADC_CALIB_SS_MASK)
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	ADC calib int Host Interrupt Mask (INT_ADC_CALIB_HOST_MASK)

Host Processor Interrupt Routing Mask 34 (INT_GPIO_AON[MASK])

MEM Offset (00000000)	4D4h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0101_0101h

Table 495. Detailed Description of Host Processor Interrupt Routing Mask 34 (INT_GPIO_AON[MASK])

Bits	Access Type	Default	Description
31:25	RO	7'h00	RSVD (RSVD) Reserved
24	RW/P/L	1'b1	AON GPIO int SS Halt Interrupt Mask (INT_GPIO_AON[SS_HALT_MASK])
23:17	RO	7'h00	RSVD (RSVD) Reserved
16	RW/P/L	1'b1	AON GPIO int Host Halt Interrupt Mask (INT_GPIO_AON[HOST_HALT_MASK])
15:9	RO	7'h00	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
8	RW/P/L	1'b1	AON GPIO int SS Interrupt Mask (INT_GPIO_AON[SS_MASK])
7:1	RO	7'h00	RSVD (RSVD) Reserved
0	RW/P/L	1'b1	AON GPIO int Host Interrupt Mask (INT_GPIO_AON[HOST_MASK])

Interrupt Mask Lock (LOCK_INT_MASK_REG)

MEM Offset (00000000)	4D8h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 496. Detailed Description of Interrupt Mask Lock (LOCK_INT_MASK_REG)

Bits	Access Type	Default	Description	ResetSignal
31:4	RO	28'h0000000	RSVD (RSVD) Reserved	
3	RW/1S	1'b0	Lock All Sensor Processor Halt Mask Fields (LOCK_SS_HALT_MASK)	pwr_rst_n
2	RW/1S	1'b0	Lock All Host Processor Halt Mask Fields (LOCK_HOST_HALT_MASK)	pwr_rst_n
1	RW/1S	1'b0	Lock All Sensor Processor Interrupt Mask Fields (LOCK_SS_MASK)	pwr_rst_n
0	RW/1S	1'b0	Lock All Host Processor Interrupt Mask Fields (LOCK_HOST_MASK)	pwr_rst_n

Processor Level 2 (P_LVL2)

MEM Offset (00000000)	504h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 497. Detailed Description of Processor Level 2 (P_LVL2)

Bits	Access Type	Default	Description
31:8	RO	24'h000000	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
7:0	RO	8'h00	Go to C2 (GO_TO_C2) Reads to this register return all zeroes, writes have no effect. Reads to this register generate a C2 request.

Power Management 1 Control (PM1C)

MEM Offset (00000000)	518h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 498. Detailed Description of Processor Level 2 (P_LVL2)

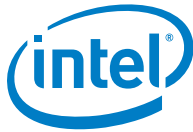
Bits	Access Type	Default	Description
31:14	RO	18'h00000	RSVD (RSVD) Reserved
13	WO	1'b0	Sleep Enable (SLPEN) Reads to this bit always return 0. Setting this bit causes the system to sequence into the Sleep state defined by SLPTYPE
12	RO	1'h0	RSVD (RSVD) Reserved
11:10	RW/P	2'b00	Sleep Type (SLPTYPE) Reserved
9:0	RO	10'h000	RSVD (RSVD) Reserved

AON Voltage Regulator (AON_VR)

MEM Offset (00000000)	540h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0090h

Table 499. Detailed Description of Processor Level 2 (P_LVL2)

Bits	Access Type	Default	Description
31:9	RO	23'h000000	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
8	RW/P/L	1'h0	High Impedance Mode (HIZ) This bit is used to put the regulator into High Impedance mode. HIZ has higher priority than EN. 0b : Normal Mode/Shutdown Mode (determined by EN) 1b : High Impedance Mode For REG_PLAT = 0 or 1, the default value of HIZ is 0b
7	RW/P/L	1'h1	Regulator Enable (EN) This bit is used to enable the regulators. When disabled, the regulators are in shutdown mode and the output is pulled to 0V. EN has lower priority than HIZ. 0b : Shutdown Mode 1b : Normal Mode For REG_PLAT = 0 or 1, the default value of EN is 1b
6	RO	1'h0	RSVD (RSVD) Reserved
5	RW/P/L	1'h0	Voltage Select Strobe (VSTRB) Enables output voltage programming using VSEL. The VSEL value is strobed only on a rising edge of VSTRB



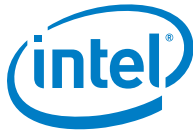
Bits	Access Type	Default	Description
4:0	RW/P/L	5'b10000	Voltage Select (VSEL) These control bits are used to program the output voltage in conjunction with VSTRB 01000b : 1.20V 01001b : 1.25V 01010b : 1.30V 01011b : 1.35V 01100b : 1.40V 01101b : 1.50V 01110b : 1.60V 01111b : 1.70V 10000b : 1.80V 10001b : 1.90V 10010b : 2.00V 10011b : 2.10V 10100b : 2.20V 10101b : 2.30V 10110b : 2.40V 10111b : 2.50V 11000b : 2.60V 11001b : 2.70V 11010b : 2.80V 11011b : 2.90V 11100b : 3.00V 11101b : 3.10V 11110b : 3.20V 11111b : 3.30V Values between 00000b and 00111b are illegal.

Platform 3P3 Voltage Regulator (PLAT3P3_VR)

MEM Offset (00000000)	544h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0001_881Fh

Table 500. Detailed Description of Processor Level 2 (P_LVL2)

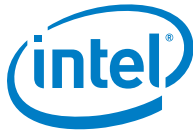
Bits	Access Type	Default	Description	ResetSignal
31:17	RO	15'h0000	RSVD (RSVD) Reserved	



Bits	Access Type	Default	Description	ResetSignal
16	RW/L	1'b1	Cold Reset Regulator Shutdown Enable (COLD_RST_SHDN_EN) Control bit to determine the cold reset behavior of regulator. When set, a cold reset will shutdown the regulator and wait for ROK to be de-asserted. This will cause a power cycle of any connected voltage rails. On exiting cold reset, the HIZ, EN and VREG_SEL register fields will be reset to default values based on REG_PLAT, regardless of setting of COLD_RST_REG_EN. When clear, a cold reset will not shutdown the regulator or power cycle any connected rails. 0b : Cold Reset Regulator Shutdown Disabled 1b : Cold Reset Regulator Shutdown Enabled	por_rst_n
15	RW/L	1'b1	Cold Reset Register Reset Enable (COLD_RST_REG_EN) Control bit to determine the cold reset behavior of HIZ, EN and VREG_SEL register fields. When set, a cold reset will reset HIZ, EN and VREG_SEL to default values based on REG_PLAT. When clear, a cold reset will have no effect on the current value of HIZ, EN and VREG_SEL. This allows the state of the regulator to be preserved during a cold reset. 0b : Cold Reset Register Reset Disabled 1b : Cold Reset Register Reset Enabled	por_rst_n
14	RO/V	1'b0	Low Temperature Flag (LOWT) Status bit indicating that the switching regulator junction temperature is below threshold level specified by LTSEL. The status bit is set when the temperature falls below the threshold level but the regulator will remain in regulation. The status bit is cleared when the temperature has increased by at least one step of LTSEL threshold 0b : Switching Regulator Junction Temperature Above LTSEL 1b : Switching Regulator Junction Temperature Below LTSEL	
13:12	RW/P	2'b00	Control (CTRL) Control bits for Switching Regulator CTRL input. Currently unused and not connected to Switching Regulator.	



Bits	Access Type	Default	Description	ResetSignal
11	RW/L	1'h1	Regulator OK Mask (ROKM) Mask bit used for debug purposes. When set to 1, the ROK signal from the switching regulator is masked and seen as a 1 by internal logic looking for ROK to be asserted. When set to 0, this bit has no effect. 0b : ROK Not Masked 1b : ROK Masked	por_rst_n
10	RO/V	1'h0	Regulator OK (ROK) Status bit indicating that the switching regulator has completed start-up and is regulating properly. ROK is de-asserted when proper regulation cannot be maintained or when the current limit is reached. ROK is also de-asserted when the switching regulator is placed into High Impedance Mode. 0b : Switching Regulator out of regulation 1b : Switching Regulator in regulation	
9	RW/P/L	1'h0	Force PWM Mode (FRC_PWM) Control bit to force switching regulator into PWM mode at low load. At low loads, the switching regulator enters PFM mode to maintain efficiency. Setting this bit, forces the switching regulator to remain in PWM mode regardless of the current load. 0b : Allow Regulator to switch between PWM Mode and PFM Mode based on current load 1b : Force Regulator to remain in PWM Mode	
8	RW/V/L	1'h0	High Impedance Mode (HIZ) This bit is used to put the regulators into High Impedance mode. HIZ has higher priority than EN. 0b : Normal Mode/Shutdown Mode (determined by EN) 1b : High Impedance Mode For REG_PLAT = 0, the default value of HIZ is 0b For REG_PLAT = 1, the default value of HIZ is 1b	por_rst_n



Bits	Access Type	Default	Description	ResetSignal
7	RW/V/L	1'h0	Regulator Enable (EN) This bit is used to enable the regulators. When disabled, the regulators are in shutdown mode and the output is pulled to 0V. EN has lower priority than HIZ. 0b : Shutdown Mode 1b : Normal Mode For REG_PLAT = 0, the default value of EN is 1b For REG_PLAT = 1, the default value of EN is 0b	por_rst_n
6	RW/V/L	1'h0	Voltage Regulator Select (VREG_SEL) Control bit to select between low quiescent current linear regulator and buck switching inductor regulator. 0b : Switching Regulator 1b : Linear Regulator	por_rst_n
5	RW/P/L	1'h0	Voltage Select Strobe (VSTRB) Enables output voltage programming using VSEL. The VSEL value is strobed only on a rising edge of VSTRB	



Bits	Access Type	Default	Description	ResetSignal
4:0	RW/P/L	5'b11111	Voltage Select (VSEL) These control bits are used to program the output voltage in conjunction with VSTRB 00000b : 0.80V (Switching Regulator Only) 00001b : 0.85V (Switching Regulator Only) 00010b : 0.90V (Switching Regulator Only) 00011b : 0.95V (Switching Regulator Only) 00100b : 1.00V (Switching Regulator Only) 00101b : 1.05V (Switching Regulator Only) 00110b : 1.10V (Switching Regulator Only) 00111b : 1.15V (Switching Regulator Only) 01000b : 1.20V 01001b : 1.25V 01010b : 1.30V 01011b : 1.35V 01100b : 1.40V 01101b : 1.50V 01110b : 1.60V 01111b : 1.70V 10000b : 1.80V 10001b : 1.90V 10010b : 2.00V 10011b : 2.10V 10100b : 2.20V 10101b : 2.30V 10110b : 2.40V 10111b : 2.50V 11000b : 2.60V 11001b : 2.70V 11010b : 2.80V 11011b : 2.90V 11100b : 3.00V 11101b : 3.10V 11110b : 3.20V 11111b : 3.30V	

Platform 1P8 Voltage Regulator (PLAT1P8_VR)

MEM Offset (00000000)	548h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0001_8810h

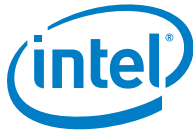
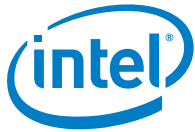


Table 501. Detailed Description of Platform 1P8 Voltage Regulator (PLAT1P8_VR)

Bits	Access Type	Default	Description	ResetSignal
31:17	RO	15'h0000	RSVD (RSVD) Reserved	
16	RW/L	1'b1	Cold Reset Regulator Shutdown Enable (COLD_RST_SHDN_EN) Control bit to determine the cold reset behavior of regulator. When set, a cold reset will shutdown the regulator and wait for ROK to be de-asserted. This will cause a power cycle of any connected voltage rails. On exiting cold reset, the HIZ, EN and VREG_SEL register fields will be reset to default values based on REG_PLAT, regardless of setting of COLD_RST_REG_EN. When clear, a cold reset will not shutdown the regulator or power cycle any connected rails. 0b : Cold Reset Regulator Shutdown Disabled 1b : Cold Reset Regulator Shutdown Enabled	por_rst_n
15	RW/L	1'b1	Cold Reset Register Reset Enable (COLD_RST_REG_EN) Control bit to determine the cold reset behavior of HIZ, EN and VREG_SEL register fields. When set, a cold reset will reset HIZ, EN and VREG_SEL to default values based on REG_PLAT. When clear, a cold reset will have no effect on the current value of HIZ, EN and VREG_SEL. This allows the state of the regulator to be preserved during a cold reset. 0b : Cold Reset Register Reset Disabled 1b : Cold Reset Register Reset Enabled	por_rst_n
14	RO/V	1'b0	Low Temperature Flag (LOWT) Status bit indicating that the switching regulator junction temperature is below threshold level specified by LTSEL. The status bit is set when the temperature falls below the threshold level but the regulator will remain in regulation. The status bit is cleared when the temperature has increased by at least one step of LTSEL threshold 0b : Switching Regulator Junction Temperature Above LTSEL 1b : Switching Regulator Junction Temperature Below LTSEL	



Bits	Access Type	Default	Description	ResetSignal
13:12	RW/P	2'b00	Control (CTRL) Control bits for Switching Regulator CTRL input. Currently unused and not connected to Switching Regulator.	
11	RW/L	1'b1	Regulator OK Mask (ROKM) Mask bit used for debug purposes. When set to 1, the ROK signal from regulator is masked and seen as a 1 by internal logic looking for ROK to be asserted. When set to 0, this bit has no effect. 0b : ROK Not Masked 1b : ROK Masked	por_rst_n
10	RO/V	1'b0	Regulator OK (ROK) Status bit indicating that the switching regulator has completed start-up and is regulating properly. ROK is de-asserted when proper regulation cannot be maintained or when the current limit is reached. ROK is also de-asserted when the switching regulator is placed into High Impedance Mode. 0b : Switching Regulator out of regulation 1b : Switching Regulator in regulation	
9	RW/P/L	1'b0	Force PWM Mode (FRC_PWM) Control bit to force switching regulator into PWM mode at low load. At low loads, the switching regulator enters PFM mode to maintain efficiency. Setting this bit, forces the switching regulator to remain in PWM mode regardless of the current load. 0b : Allow Regulator to switch between PWM Mode and PFM Mode based on current load 1b : Force Regulator to remain in PWM Mode	
8	RW/V/L	1'b0	High Impedance Mode (HIZ) This bit is used to put the regulators into High Impedance mode. HIZ has higher priority than EN. 0b : Normal Mode/Shutdown Mode (determined by EN) 1b : High Impedance Mode For REG_PLAT = 0, the default value of HIZ is 0b For REG_PLAT = 1, the default value of HIZ is 1b	por_rst_n



Bits	Access Type	Default	Description	ResetSignal
7	RW/V/L	1'b0	Regulator Enable (EN) This bit is used to enable the regulators. When disabled, the regulators are in shutdown mode and the output is pulled to 0V. EN has lower priority than HIZ. 0b : Shutdown Mode 1b : Normal Mode For REG_PLAT = 0, the default value of EN is 1b For REG_PLAT = 1, the default value of EN is 0b	por_rst_n
6	RW/V/L	1'h0	Voltage Regulator Select (VREG_SEL) Control bit to select between low quiescent current linear regulator and buck switching inductor regulator. 0b : Switching Regulator 1b : Linear Regulator	por_rst_n
5	RW/P/L	1'h0	Voltage Select Strobe (VSTRB) Enables output voltage programming using VSEL. The VSEL value is strobed only on a rising edge of VSTRB	



Bits	Access Type	Default	Description	ResetSignal
4:0	RW/P/L	5'b10000	Voltage Select (VSEL) These control bits are used to program the output voltage in conjunction with VSTRB 00000b : 0.80V (Switching Regulator Only) 00001b : 0.85V (Switching Regulator Only) 00010b : 0.90V (Switching Regulator Only) 00011b : 0.95V (Switching Regulator Only) 00100b : 1.00V (Switching Regulator Only) 00101b : 1.05V (Switching Regulator Only) 00110b : 1.10V (Switching Regulator Only) 00111b : 1.15V (Switching Regulator Only) 01000b : 1.20V 01001b : 1.25V 01010b : 1.30V 01011b : 1.35V 01100b : 1.40V 01101b : 1.50V 01110b : 1.60V 01111b : 1.70V 10000b : 1.80V 10001b : 1.90V 10010b : 2.00V 10011b : 2.10V 10100b : 2.20V 10101b : 2.30V 10110b : 2.40V 10111b : 2.50V 11000b : 2.60V 11001b : 2.70V 11010b : 2.80V 11011b : 2.90V 11100b : 3.00V 11101b : 3.10V 11110b : 3.20V 11111b : 3.30V	

Host Voltage Regulator (HOST_VR)

MEM Offset (00000000)	54Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0810h

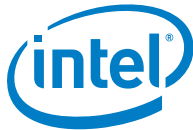
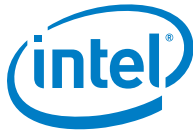


Table 502. Detailed Description of Platform 1P8 Voltage Regulator (PLAT1P8_VR)

Bits	Access Type	Default	Description	ResetSignal
31:15	RO	17'h00000	RSVD (RSVD) Reserved	
14	RO/V	1'b0	Low Temperature Flag (LOWT) Status bit indicating that the switching regulator junction temperature is below threshold level specified by LTSEL. The status bit is set when the temperature falls below the threshold level but the regulator will remain in regulation. The status bit is cleared when the temperature has increased by at least one step of LTSEL threshold 0b : Switching Regulator Junction Temperature Above LTSEL 1b : Switching Regulator Junction Temperature Below LTSEL	
13:12	RW/P	2'b00	Control (CTRL) Control bits for Switching Regulator CTRL input. Currently unused and not connected to Switching Regulator.	
11	RW/L	1'b1	Regulator OK Mask (ROKM) Mask bit used for debug purposes. When set to 1, the ROK signal from regulator is masked and seen as a 1 by internal logic looking for ROK to be asserted. When set to 0, this bit has no effect. 0b : ROK Not Masked 1b : ROK Masked	por_rst_n
10	RO/V	1'b0	Regulator OK (ROK) Status bit indicating that the switching regulator has completed start-up and is regulating properly. ROK is de-asserted when proper regulation cannot be maintained or when the current limit is reached. ROK is also de-asserted when the switching regulator is placed into High Impedance Mode. 0b : Switching Regulator out of regulation 1b : Switching Regulator in regulation	



Bits	Access Type	Default	Description	ResetSignal
9	RW/P/L	1'b0	Force PWM Mode (FRC_PWM) Control bit to force switching regulator into PWM mode at low load. At low loads, the switching regulator enters PFM mode to maintain efficiency. Setting this bit, forces the switching regulator to remain in PWM mode regardless of the current load. 0b : Allow Regulator to switch between PWM Mode and PFM Mode based on current load 1b : Force Regulator to remain in PWM Mode	
8	RW/V/L	1'b0	High Impedance Mode (HIZ) This bit is used to put the regulators into High Impedance mode. HIZ has higher priority than EN. 0b : Normal Mode/Shutdown Mode (determined by EN) 1b : High Impedance Mode For REG_PLAT = 0, the default value of HIZ is 0b For REG_PLAT = 1, the default value of HIZ is 1b	por_rst_n
7	RW/V/L	1'b0	Regulator Enable (EN) This bit is used to enable the regulators. When disabled, the regulators are in shutdown mode and the output is pulled to 0V. EN has lower priority than HIZ. 0b : Shutdown Mode 1b : Normal Mode For REG_PLAT = 0, the default value of EN is 1b For REG_PLAT = 1, the default value of EN is 0b	por_rst_n
6	RW/P	1'h0	Voltage Regulator Select (VREG_SEL) Control bit to select between low quiescent current linear regulator and buck switching inductor regulator. 0b : Switching Regulator 1b : Linear Regulator	
5	RW/P/L	1'h0	Voltage Select Strobe (VSTRB) Enables output voltage programming using VSEL. The VSEL value is strobed only on a rising edge of VSTRB	



Bits	Access Type	Default	Description	ResetSignal
4:0	RW/P/L	5'b10000	Voltage Select (VSEL) These control bits are used to program the output voltage in conjunction with VSTRB 00000b : 0.80V (Switching Regulator Only) 00001b : 0.85V (Switching Regulator Only) 00010b : 0.90V (Switching Regulator Only) 00011b : 0.95V (Switching Regulator Only) 00100b : 1.00V (Switching Regulator Only) 00101b : 1.05V (Switching Regulator Only) 00110b : 1.10V (Switching Regulator Only) 00111b : 1.15V (Switching Regulator Only) 01000b : 1.20V 01001b : 1.25V 01010b : 1.30V 01011b : 1.35V 01100b : 1.40V 01101b : 1.50V 01110b : 1.60V 01111b : 1.70V 10000b : 1.80V 10001b : 1.90V 10010b : 2.00V 10011b : 2.10V 10100b : 2.20V 10101b : 2.30V 10110b : 2.40V 10111b : 2.50V 11000b : 2.60V 11001b : 2.70V 11010b : 2.80V 11011b : 2.90V 11100b : 3.00V 11101b : 3.10V 11110b : 3.20V 11111b : 3.30V	

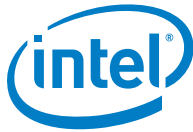
Sleeping Configuration (SLP_CFG)

MEM Offset (00000000)	550h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_000Bh



Table 503. Detailed Description of Sleeping Configuration (SLP_CFG)

Bits	Access Type	Default	Description
31:11	RO	21'h000000	RSVD (RSVD) Reserved
10	RW/1C/V/P	1'h0	IO State Retention Hold (IO_STATE_RET_HOLD) This status bit indicates when the value of the microcontroller's outputs are being held due to entering the Sleep state with IO State Retention enabled. This bit is set automatically by hardware once the outputs have been placed in the hold state. It is the responsibility of software to release the outputs from the hold state by writing a 1 to this bit. 0b : IO State Retention Release 1b : IO State Retention Hold
9	RW/P/L	1'h0	IO State Retention Enable (IO_STATE_RET_EN) When enabled, the state of any IO configured as an output will be sampled before entry to Sleep state and held constant. This allows the output state to be retained during Sleep. 0b : IO State Retention Disabled 1b : IO State Retention Enabled
8	RW/P/L	1'h0	OPM Low Power Mode Enable (LPMODE_EN) This bit determines if the OPM is placed into low power mode when Sleep state is entered. This bit should only be set if all switching regulators are powered down or in High Impedance mode prior to Sleep Entry. 0b : Normal Mode during Sleep 1b : Low Power Mode during Sleep
7	RW/P/L	1'h0	RTC Disable (RTC_DIS) This bit determines if the RTC Oscillator is disabled when Sleep state is entered. 0b : RTC Enabled during Sleep State 1b : RTC Disabled during Sleep State
6	RO	1'h0	RSVD (RSVD) Reserved
5	RW/P/L	1'h0	AON Retention Voltage Enable (VRET_EN) Reserved



Bits	Access Type	Default	Description
4:0	RW/P/L	5'b01011	AON Retention Voltage Selection (VRET_SEL) Reserved

Power Management Network (PMNet) Control and Status (PMNETCS)

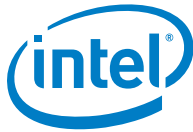
MEM Offset (00000000) 554h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 1000_001Ch

Table 504. Detailed Description of Power Management Network (PMNet) Control and Status (PMNETCS)

Bits	Access Type	Default	Description
31:30	RO	2'h0	RSVD (RSVD) Reserved
29	RO/V	1'b0	OPM Reference Voltage Output Valid (VREF_OUT_OK) Status bit indicating that VREF_OUT has reached 90% of its value. 0b : Reference Voltage Output Invalid 1b : Reference Voltage Output Valid
28	RW/P/L	1'b1	OPM Reference Voltage Output Enable (VREF_OUT_EN) When enabled, the OPM module provides a buffered reference voltage. When disabled, the reference voltage output is grounded and current consumption is reduced. 0b : Voltage Reference Disabled 1b : Voltage Reference Enabled
27	RO/V	1'b0	ACU Ready (ACU_RDY) Status bit indicating ACU has completed PMNet start-up sequence. 0b : Start Up Sequence in progress 1b : Start Up Sequence complete
26	RO/V	1'h0	Platform Regulator Start-Up Sequence Select (REG_PLAT) Status bit indicating value of REG_PLAT input. REG_PLAT is used to select the start-up sequence used by the ACU. 0b : Internal Regulator Start-Up Sequence Selected 1b : External Regulator Start-Up Sequence Selected



Bits	Access Type	Default	Description
25	RO	1'h0	RSVD (RSVD) Reserved
24	RO/V	1'h0	OPM Low Power Mode Status (LPMODE_OPM) Status bit indicating current OPM mode. 0b : Normal Mode 1b : Low Power Mode
23:20	RO	4'b0000	Spare Status (SPARE_STS) Spare PMNet status bits. Currently unused
19:16	RW/P	4'b0000	Spare Control (SPARE_CTRL) Spare PMNet control bits. Currently unused
15:7	RO	9'h000	RSVD (RSVD) Reserved
6	RW/P/L	1'h0	AVD_OPM Brownout Cold Reset Enable (BOR_VOPM_RST_EN) This bit controls whether or not a cold reset is performed due to the assertion of BOR_VOPM. If enabled, a power cycle of all active switching regulators will be performed as part of the cold reset. 0b : BOR_VOPM Cold Reset Disabled 1b : BOR_VOPM Cold Reset Enabled
5	RO/V	1'h0	AVD_OPM Brownout (BOR_VOPM) Status bit indicating current value of BOR_VOPM signal. BOR_VOPM indicates when the AVD_OPM output voltage has dropped below the OPMBOR threshold. When a brownout on AVD_OPM occurs, the operation of the switching regulators is no longer reliable and requires re-initialization. 0b : AVD_OPM above OPMBOR threshold (default value) 1b : AVD_OPM below OPMBOR threshold



Bits	Access Type	Default	Description
4:2	RW/P/L	3'b111	High Temperature Threshold (HTSEL) If the switching regulator junction temperature rises above the high temperature threshold, the regulator will terminate regulation, de-assert the ROK signal, and turn the power switches off (output is high impedance) until the temperature has dropped by at least one step of temperature, at which moment the regulator will resume normal operation. 000b : 100 degrees Celsius 001b : 105 degrees Celsius 010b : 110 degrees Celsius 011b : 115 degrees Celsius 100b : 120 degrees Celsius 101b : 125 degrees Celsius 110b : 135 degrees Celsius 111b : 150 degrees Celsius
1:0	RW/P/L	2'b00	Low Temperature Threshold (LTSEL) If the switching regulator junction temperature falls below the low temperature threshold, the regulator asserts the LOWT warning signal while the regulator remains in regulation. The warning signal is de-asserted when the temperature has increased by at least one step of temperature. 00b : -40 degrees Celsius 01b : -30 degrees Celsius 10b : -20 degrees Celsius 11b : -10 degrees Celsius

Power Management Wait (PM_WAIT)

MEM Offset (00000000)	558h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	00FF_00FFh



Table 505. Detailed Description of Power Management Wait (PM_WAIT)

Bits	Access Type	Default	Description	ResetSignal
31:16	RW/L	16'h00FF	Cold Reset Wait Duration (COLD_RST_WAIT) Determines the number of clock cycles the hardware state machine waits after performing a cold reset. When a cold reset occurs, this field allows time for the any power cycled voltage rails to discharge reached before the AON domain is released from cold reset. The delay is added by loading a counter that runs off a 32.768 kHz clock and then waiting for the counter to expire. 0000h : Wait 0 Clock Cycles 0001h : Wait 1 Clock Cycle 0002h : Wait 2 Clock Cycles FFFEh : Wait 65,534 Clock Cycles FFFFh : Wait 65,535 Clock Cycles	por_rst_n
15:0	RW/L	16'h00FF	Voltage Strobe Wait Duration (VSTRB_WAIT) Determines the number of clock cycles the hardware state machine waits after using voltage strobe to program a new output voltage for the AON regulator. When the voltage value is changed, this field allows time for the new voltage level to be reached before the AON domain is released from reset. The delay is added by loading a counter that runs off a 32.768 kHz clock and then waiting for the counter to expire. 0000h : Wait 0 Clock Cycles 0001h : Wait 1 Clock Cycle 0002h : Wait 2 Clock Cycles FFFEh : Wait 65,534 Clock Cycles FFFFh : Wait 65,535 Clock Cycles	por_rst_n

Processor Status (P_STS)

MEM Offset (00000000)	560h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 506. Detailed Description of Processor Status (P_STS)

Bits	Access Type	Default	Description
31:27	RO	5'h00	RSVD (RSVD) Reserved
26	RW/P/L	1'h0	Halt Interrupt Redirection (HALT_INT_REDIR) When an enabled host halt interrupt occurs, this bit determines if the interrupt event triggers a warm reset or an entry into Probe Mode. 0b : Warm Reset 1b : Probe Mode Entry
25:4	RO	22'h000000	RSVD (RSVD) Reserved
3	RW/1C/V/P	1'h0	Processor Bus Error (BUS_ERR) Status bit indicating that an error response has been observed on the processor bus. 0b : No Bus Error Response Observed 1b : Bus Error Response Observed
2	RW/1C/V/P	1'h0	Processor Shutdown (SHDWN) Status bit indicating the processor has issued a Shutdown special cycle. A Shutdown special cycle is generated when the processor incurs a triple fault. The processor remains in Shutdown mode until it is reset. This bit is set when the Shutdown special cycle is issued and can only be cleared by software. 0b : No Shutdown Special Cycle Issued 1b : Shutdown Special Cycle Issued
1	RO/V	1'h0	Processor Stop Grant (STP_GNT) Status bit indicating the processor has entered the Stop Grant state. When STPCLK# is asserted, the processor transitions to the C2/Stop Grant state. 0b : Processor not in Stop Grant State 1b : Processor in Stop Grant State
0	RO/V	1'h0	Processor Halt (HLT) Status bit indicating the processor has entered the Halt state. When a HLT instruction is executed, the processor transitions to the C1/Halt state. 0b : Processor not in Halt State 1b : Processor in Halt State



Reset Control (RSTC)

A write to this register with RSTC.COLD or RSTC.WARM set initiates a reset. Software must only write to one of these bits at a time, else the behavior is undefined. These bits automatically clear once the reset occurs, so there is no need for software to clear them.

MEM Offset (00000000) 570h
 Security_PolicyGroup
 IntelRsvd False
 Size 32 bits
 Default 0000_0000h

Table 507. Detailed Description of Reset Control (RSTC)

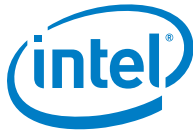
Bits	Access Type	Default	Description
31:4	RO	28'h0000000	RSVD (RSVD) Reserved
3	RW/P	1'h0	Cold Reset (COLD) When this bit is set, the microcontroller performs a cold reset.
2	RO	1'h0	RSVD (RSVD) Reserved
1	RW	1'h0	Warm Reset (WARM) When this bit is set, the mic performs a warm reset.
0	RO	1'h0	RSVD (RSVD) Reserved

Reset Status (RSTS)

MEM Offset (00000000) 574h
 Security_PolicyGroup
 IntelRsvd False
 Size 32 bits
 Default 0000_0000h

Table 508. Detailed Description of Reset Status (RSTS)

Bits	Access Type	Default	Description
31:5	RO	27'h0000000	RSVD (RSVD) Reserved
4	RW/1C/V/P	1'h0	Sensor Subsystem Halt Interrupt Triggered Warm Reset (SS_HALT_WRST) When this bit is set, it indicates that an enabled Sensor Subsystem Halt interrupt triggered a warm reset.



Bits	Access Type	Default	Description
3	RW/1C/V/P	1'h0	Host Processor Halt Interrupt Triggered Warm Reset (HOST_HALT_WRST) When this bit is set, it indicates that an enabled Host Halt interrupt triggered a warm reset.
2	RW/1C/V/P	1'h0	Sensor Subsystem Watchdog Timer Triggered Warm Reset (SS_WDG_WRST) When this bit is set, it indicates that Watchdog Timer in the Sensor Subsystem triggered a warm reset.
1	RW/1C/V/P	1'h0	Watchdog Timer Triggered Warm Reset (WDG_WRST) When this bit is set, it indicates that Watchdog Timer in the Peripheral block triggered a warm reset.
0	RW/1C/V/P	1'h0	Software Initiated Warm Reset (SW_WRST) When this bit is set, it indicates that warm reset was initiated by software writing to RSTC.WARM.

Voltage Regulator Lock (VR_LOCK)

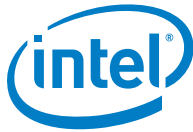
MEM Offset (00000000)	590h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 509. Detailed Description of Voltage Regulator Lock (VR_LOCK)

Bits	Access Type	Default	Description	ResetSignal
31:30	RO	2'h0	RSVD (RSVD) Reserved	
29	RW/1S	1'h0	Host VR Regulator OK Mask Lock (HOST_VR_ROKM_LOCK) Lock bit for HOST_VR.ROKM 0b : Unlocked 1b : Locked	pwr_rst_n
28	RW/1S	1'h0	Host VR Force PWM Mode Lock (HOST_VR_FRC_PWM_LOCK) Lock bit for HOST_VR.FRC_PWM 0b : Unlocked 1b : Locked	pwr_rst_n



Bits	Access Type	Default	Description	ResetSignal
27	RW/1S	1'h0	Host VR High Impedance Mode Lock (HOST_VR_HIZ_LOCK) Lock bit for HOST_VR.HIZ 0b : Unlocked 1b : Locked	pwr_rst_n
26	RW/1S	1'h0	Host Regulator Enable Lock (HOST_VR_EN_LOCK) Lock bit for HOST_VR.EN 0b : Unlocked 1b : Locked	pwr_rst_n
25	RW/1S	1'h0	Host VR Voltage Regulator Select Lock (HOST_VR_VREG_SEL_LOCK) Lock bit for HOST_VR.VREG_SEL 0b : Unlocked 1b : Locked	pwr_rst_n
24	RW/1S	1'h0	Host VR Voltage Select Lock (HOST_VR_VSEL_LOCK) Lock bit for HOST_VR.VSTRB and HOST_VR.SEL 0b : Unlocked 1b : Locked	pwr_rst_n
23	RO	1'h0	RSVD (RSVD) Reserved	
22	RW/1S	1'h0	Platform 1P8 VR Cold Reset Control Lock (PLAT1P8_VR_COLD_RST_LOCK) Lock bit for PLAT1P8_VR.COLD_RST_SHDN_EN and PLAT1P8_VR.COLD_RST_REG_EN 0b : Unlocked 1b : Locked	pwr_rst_n
21	RW/1S	1'h0	Platform 1P8 VR Regulator OK Mask Lock (PLAT1P8_VR_ROKM_LOCK) Lock bit for PLAT1P8_VR.ROKM 0b : Unlocked 1b : Locked	pwr_rst_n
20	RW/1S	1'h0	Platform 1P8 VR Force PWM Mode Lock (PLAT1P8_VR_FRC_PWM_LOCK) Lock bit for PLAT1P8_VR.FRC_PWM 0b : Unlocked 1b : Locked	pwr_rst_n
19	RW/1S	1'h0	Platform 1P8 VR High Impedance Mode Lock (PLAT1P8_VR_HIZ_LOCK) Lock bit for PLAT1P8_VR.HIZ 0b : Unlocked 1b : Locked	pwr_rst_n



Bits	Access Type	Default	Description	ResetSignal
18	RW/1S	1'h0	Platform 1P8 VR Regulator Enable Lock (PLAT1P8_VR_EN_LOCK) Lock bit for PLAT1P8_VR.EN 0b : Unlocked 1b : Locked	pwr_rst_n
17	RW/1S	1'h0	Platform 1P8 VR Voltage Regulator Select Lock (PLAT1P8_VR_VREG_SEL_LOCK) Lock bit for PLAT1P8_VR.VREG_SEL 0b : Unlocked 1b : Locked	pwr_rst_n
16	RW/1S	1'h0	Platform 1P8 VR Voltage Select Lock (PLAT1P8_VR_VSEL_LOCK) Lock bit for PLAT1P8_VR.VSTRB and PLAT1P8_VR.SEL 0b : Unlocked 1b : Locked	pwr_rst_n
15	RO	1'h0	RSVD (RSVD) Reserved	
14	RW/1S	1'h0	Platform 3P3 VR Cold Reset Control Lock (PLAT3P3_VR_COLD_RST_LOCK) Lock bit for PLAT3P3_VR.COLD_RST_SHDN_EN and PLAT3P3_VR.COLD_RST_REG_EN 0b : Unlocked 1b : Locked	pwr_rst_n
13	RW/1S	1'h0	Platform 3P3 VR Regulator OK Mask Lock (PLAT3P3_VR_ROKM_LOCK) Lock bit for PLAT3P3_VR.ROKM 0b : Unlocked 1b : Locked	pwr_rst_n
12	RW/1S	1'h0	Platform 3P3 VR Force PWM Mode Lock (PLAT3P3_VR_FRC_PWM_LOCK) Lock bit for PLAT3P3_VR.FRC_PWM 0b : Unlocked 1b : Locked	pwr_rst_n
11	RW/1S	1'h0	Platform 3P3 VR High Impedance Mode Lock (PLAT3P3_VR_HIZ_LOCK) Lock bit for PLAT3P3_VR.HIZ 0b : Unlocked 1b : Locked	pwr_rst_n
10	RW/1S	1'h0	Platform 3P3 VR Regulator Enable Lock (PLAT3P3_VR_EN_LOCK) Lock bit for PLAT3P3_VR.EN 0b : Unlocked 1b : Locked	pwr_rst_n



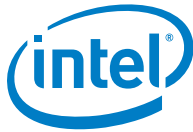
Bits	Access Type	Default	Description	ResetSignal
9	RW/1S	1'h0	Platform 3P3 VR Voltage Regulator Select Lock (PLAT3P3_VR_VREG_SEL_LOCK) Lock bit for PLAT3P3_VR.VREG_SEL 0b : Unlocked 1b : Locked	pwr_rst_n
8	RW/1S	1'h0	Platform 3P3 VR Voltage Select Lock (PLAT3P3_VR_VSEL_LOCK) Lock bit for PLAT3P3_VR.VSTRB and PLAT3P3_VR.SEL 0b : Unlocked 1b : Locked	pwr_rst_n
7:4	RO	4'h0	RSVD (RSVD) Reserved	
3	RW/1S	1'h0	AON VR High Impedance Mode Lock (AON_VR_HIZ_LOCK) Lock bit for AON_VR.HIZ 0b : Unlocked 1b : Locked	pwr_rst_n
2	RW/1S	1'h0	AON VR Regulator Enable Lock (AON_VR_EN_LOCK) Lock bit for AON_VR.EN 0b : Unlocked 1b : Locked	pwr_rst_n
1	RO	1'h0	RSVD (RSVD) Reserved	
0	RW/1S	1'h0	AON VR Voltage Select Lock (AON_VR_VSEL_LOCK) Lock bit for AON_VR.VSTRB and AON_VR.SEL 0b : Unlocked 1b : Locked	pwr_rst_n

Power Management Lock (PM_LOCK)

MEM Offset (00000000)	594h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 510. Detailed Description of Power Management Lock (PM_LOCK)

Bits	Access Type	Default	Description	ResetSignal
31:17	RO	15'h0000	RSVD (RSVD) Reserved	



Bits	Access Type	Default	Description	ResetSignal
16	RW/1S	1'h0	Power Management Wait Lock (PM_WAIT_LOCK) Lock bit for PM_WAIT.COLD_RST_WAIT and PM_WAIT.VSTRB_WAIT 0b : Unlocked 1b : Locked	pwr_rst_n
15:11	RO	5'h00	RSVD (RSVD) Reserved	
10	RW/1S	1'h0	Temperature Threshold Lock (TSEL_LOCK) Lock bit for PMNETCS.HTSEL and PMNETCS.LTSEL 0b : Unlocked 1b : Locked	pwr_rst_n
9	RW/1S	1'h0	AVD_OPM Brownout Cold Reset Lock (BOR_VOPM_RST_LOCK) Lock bit for PMNETCS.BOR_VOPM_RST_EN 0b : Unlocked 1b : Locked	pwr_rst_n
8	RW/1S	1'h0	OPM Reference Voltage Lock (VREF_OUT_LOCK) Lock bit for PMNETCS.VREF_OUT_EN 0b : Unlocked 1b : Locked	pwr_rst_n
7:4	RO	4'h0	RSVD (RSVD) Reserved	
3	RW/1S	1'h0	IO State Retention Enable Lock (IO_STATE_RET_LOCK) Lock bit for SLP_CFG.IO_STATE_RET_EN 0b : Unlocked 1b : Locked	pwr_rst_n
2	RW/1S	1'h0	OPM Low Power Mode Enable Lock (LPMODE_LOCK) Lock bit for SLP_CFG.LPMODE_EN 0b : Unlocked 1b : Locked	pwr_rst_n
1	RW/1S	1'h0	RTC Disable Lock (RTC_DIS_LOCK) Lock bit for SLP_CFG.RTC_DIS 0b : Unlocked 1b : Locked	pwr_rst_n
0	RW/1S	1'h0	AON Retention Voltage Lock (AON_RET_LOCK) Lock bit for SLP_CFG.VRET_EN and SLP_CFG.VRET_SEL 0b : Unlocked 1b : Locked	pwr_rst_n



Sensor Subsystem Configuration (SS_CFG)

MEM Offset (00000000) 600h
 Security_PolicyGroup
 IntelRsvd False
 Size 32 bits
 Default 0000_0000h

Table 511. Detailed Description of Sensor Subsystem Configuration (SS_CFG)

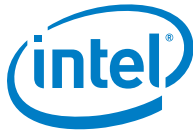
Bits	Access Type	Default	Description
31:27	RO	5'h00	RSVD (RSVD) Reserved
26	RW/P/L	1'h0	Halt Interrupt Redirection (HALT_INT_REDIR) When an enabled sensor subsystem halt interrupt occurs, this bit determines if the interrupt event triggers a warm reset or an entry into Halt. 0b : Warm Reset 1b : Halt Entry
25	RW	1'h0	Asynchronous halt request (ARC_HALT_REQ_A) Writing to this bit halts the ARC core
24	RW	1'h0	Asynchronous run request (ARC_RUN_REQ_A) After rest the Sensor Subsystem is configured to stay in the halted state until ARC_RUN_REQ_A is asserted. This is used during boot to ensure the CCMs are loaded before allowing the RAC to run.
23:16	RW	8'h0	Sensor subsystem processor ID (ARC_NUM) Not used, indicates the ID of the processor
15:0	RW/P/L	16'h0	Code protection control (PROT_RANGE) When the protect bit is set, the processor disables any load or store to the corresponding memory region.

Sensor Subsystem Status (SS_STS)

MEM Offset (00000000) 604h
 Security_PolicyGroup
 IntelRsvd False
 Size 32 bits
 Default 0000_0000h

Table 512. Detailed Description of Sensor Subsystem Status (SS_STS)

Bits	Access Type	Default	Description
31:15	RO	17'h00000	RSVD (RSVD) Reserved
14	RO/V	1'h0	Sensor Subsystem Halt (ARC_HALT) 1b: Processor is Halted



Bits	Access Type	Default	Description
13:11	RO/V	3'h0	Sensor Subsystem sleep mode (ARC_SLEEP_MODE) 1b: Processor in Sleep Mode.
10	RO/V	1'h0	Sensor Subsystem Sleep (ARC_SLEEP) 1b: Processor is Sleeping
9	RO/V	1'h0	Sensor Subsystem Run Acknowledge (ARC_RUN_ACK) Acknowledgement that the processor is running.
8	RO/V	1'h0	Sensor Subsystem Halt Acknowledge (ARC_HALT_ACK) Acknowledgement that the processor is halted.
7	RO/V	1'h0	Sensor Subsystem Debug reset (ARC_DEBUG_RESET) 1b: request from the ARC to be reset. It is based on the state of a debug register in the debug interface
6	RO/V	1'h0	Watchdog reset (ARC_WATCHDOG_RESET) 1b: request from the ARC to be reset. It is based on the timer saturation.
5	RO/V	1'h0	Sensor Subsystem GPIO0 Interrupt Clock Enable (ARC_GPIO0_INTR_CLK_EN)
4:0	RO/V	5'h0	CREG_CTRL (CREG_CTRL)

Always On Counter (AONC_CNT)

MEM Offset (00000000)	700h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 513. Detailed Description of Always On Counter (AONC_CNT)

Bits	Access Type	Default	Description
31:0	RO/V/P	32'h0	Always on count (AONC_CNT) 32 Bit Counter value

Always On Counter Enable (AONC_CFG)

MEM Offset (00000000)	704h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0001h



Table 514. Detailed Description of Always on counter enable (AONC_CFG)

Bits	Access Type	Default	Description
31:1	RO	31'h0	Reserved (RSV)
0	RW/P	1'h1	Always on count enable (AONC_CNT_EN) 1b: enable 0b: disable

Always On Periodic Timer (AONPT_CNT)

MEM Offset (00000000) 708h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 515. Detailed Description of Always on periodic timer (AONPT_CNT)

Bits	Access Type	Default	Description
31:0	RO/V/P	32'h0	Periodic Always On Timer (AONPT_CNT) 32 Bit Always On Timer Value

Always On Periodic Timer Status (AONPT_STAT)

MEM Offset (00000000) 70Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0001h

Table 516. Detailed Description of Always On Periodic Timer Status (AONPT_STAT)

Bits	Access Type	Default	Description
31:1	RO	31'h0	Reserved (RSV)
0	RO/V/P	1'h1	Periodic always on timer status (AONPT_STAT) 1b: always on periodic timer has wrapped and an alarm indication has been generated. This must be cleared before a subsequent alarm indication can be triggered.

Always on periodic timer control (AONPT_CTRL)

MEM Offset (00000000) 710h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

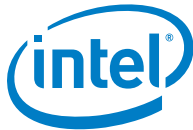


Table 517. Detailed Description of Always on periodic timer control (AONPT_CTRL)

Bits	Access Type	Default	Description
31:2	RO	30'h0	Reserved (RSV)
1	RW/V/P	1'b0	Periodic always on timer reset (AONPT_RST) 1b: always on periodic timer is reset to the value contained in the always on periodic timer configuration register
0	RW/V/P	1'h0	Periodic always on timer alarm clear (AONPT_CLR) 1b is written to this register to clear the periodic always on timer alarm.

Always On Periodic Timer Configuration (AONPT_CFG)

MEM Offset (00000000)	714h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 518. Detailed Description of Always On Periodic Timer Configuration (AONPT_CFG)

Bits	Access Type	Default	Description
31:0	RW/P	32'h0	Periodic always on time out configuration (AONPT_CFG) 0000h: Periodic Always On Counter Disabled. When Set To a Non 0000h Value The Periodic Always On Counter is Loaded With The Configured Time Out Value and down-counts From the Configured Value to 0000h. When it Reaches 0000h an Interrupt is Generated and the Counter Reloads to the Configured Time Out Value.

USB Configuration (USB_PHY_CFG0)

MEM Offset (00000000)	800h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 519. Detailed Description of USB Configuration (USB_PHY_CFG0)

Bits	Access Type	Default	Description
31:2	RO	30'h0000_0000	RSVD (RSVD) Reserved



Bits	Access Type	Default	Description
1	RW/P/L	1'h0	USB Low Speed Mode Enable (USB_LOSR) Control bit to enable USB Low Speed Mode. When disabled, USB operates in Full Speed mode (12 Mbps). When enabled, USB operates in Low Speed mode (1.5 Mbps). 0b : Low Speed Mode Disabled 1b : Low Speed Mode Enabled
0	RW/P/L	1'h0	USB Power Down Mode Enable (USB_STDBY) Control bit to enable USB Power Down Mode. 0b : Power Down Mode Disabled 1b : Power Down Mode Enabled

Peripheral Configuration (PERIPH_CFG0)

MEM Offset (00000000)	804h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 520. Detailed Description of Peripheral Configuration (PERIPH_CFG0)

Bits	Access Type	Default	Description
31:2	RO	30'h0000_0000	RSVD (RSVD) Reserved
1	RW/P/L	1'h0	Watchdog Clock Enable (WDT_CLK_EN) Enables the clock for the peripheral watchdog 0b : Watchdog Clock Disabled 1b : Watchdog Clock Enabled
0	RW/P/L	1'h0	Watchdog Speed Up (WDT_SPEED_UP) Debug mode allowing the watchdog time-out to be accelerated 0b : Watchdog Speed Up Disabled 1b : Watchdog Speed Up Enabled

Configuration Lock (CFG_LOCK)

MEM Offset (00000000)	810h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

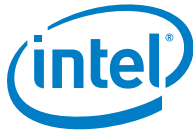


Table 521. Detailed Description of Configuration Lock (CFG_LOCK)

Bits	Access Type	Default	Description	ResetSignal
31:11	RO	21'h000000	RSVD (RSVD) Reserved	
10	RW/1S	1'h0	SS code protection region Lock (PROT_RANGE_LOCK) Lock bit for SS_CFG.PROT_RANGE 0b : Unlocked 1b : Locked	pwr_rst_n
9	RW/1S	1'h0	USB Low Speed Mode Enable Lock (USB_LOSR_LOCK) Lock bit for USB_PHY_CFG0.USB_LOSR 0b : Unlocked 1b : Locked	pwr_rst_n
8	RW/1S	1'h0	USB Power Down Mode Enable Lock (USB_STDBY_LOCK) Lock bit for USB_PHY_CFG0.USB_STDBY 0b : Unlocked 1b : Locked	pwr_rst_n
7:2	RO	6'h00	RSVD (RSVD) Reserved	
1	RW/1S	1'h0	Watchdog Clock Enable Lock (WDT_CLK_EN_LOCK) Lock bit for PERIPH_CFG0.WDT_CLK_EN 0b : Unlocked 1b : Locked	pwr_rst_n
0	RW/1S	1'h0	Watchdog Speed Up Lock (WDT_SPEED_UP_LOCK) Lock bit for PERIPH_CFG0.WDT_SPEED_UP 0b : Unlocked 1b : Locked	pwr_rst_n

Pin Mux Pullup (PMUX_PULLUP [0..3])

MEM Offset (00000000)

[0]:900h [1]:904h [2]:908h [3]:90Ch

Security_PolicyGroup

IntelRsvd

False

Size

32 bits

Default

0000_0000h



Table 522. Detailed Description of Pin Mux Pullup (PMUX_PULLUP [0..3])

Bits	Access Type	Default	Description
31:0	RW/P/L	32'h0	Pin Mux Pullup Enable (PMUX_PU_EN) 0b: disable pull-up 1b: enables pull-up

Pin Mux Slew Rate (PMUX_SLEW [0..3])

MEM Offset (00000000) [0]:910h [1]:914h [2]:918h [3]:91Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 523. Detailed Description of Pin Mux Slew Rate (PMUX_SLEW [0..3])

Bits	Access Type	Default	Description
31:0	RW/P/L	32'h0	Pin mux slew rate (PMUX_SLEW_EN) 0b: 2 mA driver 1b: 4 mA driver

Pin Mux Input Enable (PMUX_IN_EN [0..3])

MEM Offset (00000000) [0]:920h [1]:924h [2]:928h [3]:92Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default FFFF_FFFFh

Table 524. Detailed Description of Pin Mux Input Enable (PMUX_IN_EN [0..3])

Bits	Access Type	Default	Description
31:0	RW/P/L	32'hFFFFFFFF	Pin mux input enable (PMUX_IN_EN) 0b: disable input pad 1b: enables input pad

Pin Mux Select (PMUX_SEL [0..5])

MEM Offset (00000000) [0]:930h [1]:934h [2]:938h [3]:93Ch
 [4]:940h [5]:948h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h



Table 525. Detailed Description of Pin Mux Select (PMUX_SEL [0..5])

Bits	Access Type	Default	Description
31:30	RW/P/L	2'h0	Pin Mux Select 15 (PMUX_SEL15) 00b: Select Mode A 01b: Select Mode B 10b: Select Mode C 11b: Select Mode D
29:28	RW/P/L	2'h0	Pin Mux Select 14 (PMUX_SEL14) 00b: Select Mode A 01b: Select Mode B 10b: Select Mode C 11b: Select Mode D
27:26	RW/P/L	2'h0	Pin Mux Select 13 (PMUX_SEL13) 00b: Select Mode A 01b: Select Mode B 10b: Select Mode C 11b: Select Mode D
25:24	RW/P/L	2'h0	Pin Mux Select 12 (PMUX_SEL12) 00b: Select Mode A 01b: Select Mode B 10b: Select Mode C 11b: Select Mode D
23:22	RW/P/L	2'h0	Pin Mux Select 11 (PMUX_SEL11) 00b: Select Mode A 01b: Select Mode B 10b: Select Mode C 11b: Select Mode D
21:20	RW/P/L	2'h0	Pin Mux Select 10 (PMUX_SEL10) 00b: Select Mode A 01b: Select Mode B 10b: Select Mode C 11b: Select Mode D
19:18	RW/P/L	2'h0	Pin Mux Select 9 (PMUX_SEL9) 00b: Select Mode A 01b: Select Mode B 10b: Select Mode C 11b: Select Mode D
17:16	RW/P/L	2'h0	Pin Mux Select 8 (PMUX_SEL8) 00b: Select Mode A 01b: Select Mode B 10b: Select Mode C 11b: Select Mode D



Bits	Access Type	Default	Description
15:14	RW/P/L	2'h0	Pin Mux Select 7 (PMUX_SEL7) 00b: Select Mode A 01b: Select Mode B 10b: Select Mode C 11b: Select Mode D
13:12	RW/P/L	2'h0	Pin Mux Select 6 (PMUX_SEL6) 00b: Select Mode A 01b: Select Mode B 10b: Select Mode C 11b: Select Mode D
11:10	RW/P/L	2'h0	Pin Mux Select 5 (PMUX_SEL5) 00b: Select Mode A 01b: Select Mode B 10b: Select Mode C 11b: Select Mode D
9:8	RW/P/L	2'h0	Pin Mux Select 4 (PMUX_SEL4) 00b: Select Mode A 01b: Select Mode B 10b: Select Mode C 11b: Select Mode D
7:6	RW/P/L	2'h0	Pin Mux Select 3 (PMUX_SEL3) 00b: Select Mode A 01b: Select Mode B 10b: Select Mode C 11b: Select Mode D
5:4	RW/P/L	2'h0	Pin Mux Select 2 (PMUX_SEL2) 00b: Select Mode A 01b: Select Mode B 10b: Select Mode C 11b: Select Mode D
3:2	RW/P/L	2'h0	Pin Mux Select 1 (PMUX_SEL1) 00b: Select Mode A 01b: Select Mode B 10b: Select Mode C 11b: Select Mode D
1:0	RW/P/L	2'h0	Pin Mux Select 0 (PMUX_SEL0) 00b: Select Mode A 01b: Select Mode B 10b: Select Mode C 11b: Select Mode D

**Pin Mux Pullup Lock (PMUX_PULLUP_LOCK)**

MEM Offset (00000000) 94Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 526. Detailed Description of Pin Mux Pullup Lock (PMUX_PULLUP_LOCK)

Bits	Access Type	Default	Description	ResetSignal
31:4	RO	28'h0000000	RSVD (RSVD) Reserved	
3	RW/1S	1'h0	Pin Mux Pullup 3 Enable Lock (PMUX_PU3_EN_LOCK) 1b: Lock pull-up	pwr_rst_n
2	RW/1S	1'h0	Pin Mux Pullup 2 Enable Lock (PMUX_PU2_EN_LOCK) 1b: Lock pull-up	pwr_rst_n
1	RW/1S	1'h0	Pin Mux Pullup 1 Enable Lock (PMUX_PU1_EN_LOCK) 1b: Lock pull-up	pwr_rst_n
0	RW/1S	1'h0	Pin Mux Pullup 0 Enable Lock (PMUX_PU0_EN_LOCK) 1b: Lock pull-up	pwr_rst_n

Pin Mux Slew Rate Lock (PMUX_SLEW_LOCK)

MEM Offset (00000000) 950h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 527. Detailed Description of Pin Mux Slew Rate Lock (PMUX_SLEW_LOCK)

Bits	Access Type	Default	Description	ResetSignal
31:4	RO	28'h0000000	RSVD (RSVD) Reserved	
3	RW/1S	1'h0	Pin Mux Slew Rate 3 Lock (PMUX_SLEW3_EN_LOCK) 1b: Lock Slew Rate	pwr_rst_n
2	RW/1S	1'h0	Pin Mux Slew Rate 2 Lock (PMUX_SLEW2_EN_LOCK) 1b: Lock Slew Rate	pwr_rst_n



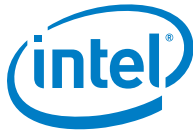
Bits	Access Type	Default	Description	ResetSignal
1	RW/1S	1'h0	Pin Mux Slew Rate 1 Lock (PMUX_SLEW1_EN_LOCK) 1b: Lock Slew Rate	pwr_rst_n
0	RW/1S	1'h0	Pin Mux Slew Rate 0 Lock (PMUX_SLEW0_EN_LOCK) 1b: Lock Slew Rate	pwr_rst_n

Pin Mux Select Lock 0 (PMUX_SEL_0_LOCK)

MEM Offset (00000000) 954h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 528. Detailed Description of Pin Mux Select Lock 0 (PMUX_SEL_0_LOCK)

Bits	Access Type	Default	Description	ResetSignal
31	RW/1S	1'h0	Pin Mux Select Lock 15 (PMUX_SEL15) 1b: Lock Pmux Select	pwr_rst_n
30	RW/1S	1'h0	Pin Mux Select Lock 14 (PMUX_SEL14) 1b: Lock Pmux Select	pwr_rst_n
29	RW/1S	1'h0	Pin Mux Select Lock 13 (PMUX_SEL13) 1b: Lock Pmux Select	pwr_rst_n
28	RW/1S	1'h0	Pin Mux Select Lock 12 (PMUX_SEL12) 1b: Lock Pmux Select	pwr_rst_n
27	RW/1S	1'h0	Pin Mux Select Lock 11 (PMUX_SEL11) 1b: Lock Pmux Select	pwr_rst_n
26	RW/1S	1'h0	Pin Mux Select Lock 10 (PMUX_SEL10) 1b: Lock Pmux Select	pwr_rst_n
25	RW/1S	1'h0	Pin Mux Select Lock 9 (PMUX_SEL9) 1b: Lock Pmux Select	pwr_rst_n
24	RW/1S	1'h0	Pin Mux Select Lock 8 (PMUX_SEL8) 1b: Lock Pmux Select	pwr_rst_n
23	RW/1S	1'h0	Pin Mux Select Lock 7 (PMUX_SEL7) 1b: Lock Pmux Select	pwr_rst_n
22	RW/1S	1'h0	Pin Mux Select Lock 6 (PMUX_SEL6) 1b: Lock Pmux Select	pwr_rst_n
21	RW/1S	1'h0	Pin Mux Select Lock 5 (PMUX_SEL5) 1b: Lock Pmux Select	pwr_rst_n



Bits	Access Type	Default	Description	ResetSignal
20	RW/1S	1'h0	Pin Mux Select Lock 4 (PMUX_SEL4) 1b: Lock Pmux Select	pwr_rst_n
19	RW/1S	1'h0	Pin Mux Select Lock 3 (PMUX_SEL3) 1b: Lock Pmux Select	pwr_rst_n
18	RW/1S	1'h0	Pin Mux Select Lock 2 (PMUX_SEL2) 1b: Lock Pmux Select	pwr_rst_n
17	RW/1S	1'h0	Pin Mux Select Lock 1 (PMUX_SEL1) 1b: Lock Pmux Select	pwr_rst_n
16	RW/1S	1'h0	Pin Mux Select Lock 0 (PMUX_SELO) 1b: Lock Pmux Select	pwr_rst_n
15	RW/1S	1'h0	Pin Mux Select Lock 15 (PMUX_SELY15) 1b: Lock Pmux Select	pwr_rst_n
14	RW/1S	1'h0	Pin Mux Select Lock 14 (PMUX_SELY14) 1b: Lock Pmux Select	pwr_rst_n
13	RW/1S	1'h0	Pin Mux Select Lock 13 (PMUX_SELY13) 1b: Lock Pmux Select	pwr_rst_n
12	RW/1S	1'h0	Pin Mux Select Lock 12 (PMUX_SELY12) 1b: Lock Pmux Select	pwr_rst_n
11	RW/1S	1'h0	Pin Mux Select Lock 11 (PMUX_SELY11) 1b: Lock Pmux Select	pwr_rst_n
10	RW/1S	1'h0	Pin Mux Select Lock 10 (PMUX_SELY10) 1b: Lock Pmux Select	pwr_rst_n
9	RW/1S	1'h0	Pin Mux Select Lock 9 (PMUX_SELY9) 1b: Lock Pmux Select	pwr_rst_n
8	RW/1S	1'h0	Pin Mux Select Lock 8 (PMUX_SELY8) 1b: Lock Pmux Select	pwr_rst_n
7	RW/1S	1'h0	Pin Mux Select Lock 7 (PMUX_SELY7) 1b: Lock Pmux Select	pwr_rst_n
6	RW/1S	1'h0	Pin Mux Select Lock 6 (PMUX_SELY6) 1b: Lock Pmux Select	pwr_rst_n
5	RW/1S	1'h0	Pin Mux Select Lock 5 (PMUX_SELY5) 1b: Lock Pmux Select	pwr_rst_n
4	RW/1S	1'h0	Pin Mux Select Lock 4 (PMUX_SELY4) 1b: Lock Pmux Select	pwr_rst_n
3	RW/1S	1'h0	Pin Mux Select Lock 3 (PMUX_SELY3) 1b: Lock Pmux Select	pwr_rst_n
2	RW/1S	1'h0	Pin Mux Select Lock 2 (PMUX_SELY2) 1b: Lock Pmux Select	pwr_rst_n



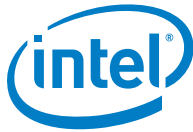
Bits	Access Type	Default	Description	ResetSignal
1	RW/1S	1'h0	Pin Mux Select Lock 1 (PMUX_SELY1) 1b: Lock Pmux Select	pwr_rst_n
0	RW/1S	1'h0	Pin Mux Select Lock 0 (PMUX_SELY0) 1b: Lock Pmux Select	pwr_rst_n

Pin Mux Select Lock 1 (PMUX_SEL_1_LOCK)

MEM Offset (00000000) 958h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 529. Detailed Description of Pin Mux Select Lock 1 (PMUX_SEL_1_LOCK)

Bits	Access Type	Default	Description	ResetSignal
31	RW/1S	1'h0	Pin Mux Select Lock 15 (PMUX_SEL15) 1b: Lock Pmux Select	pwr_rst_n
30	RW/1S	1'h0	Pin Mux Select Lock 14 (PMUX_SEL14) 1b: Lock Pmux Select	pwr_rst_n
29	RW/1S	1'h0	Pin Mux Select Lock 13 (PMUX_SEL13) 1b: Lock Pmux Select	pwr_rst_n
28	RW/1S	1'h0	Pin Mux Select Lock 12 (PMUX_SEL12) 1b: Lock Pmux Select	pwr_rst_n
27	RW/1S	1'h0	Pin Mux Select Lock 11 (PMUX_SEL11) 1b: Lock Pmux Select	pwr_rst_n
26	RW/1S	1'h0	Pin Mux Select Lock 10 (PMUX_SEL10) 1b: Lock Pmux Select	pwr_rst_n
25	RW/1S	1'h0	Pin Mux Select Lock 9 (PMUX_SEL9) 1b: Lock Pmux Select	pwr_rst_n
24	RW/1S	1'h0	Pin Mux Select Lock 8 (PMUX_SEL8) 1b: Lock Pmux Select	pwr_rst_n
23	RW/1S	1'h0	Pin Mux Select Lock 7 (PMUX_SEL7) 1b: Lock Pmux Select	pwr_rst_n
22	RW/1S	1'h0	Pin Mux Select Lock 6 (PMUX_SEL6) 1b: Lock Pmux Select	pwr_rst_n
21	RW/1S	1'h0	Pin Mux Select Lock 5 (PMUX_SEL5) 1b: Lock Pmux Select	pwr_rst_n
20	RW/1S	1'h0	Pin Mux Select Lock 4 (PMUX_SEL4) 1b: Lock Pmux Select	pwr_rst_n



Bits	Access Type	Default	Description	ResetSignal
19	RW/1S	1'h0	Pin Mux Select Lock 3 (PMUX_SEL3) 1b: Lock Pmux Select	pwr_rst_n
18	RW/1S	1'h0	Pin Mux Select Lock 2 (PMUX_SEL2) 1b: Lock Pmux Select	pwr_rst_n
17	RW/1S	1'h0	Pin Mux Select Lock 1 (PMUX_SEL1) 1b: Lock Pmux Select	pwr_rst_n
16	RW/1S	1'h0	Pin Mux Select Lock 0 (PMUX_SEL0) 1b: Lock Pmux Select	pwr_rst_n
15	RW/1S	1'h0	Pin Mux Select Lock 15 (PMUX_SELY15) 1b: Lock Pmux Select	pwr_rst_n
14	RW/1S	1'h0	Pin Mux Select Lock 14 (PMUX_SELY14) 1b: Lock Pmux Select	pwr_rst_n
13	RW/1S	1'h0	Pin Mux Select Lock 13 (PMUX_SELY13) 1b: Lock Pmux Select	pwr_rst_n
12	RW/1S	1'h0	Pin Mux Select Lock 12 (PMUX_SELY12) 1b: Lock Pmux Select	pwr_rst_n
11	RW/1S	1'h0	Pin Mux Select Lock 11 (PMUX_SELY11) 1b: Lock Pmux Select	pwr_rst_n
10	RW/1S	1'h0	Pin Mux Select Lock 10 (PMUX_SELY10) 1b: Lock Pmux Select	pwr_rst_n
9	RW/1S	1'h0	Pin Mux Select Lock 9 (PMUX_SELY9) 1b: Lock Pmux Select	pwr_rst_n
8	RW/1S	1'h0	Pin Mux Select Lock 8 (PMUX_SELY8) 1b: Lock Pmux Select	pwr_rst_n
7	RW/1S	1'h0	Pin Mux Select Lock 7 (PMUX_SELY7) 1b: Lock Pmux Select	pwr_rst_n
6	RW/1S	1'h0	Pin Mux Select Lock 6 (PMUX_SELY6) 1b: Lock Pmux Select	pwr_rst_n
5	RW/1S	1'h0	Pin Mux Select Lock 5 (PMUX_SELY5) 1b: Lock Pmux Select	pwr_rst_n
4	RW/1S	1'h0	Pin Mux Select Lock 4 (PMUX_SELY4) 1b: Lock Pmux Select	pwr_rst_n
3	RW/1S	1'h0	Pin Mux Select Lock 3 (PMUX_SELY3) 1b: Lock Pmux Select	pwr_rst_n
2	RW/1S	1'h0	Pin Mux Select Lock 2 (PMUX_SELY2) 1b: Lock Pmux Select	pwr_rst_n
1	RW/1S	1'h0	Pin Mux Select Lock 1 (PMUX_SELY1) 1b: Lock Pmux Select	pwr_rst_n



Bits	Access Type	Default	Description	ResetSignal
0	RW/1S	1'h0	Pin Mux Select Lock 0 (PMUX_SELY0) 1b: Lock Pmux Select	pwr_rst_n

Pin Mux Select Lock 2 (PMUX_SEL_2_LOCK)

MEM Offset (00000000) 95Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 530. Detailed Description of Pin Mux Select Lock 2 (PMUX_SEL_2_LOCK)

Bits	Access Type	Default	Description	ResetSignal
31	RW/1S	1'h0	Pin Mux Select Lock 15 (PMUX_SEL15) 1b: Lock Pmux Select	pwr_rst_n
30	RW/1S	1'h0	Pin Mux Select Lock 14 (PMUX_SEL14) 1b: Lock Pmux Select	pwr_rst_n
29	RW/1S	1'h0	Pin Mux Select Lock 13 (PMUX_SEL13) 1b: Lock Pmux Select	pwr_rst_n
28	RW/1S	1'h0	Pin Mux Select Lock 12 (PMUX_SEL12) 1b: Lock Pmux Select	pwr_rst_n
27	RW/1S	1'h0	Pin Mux Select Lock 11 (PMUX_SEL11) 1b: Lock Pmux Select	pwr_rst_n
26	RW/1S	1'h0	Pin Mux Select Lock 10 (PMUX_SEL10) 1b: Lock Pmux Select	pwr_rst_n
25	RW/1S	1'h0	Pin Mux Select Lock 9 (PMUX_SEL9) 1b: Lock Pmux Select	pwr_rst_n
24	RW/1S	1'h0	Pin Mux Select Lock 8 (PMUX_SEL8) 1b: Lock Pmux Select	pwr_rst_n
23	RW/1S	1'h0	Pin Mux Select Lock 7 (PMUX_SEL7) 1b: Lock Pmux Select	pwr_rst_n
22	RW/1S	1'h0	Pin Mux Select Lock 6 (PMUX_SEL6) 1b: Lock Pmux Select	pwr_rst_n
21	RW/1S	1'h0	Pin Mux Select Lock 5 (PMUX_SEL5) 1b: Lock Pmux Select	pwr_rst_n
20	RW/1S	1'h0	Pin Mux Select Lock 4 (PMUX_SEL4) 1b: Lock Pmux Select	pwr_rst_n
19	RW/1S	1'h0	Pin Mux Select Lock 3 (PMUX_SEL3) 1b: Lock Pmux Select	pwr_rst_n



Bits	Access Type	Default	Description	ResetSignal
18	RW/1S	1'h0	Pin Mux Select Lock 2 (PMUX_SEL2) 1b: Lock Pmux Select	pwr_rst_n
17	RW/1S	1'h0	Pin Mux Select Lock 1 (PMUX_SEL1) 1b: Lock Pmux Select	pwr_rst_n
16	RW/1S	1'h0	Pin Mux Select Lock 0 (PMUX_SEL0) 1b: Lock Pmux Select	pwr_rst_n
15	RW/1S	1'h0	Pin Mux Select Lock 15 (PMUX_SELY15) 1b: Lock Pmux Select	pwr_rst_n
14	RW/1S	1'h0	Pin Mux Select Lock 14 (PMUX_SELY14) 1b: Lock Pmux Select	pwr_rst_n
13	RW/1S	1'h0	Pin Mux Select Lock 13 (PMUX_SELY13) 1b: Lock Pmux Select	pwr_rst_n
12	RW/1S	1'h0	Pin Mux Select Lock 12 (PMUX_SELY12) 1b: Lock Pmux Select	pwr_rst_n
11	RW/1S	1'h0	Pin Mux Select Lock 11 (PMUX_SELY11) 1b: Lock Pmux Select	pwr_rst_n
10	RW/1S	1'h0	Pin Mux Select Lock 10 (PMUX_SELY10) 1b: Lock Pmux Select	pwr_rst_n
9	RW/1S	1'h0	Pin Mux Select Lock 9 (PMUX_SELY9) 1b: Lock Pmux Select	pwr_rst_n
8	RW/1S	1'h0	Pin Mux Select Lock 8 (PMUX_SELY8) 1b: Lock Pmux Select	pwr_rst_n
7	RW/1S	1'h0	Pin Mux Select Lock 7 (PMUX_SELY7) 1b: Lock Pmux Select	pwr_rst_n
6	RW/1S	1'h0	Pin Mux Select Lock 6 (PMUX_SELY6) 1b: Lock Pmux Select	pwr_rst_n
5	RW/1S	1'h0	Pin Mux Select Lock 5 (PMUX_SELY5) 1b: Lock Pmux Select	pwr_rst_n
4	RW/1S	1'h0	Pin Mux Select Lock 4 (PMUX_SELY4) 1b: Lock Pmux Select	pwr_rst_n
3	RW/1S	1'h0	Pin Mux Select Lock 3 (PMUX_SELY3) 1b: Lock Pmux Select	pwr_rst_n
2	RW/1S	1'h0	Pin Mux Select Lock 2 (PMUX_SELY2) 1b: Lock Pmux Select	pwr_rst_n
1	RW/1S	1'h0	Pin Mux Select Lock 1 (PMUX_SELY1) 1b: Lock Pmux Select	pwr_rst_n
0	RW/1S	1'h0	Pin Mux Select Lock 0 (PMUX_SELY0) 1b: Lock Pmux Select	pwr_rst_n



Pin Mux Slew Rate Lock (PMUX_IN_EN_LOCK)

MEM Offset (00000000) 960h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 531. Detailed Description of Pin Mux Slew Rate Lock (PMUX_IN_EN_LOCK)

Bits	Access Type	Default	Description	ResetSignal
31:4	RO	28'h0000000	RSVD (RSVD) Reserved	
3	RW/1S	1'h0	Pin Mux Input enable 3 Lock (PMUX_IN3_EN_LOCK) 1b: Lock Input Enable	pwr_rst_n
2	RW/1S	1'h0	Pin Mux Input enable 2 Lock (PMUX_IN2_EN_LOCK) 1b: Lock Input Enable	pwr_rst_n
1	RW/1S	1'h0	Pin Mux Input enable 1 Lock (PMUX_IN1_EN_LOCK) 1b: Lock Input Enable	pwr_rst_n
0	RW/1S	1'h0	Pin Mux Input enable 0 Lock (PMUX_IN0_EN_LOCK) 1b: Lock Input Enable	pwr_rst_n

Mailbox Channel Control Word (MBOX_CH_CTRL [0..7])

The source processor should not re-write the Control Word or any of the Payload Data if the status flag in CHn_STS is asserted

MEM Offset (00000000) [0]:0A00h [1]:0A18h [2]:0A30h [3]:0A48h
 [4]:0A60h [5]:0A78h [6]:0A90h [7]:0AA8h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

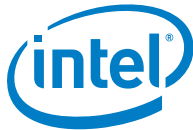


Table 532. Detailed Description of Mailbox Channel Control Word (MBOX_CH_CTRL [0..7])

Bits	Access Type	Default	Description
31	RW/1S/V	1'h0	Mailbox Channel Control Word interrupt (MBOX_CH_CTRL_INT) A write of 1 to Bit 31 of this register will trigger the channel interrupt and set the corresponding flag in the CHn_STS register. The Payload Data, if any, should be populated in advance of writing to this register
30:0	RW	31'h0	Mailbox Channel Control Word (MBOX_CH_CTRL) Mailbox Channel 0 Control Word The Control Word format/encoding is completely flexibly and can be defined at the Mailbox software protocol level. For example, the Control Word could be a Message Identifier.

Mailbox Channel Payload Data Word 0 (MBOX_CH_DATA0 [0..7])

MEM Offset (00000000)	[0]:0A04h [1]:0A1Ch [2]:0A34h [3]:0A4Ch [4]:0A64h [5]:0A7Ch [6]:0A94h [7]:0AACh
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 533. Detailed Description of Mailbox Channel Payload Data Word 0 (MBOX_CH_DATA0 [0..7])

Bits	Access Type	Default	Description
31:0	RW	32'h0	Mailbox Channel Payload Data Word 0 (MBOX_CH_DATA0) 1st 32bits of Data Payload

Mailbox Channel Payload Data Word 1 (MBOX_CH_DATA1 [0..7])

MEM Offset (00000000)	[0]:0A08h [1]:0A20h [2]:0A38h [3]:0A50h [4]:0A68h [5]:0A80h [6]:0A98h [7]:0AB0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 534. Detailed Description of Mailbox Channel Payload Data Word 1 (MBOX_CH_DATA1 [0..7])

Bits	Access Type	Default	Description
31:0	RW	32'h0	Mailbox Channel Payload Data Word 1 (MBOX_CH_DATA1) 2nd 32bits of Data Payload

Mailbox Channel Payload Data Word 2 (MBOX_CH_DATA2 [0..7])

MEM Offset (00000000) [0]:0A0Ch [1]:0A24h [2]:0A3Ch [3]:0A54h
[4]:0A6Ch [5]:0A84h [6]:0A9Ch [7]:0AB4h

Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 535. Detailed Description of Mailbox Channel Payload Data Word 2 (MBOX_CH_DATA2 [0..7])

Bits	Access Type	Default	Description
31:0	RW	32'h0	Mailbox Channel Payload Data Word 2 (MBOX_CH_DATA2) 3rd 32bits of Data Payload

Mailbox Channel Payload Data Word 3 (MBOX_CH_DATA3 [0..7])

MEM Offset (00000000) [0]:0A10h [1]:0A28h [2]:0A40h [3]:0A58h
[4]:0A70h [5]:0A88h [6]:0AA0h [7]:0AB8h

Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

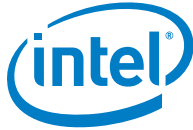
Table 536. Detailed Description of Mailbox Channel Payload Data Word 3 (MBOX_CH_DATA3 [0..7])

Bits	Access Type	Default	Description
31:0	RW	32'h0	Mailbox Channel Payload Data Word 3 (MBOX_CH_DATA3) 4th 32bits of Data Payload

Mailbox Channel Status (MBOX_CH_STS [0..7])

MEM Offset (00000000) [0]:0A14h [1]:0A2Ch [2]:0A44h [3]:0A5Ch
[4]:0A74h [5]:0A8Ch [6]:0AA4h [7]:0ABCh

Security_PolicyGroup
IntelRsvd False
Size 32 bits



Default

0000_0000h

Table 537. Detailed Description of Mailbox Channel Status (MBOX_CH_STS [0..7])

Bits	Access Type	Default	Description
31:2	RO	30'h0000_0000	RSVD (RSVD) Reserved
1	RW/1C/V	1'h0	Mailbox Channel Status (MBOX_CH_STS_CTRL_INT) This registers contains a single interrupt flag that represents the state of the channel interrupt. The interrupt (and correspondingly the flag) is cleared by writing 1 to this status flag.
0	RW/1C/V	1'h0	Mailbox Channel Status (MBOX_CH_STS) This registers contains a single status flag that represents the state of the channel. The status (and correspondingly the flag) is cleared by writing 1 to this status flag.

Channel Status Bits (MBOX_CHALL_STS)

MEM Offset (00000000)	0AC0h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 538. Detailed Description of Channel Status Bits (MBOX_CHALL_STS)

Bits	Access Type	Default	Description
31:16	RO	16'h0000	RSVD (RSVD) Reserved
15:0	RO/V	16'h0	Channel Status Bits (MBOX_CHALL_STS) A read only register showing all status bits of the mailboxes CHn_STS[1:0]

Port A GPIO_AON (GPIO_SWPORTA_DR)

Contains the GPIO Port data bits

MEM Offset (00000000)	0B00h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 539. Detailed Description of Port A GPIO_AON (GPIO_SWPORTA_DR)

Bits	Access Type	Default	Description
31:6	RO	26'h0000000	RSVD (RSVD) Reserved
5:0	RW/P	6'b0	Port Data (GPIO_SWPORTA_DR) Values written to this register are output on the I/O signals for if the corresponding data direction bits are set to Output mode and the corresponding control bit for the Port is set to Software mode. The value read back is equal to the last value written to this register

Port A GPIO_AON Direction (GPIO_SWPORTA_DDR)

Used to control the GPIO Port bits data direction

MEM Offset (00000000)	0B04h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 540. Detailed Description of Port A GPIO_AON Direction (GPIO_SWPORTA_DDR)

Bits	Access Type	Default	Description
31:6	RO	26'h0000000	RSVD (RSVD) Reserved
5:0	RW/P	6'b0	Port Data Direction (GPIO_SWPORTA_DDR) Values written to this register independently control the direction of the corresponding data bit in the Port - 0 Input (default) - 1 Output

Port A GPIO_AON Source (GPIO_SWPORTA_CTL)

Used to control the GPIO Port Data Source

MEM Offset (00000000)	0B08h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

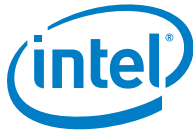


Table 541. Detailed Description of Port A GPIO_AON Source (GPIO_SWPORTA_CTL)

Bits	Access Type	Default	Description
31:1	RO	31'h0000_0000	RSVD (RSVD) Reserved
0	RW/P	1'b0	Port A Data Source (GPIO_SWPORTA_CTL) The data and control source for a signal can come from either software or hardware; this bit selects between them. The default source is configurable through the GPIO_DFLT_SRC_A configuration parameter. 0 Software mode (default) 1 Hardware mode

Interrupt Enable (GPIO_INTEN)

Used to configured Port A bits as interrupt sources

MEM Offset (00000000)	0B30h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 542. Detailed Description of Interrupt Enable (GPIO_INTEN)

Bits	Access Type	Default	Description
31:6	RO	26'h00000000	RSVD (RSVD) Reserved
5:0	RW/P	6'b0	Interrupt Enable (GPIO_INTEN) Allows each bit of Port A to be configured for interrupts. By default the generation of interrupts is disabled. Whenever a 1 is written to a bit of this register, it configures the corresponding bit on Port A to become an interrupt; otherwise, Port A operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of Port A if the corresponding data direction register is set to Output. 0 Configure Port A bit as normal GPIO signal (default) 1 Configure Port A bit as interrupt

Interrupt Mask (GPIO_INTMASK)

Controls masking for Port A bits configured as interrupt sources

MEM Offset (00000000)	0B34h
Security_PolicyGroup	
IntelRsvd	False



Size 32 bits
Default 0000_0000h

Table 543. Detailed Description of Interrupt Mask (GPIO_INTMASK)

Bits	Access Type	Default	Description
31:6	RO	26'h0000000	RSVD (RSVD) Reserved
5:0	RW/P	6'b0	Interrupt Mask (GPIO_INTMASK) Controls whether an interrupt on Port A can create an interrupt for the interrupt controller by not masking it. By default, all interrupts bits are unmasked. Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through. The unmasked status can be read as well as the resultant status after masking. 0 Interrupt bits are unmasked (default) 1 Mask interrupt

Interrupt Type (GPIO_INTTYPE_LEVEL)

Controls the type of interrupt associated with Port A bits configured as interrupt source

MEM Offset (00000000) 0B38h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 544. Detailed Description of Interrupt Type (GPIO_INTTYPE_LEVEL)

Bits	Access Type	Default	Description
31:6	RO	26'h0000000	RSVD (RSVD) Reserved
5:0	RW/P	6'b0	Interrupt Type (GPIO_INTTYPE_LEVEL) Controls the type of interrupt that can occur on Port A. Whenever a 0 is written to a bit of this register, it configures the interrupt type to be level-sensitive; otherwise, it is edge-sensitive. 0 Level-sensitive (default) 1 Edge-sensitive

Interrupt Polarity (GPIO_INT_POLARITY)

Controls the interrupt polarity associated with Port A bits configured as interrupt sources



MEM Offset (00000000) 0B3Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 545. Detailed Description of Interrupt Polarity (GPIO_INT_POLARITY)

Bits	Access Type	Default	Description
31:6	RO	26'h0000000	RSVD (RSVD) Reserved
5:0	RW/P	6'b0	Interrupt Polarity (GPIO_INT_POLARITY) Controls the polarity of edge or level sensitivity that can occur on input of Port A. Whenever a 0 is written to a bit of this register, it configures the interrupt type to falling-edge or active-low sensitive; otherwise, it is rising-edge or active-high sensitive. 0 Active-low (default) 1 Active-high

Interrupt Status (GPIO_INTSTATUS)

Stores the interrupt status after masking for Port A bits configured as interrupt sources

MEM Offset (00000000) 0B40h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Table 546. Detailed Description of Interrupt Status (GPIO_INTSTATUS)

Bits	Access Type	Default	Description
31:6	RO	26'h0000000	RSVD (RSVD) Reserved
5:0	RO/V/P	6'b0	Interrupt Status (GPIO_INTSTATUS) After mask. See GPIO_RAW_INTSTATUS for raw interrupt values and GPIO_INTMASK for interrupt mask configuration

Raw Interrupt Status (GPIO_RAW_INTSTATUS)

MEM Offset (00000000) 0B44h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h



Table 547. Detailed Description of Raw Interrupt Status (GPIO_RAW_INTSTATUS)

Bits	Access Type	Default	Description
31:6	RO	26'h0000000	RSVD (RSVD) Reserved
5:0	RO/V/P	6'b0	Raw Interrupt Status (GPIO_RAW_INTSTATUS) Raw interrupt of status of Port A (premasking bits)

Debounce Enable (GPIO_DEBOUNCE)

Controls the debounce logic associated to a Port A bit configured as interrupt source

MEM Offset (00000000)	0B48h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 548. Detailed Description of Debounce Enable (GPIO_DEBOUNCE)

Bits	Access Type	Default	Description
31:6	RO	26'h0000000	RSVD (RSVD) Reserved
5:0	RW/P	6'b0	Debounce Enable (GPIO_DEBOUNCE) Controls whether an external signal that is the source of an interrupt needs to be debounced to remove any spurious glitches. Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed. 0 No debounce (default) 1 Enable debounce

Clear Interrupt (GPIO_PORTA_EOI)

Controls edge-type interrupt clearing

MEM Offset (00000000)	0B4Ch
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

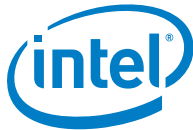


Table 549. Detailed Description of Clear Interrupt (GPIO_PORTA_EOI)

Bits	Access Type	Default	Description
31:6	RO	26'h0000000	RSVD (RSVD) Reserved
5:0	RW/1C/V/P	6'b0	Clear Interrupt (GPIO_PORTA_EOI) Controls the clearing of edge type interrupts from Port A. When a 1 is written into a corresponding bit of this register, the interrupt is cleared. All interrupts are cleared when Port A is not configured for interrupts. 0 No interrupt clear (default) 1 Clear interrupt

Port A External Port (GPIO_EXT_PORTA)

Used by the software to read values from the GPIO Port bits

MEM Offset (00000000)	0B50h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

Table 550. Detailed Description of Port A External Port (GPIO_EXT_PORTA)

Bits	Access Type	Default	Description
31:6	RO	26'h0000000	RSVD (RSVD) Reserved
5:0	RO/V/P	6'b0	External Port (GPIO_EXT_PORTA) When the Port is configured as Input, then reading this location reads the values on the external signal. When the data direction is set as Output, reading this location reads the Port data register contents

Synchronization Level (GPIO_LS_SYNC)

Controls if a level-sensitive interrupt type need to be synchronized to the system clock

MEM Offset (00000000)	0B60h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h



Table 551. Detailed Description of Synchronization Level (GPIO_LS_SYNC)

Bits	Access Type	Default	Description
31:1	RO	31'b0	Reserved (RSV)
0	RW/P	1'b0	Synchronization Level (GPIO_LS_SYNC) Writing a 1 to this register results in all level-sensitive interrupts being synchronized to the system clock. 0 Not Synchronized (default) 1 Synchronized

Interrupt both edge type (GPIO_INT_BOTHEDGE)

Controls the edge type of interrupt that can occur on Port A

MEM Offset (00000000)	0B68h
Security_PolicyGroup	
IntelRsvd	False
Size	32 bits
Default	0000_0000h

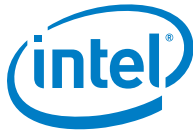
Table 552. Detailed Description of Interrupt both edge type (GPIO_INT_BOTHEDGE)

Bits	Access Type	Default	Description
31:6	RO	26'h0000000	RSVD (RSVD) Reserved
5:0	RW/P	6'b0	Interrupt both edge type (GPIO_PWIDTH_A) Controls the edge type of interrupt that can occur on Port A. Whenever a particular bit is programmed to 1, it enables the generation of interrupts on both the rising edge and the falling edge of an external input signal corresponding to that bit on port A. The values programmed in the registers gpio_intype_level and gpio_int_polarity for this particular bit are not considered when the corresponding bit of this register is set to 1. Whenever a particular bit is programmed to 0, the interrupt type depends on the value of the corresponding bits in the gpio_inttype_level and gpio_int_polarity registers. 0 - Active-low (default) 1 - Active-high

GPIO Configuration 2 (GPIO_CONFIG_REG2)

Stores the bit Port width minus one.

MEM Offset (00000000)	0B70h



Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0003_9E73h

Table 553. Detailed Description of GPIO Configuration 2 (GPIO_CONFIG_REG2)

Bits	Access Type	Default	Description
31:20	RO	12'b0	Reserved (RSV)
19:15	RO	5'b00111	Port D width (ENCODED_ID_PWIDTH_D) Port D is not used
14:10	RO	5'b00111	Port C width (ENCODED_ID_PWIDTH_C) Port C is not used
9:5	RO	5'b10011	Port B width (ENCODED_ID_PWIDTH_B) The value of this register is equal to (port B bits - 1) Intel® Quark™ SoC X1000 GPIO Port B uses 20 bits. Value = 0x13
4:0	RO	5'b10011	Port A width (ENCODED_ID_PWIDTH_A) The value of this register is equal to (port A bits - 1) Intel® Quark™ SoC X1000 GPIO Port A uses 20 bits. Value = 0x13

GPIO Configuration 1 (GPIO_CONFIG_REG1)

Stores information on the GPIO controller configuration

MEM Offset (00000000) 0B74h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 001F_70F6h

Table 554. Detailed Description of GPIO Configuration 1 (GPIO_CONFIG_REG1)

Bits	Access Type	Default	Description
31:21	RO	11'b0	Reserved (RSV)
20:16	RO	5'b11111	GPIO ID Width (ENCODED_ID_WIDTH) Not used
15	RO	1'b0	GPIO ID Support (GPIO_ID) 0 = exclude 1 = include



Bits	Access Type	Default	Description
14	RO	1'b1	Encoded Parameters (ADD_ENCODED_PARAMS) 0 = false 1 = true
13	RO	1'b1	Port A Debounce Logic Support (DEBOUNCE) 0 = exclude 1 = include
12	RO	1'b1	Port A Interrupt Source Support (PORTA_INTR) Port A as an interrupt source 0 = exclude 1 = include
11	RO	1'b0	Port D Hardware Control Support (HW_PORTD) 0 = exclude 1 = include
10	RO	1'b0	Port C Hardware Control Support (HW_PORTC) 0 = exclude 1 = include
9	RO	1'b0	Port B Hardware Control Support (HW_PORTB) 0 = exclude 1 = include
8	RO	1'b0	Port A Hardware Control Support (HW_PORTA) 0 = exclude 1 = include
7	RO	1'b1	Port D Source Control Mode (PORTD_SINGLE_CTL) All Port bits controlled by a single source (HW/SW) 0 = false 1 = true NOTE: Valid only if both HW and SW control modes are supported (GPIO_CONFIG_REG1.HW_PORTx fields)
6	RO	1'b1	Port C Source Control Mode (PORTC_SINGLE_CTL) All Port bits controlled by a single source (HW/SW) 0 = false 1 = true NOTE: Valid only if both HW and SW control modes are supported (GPIO_CONFIG_REG1.HW_PORTx fields)



Bits	Access Type	Default	Description
5	RO	1'b1	Port B Source Control Mode (PORTB_SINGLE_CTL) All Port bits controlled by a single source (HW/SW) 0 = false 1 = true NOTE: Valid only if both HW and SW control modes are supported (GPIO_CONFIG_REG1.HW_PORTx fields)
4	RO	1'b1	Port A Source Control Mode (PORTA_SINGLE_CTL) All Port bits controlled by a single source (HW/SW) 0 = false 1 = true NOTE: Valid only if both HW and SW control modes are supported (GPIO_CONFIG_REG1.HW_PORTx fields)
3:2	RO	2'b01	Number of ports (NUM_PORTS) Number of ports supported 0x0 = 1 0x1 = 2 0x2 = 3 0x3 = 4
1:0	RO	2'b10	System Data Bus Width (APB_DATA_WIDTH) Width of Data Bus to which this component is attached. 0x0 = 8 bits 0x1 = 16 bits 0x2 = 32 bits



29 AON Counters

The Intel® Quark™ SE Microcontroller C1000 supports 2 Always On counters. Both counters run off the 32 kHz RTC clock.

The first counter is an always on free running counter (AONC).

The second is a periodic counter (AONPT) which allows a timer value to be loaded, and an interrupt to fire when the timer expires.

29.1 Features

29.1.1 AON Counter

The following is a list of AON counters features:

- A free running up counter running off the 32,768Hz clock
- Can be enabled and disabled through software
- Can be accessed by any AHB Master in the fabric and used as a general purpose timer
- Connected directly to the Sensor subsystem - can be used for time-stamping samples received from the sensors

29.1.2 AON Periodic Timer

The following is a list of AON periodic timer features:

- Periodic counter running off the 32,768 Hz clock
- AON Periodic Timer continuously decrements from a configured value
- AON Periodic Timer expires when the counter reaches 0
- When the AON Periodic Timer expires it reloads a configured value and decrements
- The AON Periodic Timer is disabled by loading a value of 0, it is enabled by loading a non 0 value
- Generates an alarm when the timer expires

The AON Periodic Timer configuration comes from the core clock domain – the AON Periodic Timer is clocked using the RTC clock, so it will take a number of core clocks for the AON Periodic Timer configuration to propagate into the RTC clock domain. To program the AON Periodic Timer (that is, clear an alarm via the AONPT_CTRL.AONPT_CLR register bit or reset the counter value via the AONPT_CTRL.AONPT_RST) the relevant control bit must be set by software and then



polled until it is cleared by hardware. At this point the desired configuration has taken effect.

The counter can then reset to the value contained in (**AONPT_CFG**) by writing to 1 to (**AONPT_RST**). (**AONPT_RST**) is self-clearing, however, due to the CDC from the slow to the fast domain, you must poll the register to ensure the reset has occurred. To do this, follow these steps:

1. Write value to the (**AONPT_CFG**) to stop the counter.
2. Write 1 to (**AONPT_RST**) to apply the counter value.
3. Poll (**AONPT_RST**) to ensure the operation has complete.

Note: Step 3 can take a number of 32 kHz clocks (1000s of 32 MHz clocks to complete).

The sequence for clearing an interrupt is as follows:

1. Interrupt asserted.
2. Write 0 to the (**AONPT_CFG**) to stop the counter.
3. Write 1 to (**AONPT_CLR**) to clear the interrupt.
4. Poll (**AONPT_CLR**) to ensure the operation has complete.

Note: Step 3 can take a number of 32 kHz clocks (1000s of 32 MHz clocks to complete).



30 Debug Port and JTAG/TAP

30.1 Signal Descriptions

The JTAG interface is a 5-pin interface timed with respect to TCK input clock.

- TMS, TDI are inputs which are sampled by SoC on rising edge of TCK and is expected to be driven by JTAG host on falling edge of TCK.
- TDO is output from SoC driven on falling edge of TCK and expected to be sampled by JTAG host on rising edge of TCK.
- TRSTB is asynchronous signal.

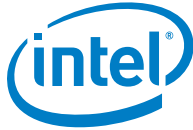
Delays shown in the following table are with respect to SoC.

Parameter	Min	Max
TCK clock frequency	-	8 MHz (125 ns)
Setup time of TMS, TDI with respect to rising edge of TCK	25 ns	-
Hold time of TMS, TDI with respect to rising edge of TCK	0 ns	-
Output data valid delay of TDO with respect to falling edge of TCK	1 ns	40 ns
Output tristate delay of TDO with respect to falling edge of TCK	-	40 ns

Output load supported for JTAG TDO output is 40 pF max and 5 pF min.

30.2 Probe Mode

The Sensor Subsystem core supports a halt mode to facilitate debug. The Sensor Subsystem can be halted due to an internal event where an action point triggers or the debugger halts the core. The Sensor Subsystem also provides an interface to allow an external agent to put the core into a halted state. Note the Watchdog Timer will pause automatically in Probe Mode. The following external sources are capable of halting the



Sensor Subsystem:

- System interrupt event
- JTAG command to halt the Sensor Subsystem
- CPU entering probe mode

The CPU supports a probe mode to facilitate debug. The CPU can enter probe mode due an internal event where a breakpoint is hit or the debugger halts the core. It also provides an interface to allow an external agent to put the core into probe mode. The following external sources are capable of putting the core into probe mode:

- System interrupt event
- JTAG command to halt the CPU
- Sensor Subsystem entering halt state

As outlined above, when the CPU enters probe mode it can put the Sensor Subsystem CPU into a halted state. Also, when Sensor Subsystem enters a halted state, it can put the CPU into probe mode. This is called cross triggering: it allows each core to put the other core into its debug state. There is an enable per direction for cross triggering.

When a cross triggering event occurs, there is some latency between the halting of the cores, but this is expected to be a low number of clock cycles. In the case of the Sensor Subsystem, it will finish external memory transactions or multi-cycle instructions that are committed but have not yet returned their result before entering the halt state. In the case of the CPU, it will finish the current instruction before entering probe mode.

Both cores have low power sleep states. If either core receives a trigger to enter debug mode when it is in its low power state (that is, sleep state for the Sensor Subsystem and C2 state for the CPU), the core is taken out of its lower power mode and enters halt/probe mode state.

Once the cores are in halted/probe mode states, they can only be restarted through a JTAG command.

Note: Both cores cannot be restarted at the same time, as a separate command is required to restart each core.

Note: If the CPU steps through code when the CPU is in probe mode and the Sensor Subsystem has been taken out of the halted state, this causes the Sensor Subsystem to go back into the halted state. If this behavior is not desired, the CPU must be disabled from halting the Sensor Subsystem before stepping through the code.

If the ROM portion of Flash has been programmed, the Sensor Subsystem is blocked from going into halt mode and the CPU is blocked from going into probe mode.