			Init Value			Base FIELD_ID (Hex)	VMM	VMM	L1	VMM Wr Mask Prod.	VMM Wr Mask Debug	L1 Wr Mask
				Size	Fields		Access	Access	Access			
				(Bytes)			Prod.	Debug				
Guest State G	Guest CR0	See the Guest CR0 page	0x00000000000000021	0		1 0x0024000300006800	None	RW	RW	0x00000000000000000	0x0000000008005001F	0x0000000008005001F
	Guest CR3	Checked on write to be a valid private	0	8		1 0x0024000300006802	None	RW	RW	0	-1	-1
		GPA. If LAM is supported by the CPU, bits										
		62 and/or 61 may be 1.										
Guest State G	Guest CR4	See the Guest CR4 page	0x0000000000002040	8		1 0x0024000300006804	None	RW	RW	0x00000000000000000	0x000000011BFF1FBF	0x000000011BFF1FBF
	Guest DR7		0x00000400	8		1 0x002400030000681A	None	RW	RW	0	-1	-1
	Guest RSP		0	8		1 0x002400030000681C	None	RW	RW	0	-1	-1
	Guest RIP		0xFFFFFF0	8		1 0x002400030000681E	None	RW		0	-1	-1 -1
	Guest RFLAGS Guest ES selector		0×00000002	3		1 0x0024000300006820 1 0x0024000100000800	None None	RW RW	RW RW	0	-1 -1	-1
	Guest CS selector		ρ	2		1 0x0024000100000802	None	RW	RW	a	-1	-1
	Guest SS selector		0	2		1 0x0024000100000804	None	RW	RW	0	-1	-1
	Guest DS selector		0	2		1 0x0024000100000806	None	RW	RW	0	-1	-1
	Guest FS selector		0	2		1 0x0024000100000808	None	RW	RW	0	-1	-1
	Guest GS selector		0	2		1 0x002400010000080A	None	RW	RW	0	-1	-1
Guest State G	Guest LDTR selector		0	2		1 0x002400010000080C	None	RW	RW	0	-1	-1
Guest State G	Guest TR selector		0	2		1 0x002400010000080E	None	RW	RW	0	-1	-1
	Guest ES base		0	8		1 0x0024000300006806	None	RW	RW	0	-1	-1
	Guest CS base		0	8		1 0x0024000300006808	None	RW	11.44	0	-1	-1
	Guest SS base		0	8		1 0x002400030000680A	None	RW		0	-1	-1
	Guest DS base		0	8		1 0x002400030000680C	None	RW	RW	0	-1	-1
	Guest FS base		0	8		1 0x002400030000680E	None	RW	RW	0	-1	-1
	Guest GS base		0	8		1 0x0024000300006810 1 0x0024000300006812	None	RW	RW RW	0	-1 -1	-1 -1
	Guest LDTR base		0 0	8		1 0x0024000300006812	None None	RW RW	RW	9	-1	-1
	Guest TR base Guest GDTR base		ρ	0		1 0x0024000300006816	None	RW		0	-1	-1
	Guest IDTR base		9	8		1 0x0024000300006818	None	RW	RW	a	-1	-1
	Guest ES limit		0xfffffff	4		1 0x0024000200004800	None	RW	RW	0	-1	-1
	Guest CS limit		0xFFFFFFF	4		1 0x0024000200004802	None	RW	RW	0	-1	-1
	Guest SS limit		0xFFFFFFF	4		1 0x0024000200004804	None	RW	RW	0	-1	-1
	Guest DS limit		0xFFFFFFF	4		1 0x0024000200004806	None	RW	RW	0	-1	-1
Guest State G	Guest FS limit		0xFFFFFFF	4		1 0x0024000200004808	None	RW	RW	0	-1	-1
	Guest GS limit		0xFFFFFFF	4		1 0x002400020000480A	None	RW	RW	0	-1	-1
	Guest LDTR limit		0x0000FFFF	4		1 0x002400020000480C	None	RW	RW	0	-1	-1
	Guest TR limit		0x0000FFFF	4		1 0x002400020000480E	None	RW	11.44	0	-1	-1
	Guest GDTR limit		0x0000FFFF	4		1 0x0024000200004810	None	RW		0	-1	-1
	Guest IDTR limit		0.0000000	4		1 0x0024000200004812	None	RW	RW	0	-1 -1	-1
Guest State G	Guest ES access rights		0x0000C093	4		1 0x0024000200004814	None	RW	RW	0	-1	-1
			(Data, RW, Accessed, DPL=0, Present, 32b, 4KB granularity)									
Guest State G	Guest CS access rights		0x0000C09B	4		1 0x0024000200004816	None	RW	RW	0	-1	-1
dest state	aucst es access rights		(Code, RX, Accessed, DPL=0, Present, 32b)	7		1 0.002 10002000 1020	None	1000			-	-
Guest State G	Guest SS access rights		0x0000C093	4		1 0x0024000200004818	None	RW	RW	0	-1	-1
	· · · · · · · · · · · · · · · · · · ·		(Data, RW, Accessed, DPL=0, Present, 32b, 4KB									
			granularity)									
Guest State G	Guest DS access rights		0x0000C093	4		1 0x002400020000481A	None	RW	RW	0	-1	-1
			(Data, RW, Accessed, DPL=0, Present, 32b, 4KB									
			granularity)									
Guest State G	Guest FS access rights		0x0000C093	4		1 0x002400020000481C	None	RW	RW	0	-1	-1
			(Data, RW, Accessed, DPL=0, Present, 32b, 4KB									
S 61-14-	Ct CC		granularity)			4 00024000200004045	Nere	DVA	DIM	0	4	
Guest State G	Guest GS access rights		0x0000C093	4		1 0x002400020000481E	None	RW	RW	0	-1	-1
			(Data, RW, Accessed, DPL=0, Present, 32b, 4KB granularity)		l				1			1
Guest State G	Guest LDTR access rights		0x00010082	1	1	1 0x0024000200004820	None	RW	RW	0	-1	-1
ucsi state	Gacat Fo IV acress Highly		(LDT, Present, 32b, 1B granularity, Unusable)	4	l	100024000200004020	None	1// 4/	1,000	ľ	-	1-
			, , , , , , , , , , , , , , , , , , ,		l				1			1
Guest State G	Guest TR access rights		0x0000008B	4		1 0x0024000200004822	None	RW	RW	0	-1	-1
			(32b TSS, Busy, Present, 32b, 1B granularity)		l		1		1			1
			, , , , , , , , , , , , , , , , , , , ,		l				1			1
Guest State G	Guest SMBASE		0	4		1 0x0024000200004828	None	None	None	0	0	0

	1				1			1	1		
Guest State	IA32_DEBUGCTL	• Reserved bits 63:16 and 5:3 must be 0	0	8	1 0x0024000300002802	None	RW	RW	0	0xFFC7	0xFFC7
		• Bit 13 is 0 on read and ignored on write									
		• Bits 7:6 must not be set to 01									
Guest State	IA32_SYSENTER_CS		0	4	1 0x002400020000482A	None	RW	11.44	0	-1	-1
Guest State	IA32_SYSENTER_ESP		0	8	1 0x0024000300006824	None	RW	RW	0	-1	-1
Guest State	IA32_SYSENTER_EIP		0	8	1 0x0024000300006826	None	RW	RW	0	-1	-1
Guest State	IA32_PERF_GLOBAL_CTRL		If (ATTRIBUTES.PERFMON)	8	1 0x0024000300002808	None	RW	RW	0	-1	-1
			0x00000000_000000FF								
			• EN_PMCx (bits 0 to (NUM_PMC - 1)) = 1								
			• Other bits = 0								
			Else								
			0x0000001_00000000								
			• EN_FC0 (bit 32) = 1								
			• Other bits = 0								
Guest State	IA32_PAT		0x0007040600070406	8	1 0x0024000300002804	None	RW	RW	0	-1	-1
Guest State	IA32_EFER		0x901	8	1 0x0024000300002806	None	RW	RW	0	-1	0×0000000000000501
			• SCE (bit 0) is set to 1.								
			• LME (bit 8) is set to 1.								
			• NXE (bit 11) is set to 1.								
			<ul> <li>All other bits are cleared to 0.</li> </ul>								
Guest State	GUEST_IA32_S_CET		0	8	1 0x0024000300006828	None	RW	RW	0	-1	-1
Guest State	GUEST_SSP		0	8	1 0x002400030000682A	None	RW	RW	0	-1	-1
Guest State	GUEST_IA32_INTERRUPT_		0	8	1 0x002400030000682C	None	RW	RW	0	-1	-1
	SSP_TABLE_ADDR										
Guest State	IA32 RTIT CTL		0	8	1 0x0024000300002814	None	RW	RW	0	-1	-1
Guest State	IA32 LBR CTL		0	8	1 0x0024000300002816	None	RW	RW	0	-1	-1
Guest State	IA32 GUEST PKRS		0	8	1 0x0024000300002818	None	RW	RW	0	-1	-1
Guest State	IA32 FRED CONFIG		0	8	1 0x002400030000281A	None	RW	RW	0	-1	-1
Guest State	IA32 FRED RSP1		0	8	1 0x002400030000281C	None	RW	RW	0	-1	-1
Guest State	IA32 FRED RSP2		0	8	1 0x002400030000281E	None	RW	RW	0	-1	-1
Guest State	IA32 FRED RSP3		0	8	1 0x0024000300002820	None	RW	RW	0	-1	-1
Guest State	IA32 FRED STKLVLS		0	8	1 0x0024000300002822	None	RW	RW	0	-1	-1
Guest State	IA32 FRED SSP1		0	8	1 0x0024000300002824	None	RW	RW	0	-1	-1
Guest State	IA32 FRED SSP2		0	8	1 0x0024000300002826	None	RW	RW	0	-1	-1
Guest State	IA32 FRED SSP3		0	8	1 0x0024000300002828	None	RW	RW	0	-1	-1
Guest State	Activity State	Saved/restored on VM exit/entry	Active (0)	4	1 0x0024000200004826	None	RO	RO	0	0	0
Guest State	Interruptibility State	Saved/restored on VM exit/entry	0	4	1 0x0024000200004824	None	RW	RW	0	-1	-1
Guest State		Saved/restored on VM exit/entry	0	8	1 0x0024000300006822	None	RW	RW	0	-1	-1
		ŕ									
Guest State	VMCS Link Pointer		NULL PA (-1)	8	1 0x0024000300002800	None	None	None	0	0	0
Guest State	VMX-Preemption Timer	VMX-preemption timer is used by the TDX	0	4	1 0x002400020000482E	None	RW	None	0	-1	0
	Value	module									
Guest State	PDPTEn		NULL_PA (-1)	8	4 0x002400030000280A	None	RO	RW	0	0	-1
Guest State	Guest Interrupt Status	Includes RVI (lower byte) and SVI (upper	0	2	1 0x0024000100000810	None	RW	RW	0	-1	-1
		byte): saved/restored on VM exit/entry		-							
Guest State	PML Index		0	2	1 0x0024000100000812	None	RW	None	0	-1	0
Guest State	Guest UINV		0	2	1 0x0024000100000814	None	RW	RW	0	-1	-1
Host State	Host RIP	Set to the Intel TDX module's entry point		8	1 0x0024000300006C16	None	None	None	0	0	0
		for VM entry. Updated after TD-preserving		-		1		1		1	1
		updates, on the first entry to this L2 VM.									
		· · · · · · · · · · · · · · · · · · ·				1					
Host State	Host RSP	Different value per LP. Updated after		8	1 0x0024000300006C14	None	None	None	0	0	0
	nose noi	VCPU-to-LP association and after TDX		٦	1	. 40110	. 10110	.,,	_	Ī	1
		module TD-preserving updates, on the first									
		entry to this L2 VM.									
Host State	HOST_SSP	Different value per LP. Updated after		8	1 0x0024000300006C1A	None	None	None	a	a	la
nost state	11031_335	VCPU-to-LP association and after TDX		o	I CASSETOUS SUCCESA	140116	140116	None	ľ	Ĭ	Ĭ
		module TD-preserving updates, on the first				1					1
		entry to this L2 VM.									
<u> </u>	1					-			ı	L .	_ l

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Host State	Host GS Base	Different value per LP. Updated after VCPU-to-LP association and after TDX		8	1 0x0024000300006C08	None	None	None	О	0	О
		module TD-preserving updates, on the first									
		entry to this L2 VM.									
VM-Execution	Pin-Based VM-Exection	See Pin-Based Exec Controls table		4	1 0x0024000200004000	None	RO	RO	0x00000000	0x00000000	0x00000000
Controls	Controls										
	Primary Processor-Based	See Primary Processor-Based Exec Controls		4	1 0x0024000200004002	None	RW	RW	0×00000000	0x69999A04	0x48D99A04
Controls	VM-Exection Controls	table									
	Secondary Processor-	See Secondary Processor-Based Exec Controls table		4	1 0x002400020000401E	RW	RW	RW	0xC0000000	0xC0130C04	0x0C513E0C
Controls	Based VM-Exection Controls	CONTROLS CADLE									
VM-Execution	Tertiary Processor-Based	See Tertiary Processor-Based Exec Controls		8	1 0x0024000300002034	None	RW	RW	0x00000000000000000	0x0000000000000000001	0×0000000000000000
Controls	VM-Exection Controls	table		Ĭ	2 0,002 10003000203 1				0.0000000000000000000000000000000000000	0.0000000000000000000000000000000000000	UNCOUCCUST OF THE PROPERTY OF
VM-Execution	APIC-access address		NULL_PA (-1)	8	1 0x0024000300002014	None	RO	RO	0	0	0
Controls											
VM-Execution	Virtual-APIC address	L1 read and write access is to	NULL_PA (-1)	8	1 0x0024000300002012	None	RO	RW	0	0	0xFFFFFFFFFFF000
Controls		TDVPS.L2_VAPIC_GPA. On write, TDVPS.L2 VAPIC HPA is nullified. The TDX									
		module translates L2 VAPIC GPA to									
		L2 VAPIC HPA on demand.									
VM-Execution	TPR threshold		0	4	1 0x002400020000401C	None	RO	RW	0	0	-1
Controls											
	EOI-exit bitmap n		0	8	4 0x002400030000201C	None	RO	RW	0	0	-1
Controls											
	Posted-interrupt	Posting interrupts to L2 is not supported	0xFFFF	2	1 0x0024000100000002	RO	RO	RO	0	0	0
Controls	notification vector	Posting interrupts to L2 is not supported	NULL PA (-1)		1 0x0024000300002016	RO	RO	RO	0	0	9
VM-Execution Controls	Posted-interrupt descriptor address	Posting interrupts to L2 is not supported	NOLL_PA (-1)	8	1 000024000300002016	RO	KU	KU	Ø	0	О
	EPTP	See EPTP table	See EPTP table	8	1 0x002400030000201A	RO	RW	RW	0x00000000000000000	0x000000000000000000000000000000000000	0x00000000000000000000
Controls											
VM-Execution	Shared EPTP	See Shared EPTP table	See Shared EPTP table	8	1 0x002400030000203C	RW	RW	None	0x000FFFFFFFFF000	0x000FFFFFFFFF000	0x00000000000000000
Controls											
	CR0 Guest/Host Mask	Actual value is calculated by the TDX module from the TD VMCS' CR0 Guest/Host	0xfffffffffffff	8	1 0x0024000300006000	None	RO	RW	Ø	0	-1
Controls		Mask and the value written by the L1 VMM									
VM-Execution	CR0 Read Shadow	Actual value is calculated by the TDX	0x00000000000000021	8	1 0x0024000300006004	None	RO	RW	0	0	-1
Controls		module from the TD VMCS' CR0 Read Shadow									
		and the value written by the L1 VMM									
VM-Execution	CR4 Guest/Host Mask	Actual value is calculated by the TDX	0xFFFFFFFFFFFFF		1 0x0024000300006002	None	RO	RW	0	a	-1
Controls	CN4 Guest/ Host Wask	module from the TD VMCS' CR4 Guest/Host	0.211111111111111	٥	1 0000240003000000002	None	NO	NVV	0	0	-1
Controls		Mask and the value written by the L1 VMM									
VM-Execution	CR4 Read Shadow	Actual value is calculated by the TDX	0×0000000000002040	8	1 0x0024000300006006	None	RO	RW	0	0	-1
Controls		module from the TD VMCS' CR4 Read Shadow									
		and the value written by the L1 VMM									
VM-Execution	CR3-Target Values		0	8	4 0x0024000300006008	None	RW	RW	0	-1	-1
Controls				-							
	CR3-Target Count		0	4	1 0x002400020000400A	None	RW	RW	0	-1	-1
Controls											
	Exception Bitmap	• Bit 18 (MCE) is set to 1, even in	0×00040000	4	1 0x0024000200004004	None	RW	RW	0	0xFFFFFFFFFFFFFF	0xFFFFFFFFFFFFFF
Controls		debug mode.  • Other bits are cleared to 0. They may									
		be									
		modified in debug mode.									
VM-Execution	Page-fault error-code	<u> </u>	0	4	1 0x0024000200004006	None	RW	RW	0	-1	-1
Controls	mask						l <sup>*</sup>	1			
	Page-fault error-code		0	4	1 0x0024000200004008	None	RW	RW	0	-1	-1
Controls	match	I	1	1	I	1	1	1	I	I	1

		T								1	
VM-Execution Controls	I/O-Bitmap Address n	Set to NULL_PA (-1): I/O bitmaps execution control is set to 0	NULL_PA (-1)	8 2 0:	x0024000300002000	None	RO	RO	0	0	0
VM-Execution Controls	Time-Stamp Counter Offset		Copied from TDCS.TSC_OFFSET 8	3 1 0	x0024000300002010	RO	RW	None	0	-1	0
VM-Execution Controls	Time-Stamp Counter Multiplier		Copied from TDCS.TSC_MULTIPLIER 8	8 1 0:	x0024000300002032	RO	RW	None	0	-1	0
VM-Execution Controls	MSR-Bitmap Address	The MSR bitmaps page is held as part of TDVPS. This field is set to the PA of that page.	PA (including HKID) of the L2 MSR Bitmaps page (in TDVPS)	8 1 0	x0024000300002004	RO	RO	None	0	0	0
VM-Execution	Executive-VMCS Pointer	N/A	NULL_PA (-1) 8	8 1 0	x002400030000200C	None	None	None	0	0	0
Controls VM-Execution	TD HKID		Copied from TDCS 4	4 1 0:	x0024000200004026	RO	RO	None	0	0	0
Controls VM-Execution Controls	VPID	Unique identifier of the VM in the platform: Bits 1:0: VM index Bits 15:2: TD's HKID	Bits 1:0: VM index 2 Bits 15:2: TD's HKID	2 1 0:	x0024000100000000	None	RO	None	0	0	0
VM-Execution Controls	PLE_GAP	L1 access isrouted to TDVPS.SHADOW_PLE_GAP. On write, value is converted to vative TSC value and stored in L2 VMCS.	9	4 1 0:	x0024000200004020	RO	RW	RW	0	-1	-1
VM-Execution Controls	PLE_Window	L1 access isrouted to TDVPS.SHADOW_PLE_WINDOW. On write, value is converted to vative TSC value and stored in L2 VMCS.	4		x0024000200004022	RO	RW	RW	0	-1	-1
VM-Execution Controls	VM-Function Controls	The Intel TDX module injects a #UD into the TD.	8	1 0:	x0024000300002018	RO	RO	RO	0	0	0
VM-Execution Controls	EPTP-list address	VMFUNC is not supported.	NULL_PA (-1)	8 1 0	x0024000300002024	RO	RO	None	0	0	0
VM-Execution Controls	VMREAD-bitmap address	VMCS shadowing is not supported.	NULL_PA (-1)	1 0:	x0024000300002026	None	RO	None	0	0	0
VM-Execution Controls	VMWRITE-bitmap address	VMCS shadowing is not supported.	NULL_PA (-1) 8	3 1 0:	x0024000300002028	None	RO	None	0	0	0
VM-Execution Controls	ENCLS-Exiting Bitmap		If secondary processor-based exeuction controls' Enable ENCLS Exiting (bit 15) is set to 1, this field is set to all 1's. Else, this field is not initialized.	B 1 0:	x002400030000202E	None	RO	RO	0	0	0
VM-Execution Controls	ENCLV-Exiting Bitmap	If secondary processor-based exeuction controls' Enable ENCLV Exiting (bit 28) is set to 1, this field is set to all 1's - the Intel TDX module injects a #UD into the guest TD. Else, this field is not initialized.	If secondary processor-based exeuction controls' Enable ENCLV Exiting (bit 28) is set to 1, this field is set to all 1's. Else, this field is not initialized.	1 0	x0024000300002036	None	RO	RO	0	0	0
VM-Execution Controls	PML address	Address must be:  • Valid shared physical address (HKID bits encode a shared HKID).  • Aligned on 4KB. See enable PML execution control.	NULL_PA (-1) 8		x002400030000200E	RO	RW	None	0	0xffffffffffff000	0
VM-Execution Controls	Virtualization-exception information address	L1 read and write access is to shadow VE info address (as GPA). The TDX module translates this to HPA on demand. "EPT Violation #VE" control must be 0 if the shadow value of this field is NULL_PA (-1).	NULL_PA (-1)	1 0	x002400030000202A	None	RO	RO	10	0	10
VM-Execution Controls	EPTP index		0 2	2 1 0:	x00240001000000004	None	RO	None	0	0	0
VM-Execution Controls	XSS-Exiting Bitmap		0 8	8 1 0	x002400030000202C	None	RW	RW	0	-1	-1
VM-Execution Controls	low PASID directory		Implementation-dependent 8	B 1 0:	x0024000300002038	None	RO	None	0	0	0
VM-Execution Controls	address high PASID directory address		Implementation-dependent 8	B 1 0:	x002400030000203A	None	RO	None	0	0	0
CONTROIS	auuress			1		l	1	1			

VM-Execution	Instruction Timeout		0	4	1 0x0024000200004024	RW	RW	RO	-1	-1	0
Controls	Control										
VM-Execution	PCONFIG-Exiting Bitmap		-1	8	1 0x002400030000203E	None	RO	None	0	0	0
Controls	III AT a state a		0		1 0x0024000300002040	N	DIA	DIA	0	0x000FFFFFFFFF018	0x000FFFFFFFFF018
VM-Execution Controls	HLAT pointer		8	8	1 000024000300002040	None	RW	RW	Ø	0X000FFFFFFFF618	000001111111111111111111111111111111111
VM-Execution	HLAT prefix size		a	2	1 0x0024000100000006	None	RW	RW	а	-1	-1
Controls	nLAT prefix size		8	2	1 0000240001000000000	None	KVV	KVV	Ø	-1	-1
VM-Execution	IA32 SPEC CTRL mask		Bit 8 (DDPD_U) = 1, other bits = 0	0	1 0x002400030000204A	None	RO	Nana	a	α.	0
Controls	IA32_SPEC_CIRL IIIask		BIC 8 (DDFD_0) = 1, Other bits = 0	٥	1 0X002400030000204A	None	RU	None	Ø	e e	·
VM-Execution	IA32 SPEC_CTRL shadow		None	0	1 0x002400030000204C	None	RO	None	a	a	a
Controls	IA32_3FEC_CTRL STIAUOW		Notice	٥	1 000024000300002040	None	NO	None	o .	· ·	o a
VM-Exit	VM-Exit Controls		See VM-Exit Ctls page	4	1 0x002400020000400C	None	RO	RO	0×00000000	0x00000000	0x00000000
Controls	THE EARL CONCLOSS		see in this eets page		2 0.002 10002000 1000	110110			0,00000000	0.00000000	0.00000000
VM-Exit	Secondary VM-Exit		See VM-Exit Ctls2 page	8	1 0x0024000300002044	None	RO	RO	0x00000000000000000	0x00000000000000000	0x00000000000000000
Controls	Controls		F-8	ŭ		110110					
VM-Exit		Not used	0	4	1 0x002400020000400E	None	RO	None	0	0	0
Controls											
VM-Exit	VM-exit MSR-store	Not used	NULL_PA (-1)	8	1 0x0024000300002006	None	RO	None	0	0	0
Controls	address										
VM-Exit	VM-exit MSR-load count	Not used	0	4	1 0x0024000200004010	None	RO	None	0	0	0
Controls											
VM-Exit	VM-exit MSR-load address	Not used	NULL_PA (-1)	8	1 0x0024000300002008	None	RO	None	0	0	0
Controls											
VM-Entry	VM-Entry Controls		See VM-Entry Controls table	4	1 0x0024000200004012	None	RO	RW	0x00000000	0x00000000	0x00000200
Controls											
VM-Entry	VM-entry MSR-load count	Not used	0	4	1 0x0024000200004014	None	RO	None	0	0	0
Controls											
VM-Entry	VM-entry MSR-load	Not used	NULL_PA (-1)	8	1 0x002400030000200A	None	RO	None	0	0	0
Controls	address								_	_	
VM-Entry	VM-entry interruption		N/A	4	1 0x0024000200004016	None	RO	RW	0	0	-1
Controls	information		N/A		1 0x0024000200004018				0	0	-1
VM-Entry	VM-entry exception error code		N/A	4	1 000024000200004018	None	RO	RW	Ø	U	-1
Controls VM-Entry	VM-entry instruction		N/a	4	1 0x002400020000401A	None	RO	RW	ρ	0	-1
Controls	length		11/ 0	4	1 0X002400020000401A	None	NO	IN VV	o .	·	-1
VM-Exit	Exit reason	If the Intel TDX module decides to perform	N/Δ	4	1 0x0024000200004402	None	RO	RW	а	а	-1
Information	LAICTCUSOIT	a TD exit, it returns this in RAX bits	11/6		0.002400020004402	None	illo		o a a a a a a a a a a a a a a a a a a a	o o	1
milor mation		31:0.									
VM-Exit	Exit qualification	If the Intel TDX module decides to perform	N/A	8	1 0x0024000300006400	None	RO	RW	0	0	-1
Information		a TD exit, it returns this in RCX. If the		-							
		exit is due to EPT violation, bits 12-7 of									
		the exit qualification are cleared to 0.									
VM-Exit	Guest-Linear Address		N/A	8	1 0x002400030000640A	None	RO	RW	0	0	-1
Information					<u> </u>						
VM-Exit	Guest-physical Address	If the Intel TDX module decides to perform	N/A	8	1 0x0024000300002400	None	RO	RW	0	0	-1
Information		a TD exit, it returns this in R8. It the					l	ĺ			
		EPT fault was caused by an access attempt									
		to a private page, the Intel TDX module									
		clears bits 11:0 to 0.									
					<u> </u>				_		_
VM-Exit	VM-exit interruption	On asynchronous TD exit, the Intel TDX module returns this in R9. Bits 63:32 are	N/A	4	1 0x0024000200004404	None	RO	RW	0	٧	-1
Information	information										
VAA Fuic	VMA authintermenting	cleared to 0.	N/A	4	1 0,000,400,000,000,440.5	Nacio	DO.	D)A/	9	0	-1
VM-Exit	VM-exit interruption error		N/A	4	1 0x0024000200004406	None	RO	RW	Ø	٥	-1
Information VM-Exit	code		N/A	4	1 0x0024000200004408	Nama	RO	RW	α	a .	-1
Information	IDT-vectoring information		IV/ FI	4	1 070074000700004408	None	KU	r( vv	U	ď	- <del>-</del>
VM-Exit	IDT-vectoring error code		N/A	4	1 0x002400020000440A	None	RO	RW	9	a	-1
Information	io i vectoring error code		,	7		None	WO.	17.44	ľ	ľ	1 -
VM-Exit	VM-exit instruction length		N/A	4	1 0x002400020000440C	None	RO	RW	0	0	-1
Information	care most action length		***		1				-	Ī-	1 -
VM-Exit	VM-exit instruction		N/A	4	1 0x002400020000440E	None	RO	RW	0	0	-1
Information	information			1		1	l <sup></sup>	l			
		1			1	•	•				

VM-Exit	I/O RCX	N/A	8	1	0x0024000300006402	None	RO	RW	0	0	-1
Information											
VM-Exit	I/O RSI	N/A	8	1	0x0024000300006404	None	RO	RW	0	0	-1
Information											
VM-Exit	I/O RDI	N/A	8	1	0x0024000300006406	None	RO	RW	0	0	-1
Information											
VM-Exit	I/O RIP	N/A	8	1	0x0024000300006408	None	RO	RW	0	0	-1
Information											
VM-Exit	VM-instruction error	N/A	4	1	0x0024000200004400	None	RO	RW	0	0	-1
Information											
VM-Exit	VM-exit extended	N/A	8	1	0x0024000300002406	None	RO	RW	0	0	-1
Information	instruction information									1	