Sub-Class	Field	Description	Init Value	Field Size (Bytes)	Num Fields	Base FIELD_ID (Hex)	VMM Access Prod.	VMM Access Debug	VMM Wr Mask Prod.	VMM Wr Mask Debug
Guest State	Guest CR0	Write value is checked for architectural compatibility, platform capability, TDX compatibility and current guest CR4 value.	0x0021 • Bits PE (0) and NE (5) are set to 1. • All other bits are cleared to 0. The initial value is checked for compatibility with fixed-0 and fixed-1 bits according to IA32_VMX_CR0_FIXED* MSRs, except for PG (bit 31) which is allowed to be 0 since the guest TD runs as an unrestricted guest.	8	1	0x0024000300006800	None	RW	0	-1
Guest State	Guest CR3	Checked on write to be a valid private GPA. If LAM is supported by the CPU, bits 62 and/or 61 may be 1.	0	8	1	0x0024000300006802	None	RW	0	-1
Guest State	Guest CR4	Write value is checked for architectural compatibility, platform capability, TDX compatibility and current guest CR0 value.	0x2040 • Bits MCE (6) and VMXE (13) are set to 1 • All other bits are cleared to 0. The initial value is checked for compatibility with fixed-0 and fixed-1 bits according to IA32_VMX_CR4_FIXED* MSRs.	8	1	0x0024000300006804	None	RW	0	-1
Guest State	Guest DR7		0x00000400	8	1	0x002400030000681A	None	RW	0	-1
Guest State	Guest RSP		0	8	1	0x002400030000681C	None	RW	0	-1
Guest State	Guest RIP		0xFFFFFFF0	8	1	0x002400030000681E	None	RW	0	-1
Guest State	Guest RFLAGS		0x00000002	8	1	0x0024000300006820	None	RW	0	-1
Guest State	Guest ES selector		0	2	1	0x0024000100000800	None	RW	0	-1
Guest State	Guest CS selector		0	2	1	0x0024000100000802	None	RW	0	-1
Guest State	Guest SS selector		0	2	1	0x0024000100000804	None	RW	0	-1
Guest State	Guest DS selector		0	2	1	0x0024000100000806	None	RW	0	-1
Guest State	Guest FS selector		0	2	1	0x0024000100000808	None	RW	0	-1
Guest State	Guest GS selector		0	2	1	0x002400010000080A	None	RW	0	-1
Guest State	Guest LDTR selector		0	2	1	0x002400010000080C	None	RW	0	-1
Guest State	Guest TR selector		0	2	1	0x002400010000080E	None	RW	0	-1
Guest State	Guest ES base		0	8	1	0x0024000300006806	None	RW	0	-1
Guest State	Guest CS base		0	8	1	0x0024000300006808	None	RW	0	-1
Guest State	Guest SS base		0	8	1	0x002400030000680A	None	RW	0	-1
Guest State	Guest DS base		0	8	1	0x002400030000680C	None	RW	0	-1
Guest State	Guest FS base		0	8	1	0x002400030000680E	None	RW	0	-1
Guest State	Guest GS base		0	8	1	0x0024000300006810	None	RW	0	-1
Guest State	Guest LDTR base		0	8	1	0x0024000300006812	None	RW	0	-1
Guest State	Guest TR base		0	8	1	0x0024000300006814	None	RW	0	-1
Guest State	Guest GDTR base		0	8	1	0x0024000300006816	None	RW	0	-1
Guest State	Guest IDTR base		0	8	1	0x0024000300006818	None	RW	0	-1
Guest State	Guest ES limit		0xFFFFFFFF	4	1	0x0024000200004800	None	RW	0	-1
Guest State	Guest CS limit		0xFFFFFFFF	4	1	0x0024000200004802	None	RW	0	-1
Guest State	Guest SS limit		0xFFFFFFFF	4	1	0x0024000200004804	None	RW	0	-1
Guest State	Guest DS limit		0xFFFFFFFF	4	1	0x0024000200004806	None	RW	0	-1
Guest State	Guest FS limit		0xFFFFFFFF	4	1	0x0024000200004808	None	RW	0	-1
Guest State	Guest GS limit		0xFFFFFFFF	4	1	0x002400020000480A	None	RW	0	-1
Guest State	Guest LDTR limit		0x0000FFFF	4	1	0x002400020000480C	None	RW	0	-1
Guest State	Guest TR limit		0x0000FFFF	4	1	0x002400020000480E	None	RW	0	-1
Guest State	Guest GDTR limit		0x0000FFFF	4	1	0x0024000200004810	None	RW	0	-1
Guest State	Guest IDTR limit		0	4	1	0x0024000200004812	None	RW	0	-1

Guest State	Guest ES access rights		0x0000C093 (Data, RW, Accessed, DPL=0, Present, 32b, 4KB granularity)	4	1	0x0024000200004814	None	RW	0	-1
Guest State	Guest CS access rights		0x0000C09B (Code, RX, Accessed, DPL=0, Present, 32b)	4	1	0x0024000200004816	None	RW	0	-1
Guest State	Guest SS access rights		0x0000C093 (Data, RW, Accessed, DPL=0, Present, 32b, 4KB granularity)	4	1	0x0024000200004818	None	RW	0	-1
Guest State	Guest DS access rights		0x0000C093 (Data, RW, Accessed, DPL=0, Present, 32b, 4KB granularity)	4	1	0x002400020000481A	None	RW	0	-1
Guest State	Guest FS access rights		0x0000C093 (Data, RW, Accessed, DPL=0, Present, 32b, 4KB granularity)	4	1	0x002400020000481C	None	RW	0	-1
Guest State	Guest GS access rights		0x0000C093 (Data, RW, Accessed, DPL=0, Present, 32b, 4KB granularity)	4	1	0x002400020000481E	None	RW	0	-1
Guest State	Guest LDTR access rights		0x00010082 (LDT, Present, 32b, 1B granularity, Unusable)	4	1	0x0024000200004820	None	RW	0	-1
Guest State	Guest TR access rights		0x0000008B (32b TSS, Busy, Present, 32b, 1B granularity)	4	1	0x0024000200004822	None	RW	0	-1
Guest State	Guest SMBASE		0	4	1	0x0024000200004828	None	None	0	0
Guest State	IA32_DEBUGCTL	• Reserved bits 63:16 and 5:3 must be 0 • Bit 13 is 0 on read and ignored on write • Bits 7:6 must not be set to 01	0	8	1	0x0024000300002802	None	RW	0	0xFFC7
Guest State	IA32_SYSENTER_CS		0	4	1	0x002400020000482A	None	RW	0	-1
Guest State	IA32_SYSENTER_ESP		0	8	1	0x0024000300006824	None	RW	0	-1
Guest State	IA32_SYSENTER_EIP		0	8	1	0x0024000300006826	None	RW	0	-1

Guest State	IA32_PERF_GLOBAL_CTRL		If (ATTRIBUTES.PERFMON)
			0x00000000_000000FF
			• EN_PMCx (bits 0 to (NUM_PMC - 1)) = 1
			• Other bits = 0
			Else
			0x00000001_00000000
			• EN_FC0 (bit 32) = 1
			• Other bits = 0
				8	1	0x0024000300002808	None	RW	0	-1

Guest State	IA32_PAT		0x0007040600070406	8	1	0x0024000300002804	None	RW	0	-1
Guest State	IA32_EFER		0x901 • SCE (bit 0) is set to 1. • LME (bit 8) is set to 1. • NXE (bit 11) is set to 1. • All other bits are cleared to 0.	8	1	0x0024000300002806	None	RW	0	-1
Guest State	GUEST_IA32_S_CET		0	8	1	0x0024000300006828	None	RW	0	-1
Guest State	GUEST_SSP		0	8	1	0x002400030000682A	None	RW	0	-1
Guest State	GUEST_IA32_INTERRUPT_SSP_TABLE_ADDR		0	8	1	0x002400030000682C	None	RW	0	-1
Guest State	IA32_RTIT_CTL		0	8	1	0x0024000300002814	None	RW	0	-1
Guest State	IA32_LBR_CTL		0	8	1	0x0024000300002816	None	RW	0	-1
Guest State	IA32_GUEST_PKRS		0	8	1	0x0024000300002818	None	RW	0	-1
Guest State	IA32_FRED_CONFIG		0	8	1	0x002400030000281A	None	RW	0	-1
Guest State	IA32_FRED_RSP1		0	8	1	0x002400030000281C	None	RW	0	-1
Guest State	IA32_FRED_RSP2		0	8	1	0x002400030000281E	None	RW	0	-1
Guest State	IA32_FRED_RSP3		0	8	1	0x0024000300002820	None	RW	0	-1

Guest State	IA32_FRED_STKLVLS		0	8	1	0x0024000300002822	None	RW	0	-1
Guest State	IA32_FRED_SSP1		0	8	1	0x0024000300002824	None	RW	0	-1
Guest State	IA32_FRED_SSP2		0	8	1	0x0024000300002826	None	RW	0	-1
Guest State	IA32_FRED_SSP3		0	8	1	0x0024000300002828	None	RW	0	-1
Guest State	Activity State	Saved/restored on VM exit/entry	Active (0)	4	1	0x0024000200004826	None	RO	0	0
Guest State	Interruptibility State	Saved/restored on VM exit/entry	0	4	1	0x0024000200004824	None	RW	0	-1
Guest State	Pending Debug Exceptions	Saved/restored on VM exit/entry	0	8	1	0x0024000300006822	None	RW	0	-1
Guest State	VMCS Link Pointer		NULL_PA (-1)	8	1	0x0024000300002800	None	None	0	0
Guest State	VMX-Preemption Timer Value	N/A: VMX-preemption timer is not used by guest TDs.	0	4	1	0x002400020000482E	None	RW	0	-1
Guest State	PDPTEn	N/A: PAE paging is not used by TD guests.	NULL_PA (-1)	8	4	0x002400030000280A	None	RO	0	0
Guest State	Guest Interrupt Status	Includes RVI (lower byte) and SVI (upper byte): saved/restored on VM exit/entry	0	2	1	0x0024000100000810	None	RW	0	-1
Guest State	PML Index		0	2	1	0x0024000100000812	None	RW	0	-1
Guest State	Guest UINV		0	2	1	0x0024000100000814	None	RW	0	-1
Host State	Host RIP	Set to the Intel TDX module's entry point for VM entry. Updated after TDX module TD-preserving updates, on the first entry to L1 VM.		8	1	0x0024000300006C16	None	None	0	0
Host State	Host RSP	Different value per LP. Updated after VCPU-to-LP association and after TDX module TD-preserving updates, on the first entry to L1 VM.		8	1	0x0024000300006C14	None	None	0	0
Host State	HOST_SSP	Different value per LP. Updated after VCPU-to-LP association and after TDX module TD-preserving updates, on the first entry to L1 VM.		8	1	0x0024000300006C1A	None	None	0	0
Host State	Host GS Base	Different value per LP. Updated after VCPU-to-LP association and after TDX module TD-preserving updates, on the first entry to L1 VM.		8	1	0x0024000300006C08	None	None	0	0
VM-Execution Controls	Pin-Based VM-Exection Controls	See Pin-Based Exec Controls table		4	1	0x0024000200004000	RW	RW	0x00000080	0x00000080
VM-Execution Controls	Primary Processor-Based VM-Exection Controls	See Primary Processor-Based Exec Controls table		4	1	0x0024000200004002	None	RW	0x00000000	0x69999A04
VM-Execution Controls	Secondary Processor-Based VM-Exection Controls	See Secondary Processor-Based Exec Controls table		4	1	0x002400020000401E	RW	RW	0xC0000000	0xC0130C04
VM-Execution Controls	Tertiary Processor-Based VM-Exection Controls	See Tertiary Processor-Based Exec Controls table		8	1	0x0024000300002034	None	RW	0x0000000000000000	0x0000000000000001
VM-Execution Controls	APIC-access address		NULL_PA (-1)	8	1	0x0024000300002014	None	RO	0	0
VM-Execution Controls	Virtual-APIC address	On VCPU-to-LP association, set by the Intel TDX module to the address of the VAPIC page in TDVPS, including the TD's ephemeral HKID	Address of the VAPIC page in TDVPS, including the TD's ephemeral HKID	8	1	0x0024000300002012	None	None	0	0
VM-Execution Controls	TPR threshold		0	4	1	0x002400020000401C	None	RO	0	0
VM-Execution Controls	EOI-exit bitmap n		0	8	4	0x002400030000201C	None	RO	0	0

VM-Execution Controls	Posted-interrupt notification vector	TDH.VP.WR checks the value to be in the range 0 to 255. See process posted interrupt pin-based execution control.	0xFFFF	2	1	0x0024000100000002	RW	RW	-1	-1
VM-Execution Controls	Posted-interrupt descriptor address	Address must be: • Valid shared physical address (HKID bits encode a shared HKID). • Aligned on 64B. See process posted interrupt pin-based execution control.	NULL_PA (-1)	8	1	0x0024000300002016	RW	RW	0xFFFFFFFFFFFFFFC0	0xFFFFFFFFFFFFFFC0
VM-Execution Controls	EPTP	See EPTP table	See EPTP table	8	1	0x002400030000201A	RO	RO	0x0000000000000000	0x0000000000000000
VM-Execution Controls	Shared EPTP	See Shared EPTP table	See Shared EPTP table	8	1	0x002400030000203C	RW	RW	0x000FFFFFFFFFF000	0x000FFFFFFFFFF000
VM-Execution Controls	CR0 Guest/Host Mask	Bits 0, 5, 29 and 30 can't be written even in debug mode	The following bits are set to 1, indicating they are owned by the Intel TDX module: • PE (0) • NE (5) • NW (29) • CD (30) • Any bit set to 1 in IA32_VMX_CR0_FIXED0 (i.e., a bit whose value must be 1), except for PG(31) which is set to 0, since the guest TD runs as an unrestricted guest • Any bit set to 0 in IA32_VMX_CR0_FIXED1 (i.e., a bit whose value must be 0) • Bits known to the Intel TDX module as reserved (bits 63-32, 28-19, 17 and 15-6) All other bits are cleared to 0, indicating they are owned by the guest TD.	8	1	0x0024000300006000	None	RW	0	0xFFFFFFFF9FFFFFDE
VM-Execution Controls	CR0 Read Shadow	Bits 0 and 5 can't be written even in debug mode	The following bits are set to 1: • PE (0) • NE (5) • Any bit set to 1 in IA32_VMX_CR0_FIXED0 (i.e., a bit whose value must be 1) All other bits are cleared to 0.	8	1	0x0024000300006004	None	RW	0	0xFFFFFFFFFFFFFFDE
VM-Execution Controls	CR4 Guest/Host Mask	Bits 6, 13 and 14 can't be written even in debug mode	Details are provided in the [ABI Spec]	8	1	0x0024000300006002	None	RW	0	0xFFFFFFFFFFFF9FBF
VM-Execution Controls	CR4 Read Shadow	Bit 6 can't be written even in debug mode	• Bit MCE (6) is set to 1. • Bit VMXE (13) is cleared to 0. • Any other bit whose value is set to 1 in IA32_VMX_CR4_FIXED0 (i.e., a bit whose value must be 1) is set to 1. • All other bits are cleared to 0.	8	1	0x0024000300006006	None	RW	0	0xFFFFFFFFFFFFFFBF
VM-Execution Controls	CR3-Target Values	N/A: The Intel TDX module does not control guest CR3	N/A	8	4	0x0024000300006008	None	RW	0	-1
VM-Execution Controls	CR3-Target Count	Set to 0: Intel TDX module does not control guest CR3	0	4	1	0x002400020000400A	None	RW	0	-1

VM-Execution Controls	Exception Bitmap	• Bit 18 (MCE) is set to 1, even in debug mode. • Other bits are cleared to 0. They may be modified in debug mode.	0x00040000	4	1	0x0024000200004004	None	RW	0	0xFFFFFFFFFFFBFFFF
VM-Execution Controls	Page-fault error-code mask		0	4	1	0x0024000200004006	None	RW	0	-1
VM-Execution Controls	Page-fault error-code match		0	4	1	0x0024000200004008	None	RW	0	-1
VM-Execution Controls	I/O-Bitmap Address n	Set to NULL_PA (-1): I/O bitmaps execution control is set to 0	NULL_PA (-1)	8	2	0x0024000300002000	None	RO	0	0
VM-Execution Controls	Time-Stamp Counter Offset		Copied from TDCS.TSC_OFFSET	8	1	0x0024000300002010	RO	RW	0	-1
VM-Execution Controls	Time-Stamp Counter Multiplier		Copied from TDCS.TSC_MULTIPLIER	8	1	0x0024000300002032	RO	RW	0	-1
VM-Execution Controls	MSR-Bitmap Address	A single MSR bitmaps page is held per TD as part of TDCS. This field is set to the PA of that page.	PA (including HKID) of the TDCS MSR Bitmaps page.	8	1	0x0024000300002004	RO	RO	0	0
VM-Execution Controls	Executive-VMCS Pointer	N/A	NULL_PA (-1)	8	1	0x002400030000200C	None	None	0	0
VM-Execution Controls	TD HKID		Copied from TDCS	4	1	0x0024000200004026	RO	RO	0	0
VM-Execution Controls	VPID	Unique identifier of the VM in the platform: Bits 1:0: VM index (0) Bits 15:2: TD's HKID	Bits 1:0: VM index (0) Bits 15:2: TD's HKID	2	1	0x0024000100000000	None	RO	0	0
VM-Execution Controls	PLE_GAP		0	4	1	0x0024000200004020	RO	RW	0	-1
VM-Execution Controls	PLE_Window		0	4	1	0x0024000200004022	RO	RW	0	-1
VM-Execution Controls	VM-Function Controls	The Intel TDX module injects a #UD into the TD.	0	8	1	0x0024000300002018	RO	RO	0	0
VM-Execution Controls	EPTP-list address	VMFUNC is not supported.	NULL_PA (-1)	8	1	0x0024000300002024	RO	RO	0	0
VM-Execution Controls	VMREAD-bitmap address	VMCS shadowing is not supported.	NULL_PA (-1)	8	1	0x0024000300002026	None	RO	0	0
VM-Execution Controls	VMWRITE-bitmap address	VMCS shadowing is not supported.	NULL_PA (-1)	8	1	0x0024000300002028	None	RO	0	0
VM-Execution Controls	ENCLS-Exiting Bitmap	If secondary processor-based exeuction controls' Enable ENCLS Exiting (bit 15) is set to 1, this field is set to all 1's – the Intel TDX module injects a #UD into the guest TD. Else, this field is not initialized.	If secondary processor-based exeuction controls' Enable ENCLS Exiting (bit 15) is set to 1, this field is set to all 1's. Else, this field is not initialized.	8	1	0x002400030000202E	None	RO	0	0
VM-Execution Controls	ENCLV-Exiting Bitmap	If secondary processor-based exeuction controls' Enable ENCLV Exiting (bit 28) is set to 1, this field is set to all 1's – the Intel TDX module injects a #UD into the guest TD. Else, this field is not initialized.	If secondary processor-based exeuction controls' Enable ENCLV Exiting (bit 28) is set to 1, this field is set to all 1's. Else, this field is not initialized.	8	1	0x0024000300002036	None	RO	0	0
VM-Execution Controls	PML address	Address must be: • Valid shared physical address (HKID bits encode a shared HKID). • Aligned on 4KB. See enable PML execution control.	NULL_PA (-1)	8	1	0x002400030000200E	RO	RW	0	0xFFFFFFFFFFFFF000
VM-Execution Controls	Virtualization-exception information address		Address of the VE Info structure in TDVPS, including the TD's ephemeral HKID	8	1	0x002400030000202A	None	RO	0	0

VM-Execution Controls	EPTP index		0	2	1	0x0024000100000004	None	RO	0	0
VM-Execution Controls	XSS-Exiting Bitmap		0	8	1	0x002400030000202C	None	RW	0	-1
VM-Execution Controls	low PASID directory address		Implementation-dependent	8	1	0x0024000300002038	None	RO	0	0
VM-Execution Controls	high PASID directory address		Implementation-dependent	8	1	0x002400030000203A	None	RO	0	0
VM-Execution Controls	Instruction Timeout Control		0	4	1	0x0024000200004024	RW	RW	-1	-1
VM-Execution Controls	PCONFIG-Exiting Bitmap		-1	8	1	0x002400030000203E	None	RO	0	0
VM-Execution Controls	HLAT pointer		0	8	1	0x0024000300002040	None	RO	0	0
VM-Execution Controls	HLAT prefix size		0	2	1	0x0024000100000006	None	RO	0	0
VM-Execution Controls	IA32_SPEC_CTRL mask		Bit 8 (DDPD_U) = 1, other bits = 0	8	1	0x002400030000204A	None	RO	0	0
VM-Execution Controls	IA32_SPEC_CTRL shadow		None	8	1	0x002400030000204C	None	RO	0	0
VM-Exit Controls	VM-Exit Controls		See VM-Exit Ctls page	4	1	0x002400020000400C	None	RO	0x00000000	0x00000000
VM-Exit Controls	Secondary VM-Exit Controls		See VM-Exit Ctls2 page	8	1	0x0024000300002044	None	RO	0x0000000000000000	0x0000000000000000
VM-Exit Controls	VM-exit MSR-store count	Not used	0	4	1	0x002400020000400E	None	RO	0	0
VM-Exit Controls	VM-exit MSR-store address	Not used	NULL_PA (-1)	8	1	0x0024000300002006	None	RO	0	0
VM-Exit Controls	VM-exit MSR-load count	Not used	0	4	1	0x0024000200004010	None	RO	0	0
VM-Exit Controls	VM-exit MSR-load address	Not used	NULL_PA (-1)	8	1	0x0024000300002008	None	RO	0	0
VM-Entry Controls	VM-Entry Controls		See VM-Entry Ctls page	4	1	0x0024000200004012	None	RO	0x00000000	0x00000000
VM-Entry Controls	VM-entry MSR-load count	Not used	0	4	1	0x0024000200004014	None	RO	0	0
VM-Entry Controls	VM-entry MSR-load address	Not used	NULL_PA (-1)	8	1	0x002400030000200A	None	RO	0	0
VM-Entry Controls	VM-entry interruption information		N/A	4	1	0x0024000200004016	None	RO	0	0
VM-Entry Controls	VM-entry exception error code		N/A	4	1	0x0024000200004018	None	RO	0	0
VM-Entry Controls	VM-entry instruction length		N/a	4	1	0x002400020000401A	None	RO	0	0
VM-Exit Information	Exit reason	If the Intel TDX module decides to perform a TD exit, it returns this in RAX bits 31:0. Bit 27 (enclave mode) is not set. Bit 28 (Pending MTF VM exit) is not set. Bit 29 (VM exit from VMX root operation) is not set. Bit 31 (VM-entry failure) is not set.	N/A	4	1	0x0024000200004402	None	RO	0	0
VM-Exit Information	Exit qualification	If the Intel TDX module decides to perform a TD exit, it returns this in RCX. If the exit is due to EPT violation, bits 12-7 of the exit qualification are cleared to 0.	N/A	8	1	0x0024000300006400	None	RO	0	0

VM-Exit Information	Guest-Linear Address		N/A	8	1	0x0024000030000640A	None	RO	0	0
VM-Exit Information	Guest-physical Address	If the Intel TDX module decides to perform a TD exit, it returns this in R8. It the EPT fault was caused by an access attempt to a private page, the Intel TDX module clears bits 11:0 to 0.	N/A	8	1	0x0024000300002400	None	RO	0	0
VM-Exit Information	VM-exit interruption information	On asynchronous TD exit, the Intel TDX module returns this in R9. Bits 63:32 are cleared to 0.	N/A	4	1	0x0024000200004404	None	RO	0	0
VM-Exit Information	VM-exit interruption error code		N/A	4	1	0x0024000200004406	None	RO	0	0
VM-Exit Information	IDT-vectoring information		N/A	4	1	0x0024000200004408	None	RO	0	0
VM-Exit Information	IDT-vectoring error code		N/A	4	1	0x002400020000440A	None	RO	0	0
VM-Exit Information	VM-exit instruction length		N/A	4	1	0x002400020000440C	None	RO	0	0
VM-Exit Information	VM-exit instruction information		N/A	4	1	0x002400020000440E	None	RO	0	0
VM-Exit Information	I/O RCX		N/A	8	1	0x0024000300006402	None	RO	0	0
VM-Exit Information	I/O RSI		N/A	8	1	0x0024000300006404	None	RO	0	0
VM-Exit Information	I/O RDI		N/A	8	1	0x0024000300006406	None	RO	0	0
VM-Exit Information	I/O RIP		N/A	8	1	0x0024000300006408	None	RO	0	0
VM-Exit Information	VM-instruction error		N/A	4	1	0x0024000200004400	None	RO	0	0
VM-Exit Information	VM-exit extended instruction information		N/A	8	1	0x0024000300002406	None	RO	0	0