



AMD Processor Recognition

Application Note

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Contents

| | | |
|------------------|--|-----------|
| Chapter 1 | Introduction | 15 |
| Chapter 2 | CPUID Instruction Overview | 17 |
| Chapter 3 | Using CPUID Instructions | 19 |
| 3.1 | Testing for the CPUID Instruction | 19 |
| 3.1.1 | Illegal Instruction Exception Method | 19 |
| 3.1.2 | EFLAGS ID-Bit Method | 19 |
| 3.2 | Using CPUID Functions | 20 |
| 3.3 | Identifying the Processor Vendor | 23 |
| 3.4 | Testing For Extended Functions | 24 |
| 3.5 | Determining the Processor Signature | 24 |
| 3.6 | Identifying Supported Features | 26 |
| 3.6.1 | Determining Instruction Set Support | 26 |
| 3.6.2 | AMD Processor Signature (Extended Function) | 28 |
| 3.6.3 | Displaying the Processor Name | 28 |
| 3.6.3.1 | Differentiation of Processors of the Same Model Number | 29 |
| 3.6.3.2 | S3 State Considerations | 29 |
| 3.6.3.3 | Recommended Name String | 29 |
| 3.6.4 | Displaying Cache Information | 34 |
| 3.6.5 | Determining Power Management Capabilities | 34 |
| 3.6.6 | Determining Maximum Physical and Linear Address Size | 34 |
| 3.6.7 | Determining Vendor-Specific Feature Flags | 34 |
| 3.7 | Code Samples | 34 |
| 3.7.1 | Example CPUID Code | 35 |
| 3.7.2 | Example Function Call | 42 |
| 3.7.3 | Displaying the AMD Athlon™ 64, AMD Opteron™, AMD Athlon™, and AMD Duron™ Processor Name Strings | 43 |
| 3.7.4 | DisplayNameString Subroutine | 43 |
| 3.7.5 | DisplayNameSubstring | 44 |
| Chapter 4 | Summary of CPUID Differences | 47 |
| 4.1 | Changed Functions | 47 |

- 4.1.1 Standard Function 0000_0001h—Processor Version Information and Feature Flags47
 - 4.1.1.1 Extended Family and Extended Model (in EAX)47
 - 4.1.1.2 8-Bit Brand ID (in EBX)47
 - 4.1.1.3 CLFLUSH size (in EBX)47
 - 4.1.1.4 Initial APIC_ID (in EBX)48
 - 4.1.1.5 Standard Feature Flags (in EDX)48
- 4.1.2 Extended Function 8000_0000h—Highest Extended Function Available . . .48
- 4.1.3 Extended Function 8000_0001h—Processor Version Information and Extended Feature Flags48
 - 4.1.3.1 Extended Family and Extended Model (in EAX)48
 - 4.1.3.2 12-Bit Brand ID (in EBX)48
 - 4.1.3.3 Extended Feature Flags (in EDX)48
- 4.1.4 Extended Functions 8000_0005h and 8000_0006h—Cache and TLB Information49
- 4.1.5 Extended Function 8000_0007h—Advanced Power Management Information49
- 4.1.6 Extended Function 8000_0008h—Address Size Information49
- 4.2 New Functions49
 - 4.2.1 Extended Functions 8000_0009h–8000_0018h—Vendor-Specific Feature Flags49
- Chapter 5 CPUID Instruction Definition51**
 - 5.1 CPUID Instruction51
 - 5.2 Standard Functions52
 - 5.2.1 Function 0—Largest Standard Function Input Value and Vendor Identification String52
 - 5.2.2 Function 1—Processor Signature and Standard Feature Flags52
 - 5.2.2.1 EAX—Version (Family, Model and Stepping) Information53
 - 5.2.2.2 EBX—8-Bit Brand ID, CFLUSH, and APIC Information53
 - 5.2.2.2.1 8-Bit Brand ID54
 - 5.2.2.2.2 CLFLUSH Size54
 - 5.2.2.2.3 Initial APIC_ID54
 - 5.2.2.3 EDX—Standard Feature Flags55
 - 5.3 Extended Functions60
 - 5.3.1 Function 8000_0000h—Largest Extended Function Input Value60
 - 5.3.2 Function 8000_0001h—Processor Version Information and

| | | |
|-------------------|--|-----------|
| | Extended Feature Flags | 60 |
| 5.3.2.1 | EAX—Version (Family, Model, and Stepping) Information | 60 |
| 5.3.2.2 | EBX—12-bit Brand ID | 61 |
| 5.3.2.3 | ECX—Extended Feature Flag | 61 |
| 5.3.2.4 | EDX—Extended Feature Flags | 61 |
| 5.3.3 | Extended Functions 8000_0002h, 8000_0003h, and 8000_0004h—Processor Name String | 69 |
| 5.3.4 | Extended Function 8000_0005h—L1 Cache and L1 TLB Information for AMD Athlon™ 64, AMD Opteron™, AMD Athlon™, and AMD Duron™ Processors | 70 |
| 5.3.5 | Function 8000_0005h—L1 Cache Information for AMD-K5 and All AMD-K6® Processors | 71 |
| 5.3.6 | Extended Function 8000_0006h—L2 Cache and L2 TLB Information for the AMD Athlon™ 64 and AMD Opteron™, AMD Athlon™, and AMD Duron™ Processors | 72 |
| 5.3.7 | Function 8000_0006h—L2 Cache Information for the AMD-K6®-III Processor | 74 |
| 5.3.7.1 | Associativity Field Definitions | 74 |
| 5.3.7.1.1 | Associativity for L1 Caches and L1 TLBs | 74 |
| 5.3.7.1.2 | Associativity for L2 Caches and L2 TLBs | 74 |
| 5.3.8 | Function 8000_0007h — Advanced Power Management Feature Flags ... | 75 |
| 5.3.9 | Function 8000_0008h — Physical Address and Linear Address Size | 76 |
| 5.3.10 | Extended Functions 8000_0009h–8000_0018h—Vendor-Specific Feature Flags | 77 |
| Appendix A | Register Values Returned by the AMD Family Processors | 79 |
| A.1 | AMD Athlon™ 64 and AMD Opteron™ Processor Values | 79 |
| A.2 | AMD Athlon™ Processor and AMD Duron™ Processor Values | 83 |
| A.3 | AMD-K6® Processor Values | 91 |
| A.4 | Am486®, Am5x86, and AMD-K5 Processor Values | 93 |
| Appendix B | Programming the Name String of the AMD Athlon™ 64 and AMD Opteron™ Processors | 95 |
| B.1 | Brand ID | 95 |
| B.2 | Constructing the Name String | 96 |
| B.3 | Programming the Processor Name String | 97 |

List of Figures

| | | |
|-----------|---|----|
| Figure 1. | Contents of EAX Register Returned by Function 1 and 8000_0001h | 24 |
| Figure 2. | EAX Bit Fields for Standard Function 0000_0001h and Extended Function 8000_0001h | 53 |
| Figure 3. | EBX Bit Fields for Standard Function 0000_0001h. | 54 |
| Figure 4. | EDX Bit Fields for Extended Function 8000_0007h | 76 |
| Figure 5. | EAX Bit Fields for Extended Function 8000_0008h | 77 |

List of Tables

| | | |
|-----------|---|----|
| Table 1. | Summary of CPUID Functions for the AMD Athlon™ 64 and AMD Opteron™ Processor. | 21 |
| Table 2. | Summary of CPUID Functions in AMD Athlon™ and AMD Duron™ Processors . . . | 22 |
| Table 3. | Summary of CPUID Functions in AMD Processors. | 23 |
| Table 4. | Summary of Processor Signatures for AMD Processors | 25 |
| Table 5. | Recommended Name String by Platform Segment for AMD Athlon™ and AMD Duron™ Family of Processors Models 6 and Above. | 30 |
| Table 6. | Processor Name Strings for AMD Athlon™ and AMD Duron™ Family of Processors Through Model 4 | 31 |
| Table 7. | Model Number Mappings for AMD Athlon™ Family of Processors with 256-Kbyte L2 Cache. | 32 |
| Table 8. | Model Number Mappings for AMD Athlon™ Family Processors with 512-Kbyte L2 Cache. | 33 |
| Table 9. | Initial APIC_ID Bit Definitions | 55 |
| Table 10. | Standard Feature Flag Descriptions for AMD Athlon™ 64 and AMD Opteron™ Processors | 55 |
| Table 11. | Standard Feature Flag Descriptions for AMD Athlon™ Processors | 57 |
| Table 12. | Standard Feature Flag Descriptions for AMD Duron™ Processors. | 58 |
| Table 13. | Standard Feature Flag Descriptions for AMD-K6®-2 and AMD-K6®-III Processors .59 | |
| Table 14. | Extended Feature Flags—AMD Athlon™ 64 and AMD Opteron™ Processors | 62 |
| Table 15. | Extended Feature Flag Descriptions for AMD Athlon™ Processors. | 64 |
| Table 16. | Extended Feature Flag Descriptions for AMD Duron™ Processors | 66 |
| Table 17. | Extended Feature Flag Descriptions for AMD-K6®-2 and AMD-K6®-III Processors .68 | |
| Table 18. | Standard Feature Flags Versus Extended Feature Flags. | 69 |
| Table 19. | EAX Format Returned by Function 8000_0005h. | 70 |
| Table 21. | ECX Format Returned by Function 8000_0005h. | 71 |
| Table 22. | EDX Format Returned by Function 8000_0005h. | 71 |
| Table 20. | EBX Format Returned by Function 8000_0005h. | 71 |
| Table 23. | EBX Format Returned by Function 8000_0005h. | 72 |
| Table 24. | ECX Format Returned by Function 8000_0005h. | 72 |

| | | |
|-----------|---|----|
| Table 25. | EDX Format Returned by Function 8000_0005h..... | 72 |
| Table 26. | EAX Format Returned by Function 8000_0006h..... | 73 |
| Table 27. | EBX Format Returned by Function 8000_0006h..... | 73 |
| Table 28. | ECX Format Returned by Function 8000_0006h..... | 73 |
| Table 29. | ECX Format Returned by Function 8000_0006h for the AMD-K6 [®] -III Processor ... | 74 |
| Table 30. | Associativity Values For L2 Caches and TLBs | 74 |
| Table 31. | Values Returned by the AMD Athlon™ 64 and AMD Opteron™ Processors | 79 |
| Table 32. | Values Returned by AMD Athlon™ and AMD Duron™ Processors Models 6 and Higher..... | 83 |
| Table 33. | Values Returned by Mobile AMD Athlon™ Processors Models 6 Higher, and Mobile AMD Duron™ Processors Models 3, 6, and 7 | 86 |
| Table 34. | Values Returned by AMD Athlon™ Processors Models 1, 2, and 4, and AMD Duron™ Processors Model 3 | 89 |
| Table 35. | Values Returned by AMD-K6 [®] Processors | 91 |
| Table 36. | Values Returned by Am486 [®] , Am5 _x 86, and AMD-K5 Processors | 93 |
| Table 37. | Processor Name String Values for AMD Athlon™ 64 and AMD Opteron™ Processors..... | 96 |

Revision History

| Date | Revision | Description |
|----------------|----------|--|
| September 2003 | 3.04 | Incorporated additional AMD Athlon™ 64, AMD Athlon™ 64 FX, and AMD Opteron™ CPUID feature identification and branding information. |
| August 2003 | 3.03 | Incorporated additional AMD Athlon™ 64 branding information. |
| June 2003 | 3.02 | Added AMD Athlon 64 information and made minor corrections. |
| May 2003 | 3.01 | Added 3000+ and 3200+ models to table 8. |
| April 2003 | 3.00 | Added content for the AMD Opteron™ processor. Changed to new AMD technical document format, which includes new look and feel as well as new revision system. |
| November 2002 | W-1 | Revised Table 12 in Appendix A |
| November 2002 | W | Revised Table 7: Added additional model numbers — 2600+, a 2700+, and a 2800+ |
| August 2002 | V | Added 2400+ and 2600+ models to table 4. |
| August 2002 | U | Added AMD Athlon™ processor model 8 information to the following: Table 2, “Summary of CPUID Functions in AMD Athlon™ and AMD Duron™ Processors” Table 3, “Summary of Processor Signatures for AMD Processors,” on page 9 Table 6, “Recommended Name String by Platform Segment for AMD Athlon™ and AMD Duron™ Family of Processors Models 6 and Above,” on page 15 Table 7, “Model Number Mappings for AMD Athlon™ Family of Processors,” on page 16 Table 9, “Standard Feature Flag Descriptions for the AMD Athlon™ Processors” Table 12, “Extended Feature Flag Descriptions for AMD Athlon™ Processors” Table 26, “Values Returned By the AMD Athlon™ and AMD Duron™ Processors models 6 and 7, and 8” |

| Date | Revision | Description |
|--------------|----------|---|
| January 2002 | T | <p>Added the following:</p> <ul style="list-style-type: none"> “Name String Supports up to 48 Characters” on page 14 “Differentiation of Processors of the Same Model Number” on page 14 “S3 State Considerations” on page 14 “Recommended Name String” on page 14 Table 5, “Processor Name Strings for AMD Athlon™ and AMD Duron™ Family of Processors Through Model 4,” on page 14 <p>Revised the following:</p> <ul style="list-style-type: none"> Table 2, “Summary of CPUID Functions in AMD Athlon™ and AMD Duron™ Processors,” on page 6 “Testing For Extended Functions” on page 7 Table 3, “Summary of Processor Signatures for AMD Processors,” on page 8 Table 4, “Summary of Standard and Extended Feature Bits,” on page 10 Table 6, “Recommended Name String by Platform Segment for AMD Athlon™ and AMD Duron™ Family of Processors Models 6 and Above,” on page 16 Table 7, “Model Number Mappings for AMD Athlon™ Family of Processors,” on page 17 Table 9, “Standard Feature Flag Descriptions for the AMD Athlon™ Processors,” on page 35 Table 10, “Standard Feature Flag Descriptions for the AMD Duron™ Processors,” on page 36 Table 12, “Extended Feature Flag Descriptions for AMD Athlon™ Processors,” on page 39 Table 13, “Extended Feature Flag Descriptions for AMD Duron™ Processors,” on page 41 Table 26, “Values Returned By the AMD Athlon™ and AMD Duron™ Processors Models 6 and 7,” on page 52 Table 27, “Values Returned by the Mobile AMD Athlon™ Processors Models 6, 7, and 8, and the Mobile AMD Duron™ Processors Models 3, 6, and 7,” on page 55 |
| July 2001 | S | <p>Added information about the mobile AMD Athlon™ 4 processor, the AMD Athlon™ MP processor, and the mobile AMD Duron™ processors.</p> |
| June 2000 | R | <p>Added information about the AMD Duron™ processor throughout the document.</p> <p>Revised “CPUID Instruction Overview” on page 3.</p> <p>Added “The AMD Duron™ Processor” on page 2.</p> <p>Added Table 5, “Processor Name Strings for the AMD Duron™ Processor,” on page 13.</p> |

| Date | Revision | Description |
|-------------|----------|--|
| June 2000 | Q | <p>Added information about the AMD Athlon™ processor Model 4 throughout the document.</p> <p>Revised “CPUID Instruction Overview” on page 3.</p> <p>Revised Table 5, “Processor Name String,” on page 15.</p> <p>Added code sample to “Code Samples” on page 17.</p> <p>Added “Displaying the AMD Athlon™ or AMD Duron™ Processor Name String” on page 25 and “DisplayK7NameString Subroutine” on page 26.</p> <p>Revised information about bit 15 in Table 4, “Summary of Standard and Extended Feature Bits,” on page 11.</p> <p>Revised name string for AMD Athlon™ processor Model 1 in Table 5, “Processor Name String,” on page 15.</p> <p>Made Table 6, “Standard Feature Flag Descriptions for the AMD-K6®-2 and AMD-K6-III Processors,” on page 32 is specific to these processors.</p> <p>Added Table 6, “Standard Feature Flag Descriptions for the AMD Athlon™ Processors,” on page 31, which is specific to these processors.</p> <p>Clarified instruction family and generation being derived from function 1 and function 8000_0001 respectively.</p> <p>Made Table 9, “Extended Feature Flag Descriptions for the AMD-K6®-2 and AMD-K6-III Processors,” on page 36 is specific to these processors.</p> <p>Added Table 8, “Extended Feature Flag Descriptions for the AMD Athlon™ Processors,” on page 34, which is specific to these processors.</p> <p>Revised Table 21, “Values Returned By the AMD Athlon™ Processor,” on page 42.</p> |
| Dec 1999 | P | <p>Added the AMD Athlon processor Model 2 information throughout document. Model 1 refers to the AMD Athlon processor manufactured with 0.25-micron process technology and Model 2 refers to the AMD Athlon processor manufactured with 0.18-micron process technology.</p> |
| Nov 1999 | O | <p>Clarified usage of “Code Samples” on page 17.</p> <p>Added “Example Function Call” on page 25.</p> |
| August 1999 | N | <p>Merged standard and extended feature bits into one table. See Table 4, “Summary of Standard and Extended Feature Bits,” on page 11.</p> <p>Revised Table 21, “Values Returned By the AMD Athlon™ Processor,” on page 42.</p> |
| August 1999 | M | <p>Added the AMD Athlon™ processor information throughout document.</p> <p>Added url www.amd.com/products/cpg/bin, where codes samples and utilities are available.</p> <p>Revised “Testing for the CPUID Instruction” on page 4.</p> <p>Revised “Determining Instruction Set Support” on page 13.</p> <p>Revised Tables 12 through 22 to cross-reference new section—“Associativity Field Definitions” on page 45.</p> |

| Date | Revision | Description |
|-----------|----------|---|
| May 1999 | L | In Table 11 on page 18, changed function 8000_0001h EDX entries for Models 6 and 7 from 0080_01BFh to 0080_05BFh. |
| May 1999 | L | Added note about the name string for the AMD-K6-2 processor to Table 11 on page 18. |
| Feb 1999 | K | <p>Added L2 cache information to Table 1 on page 4.</p> <p>Added Function 8000_0006h to “Displaying Cache Information” on page 10.</p> <p>Added Function 8000_0006h — L2 Cache Information and Table 10, “ECX Format Returned by Function 8000_0006h,” on page 17.</p> <p>Added AMD-K6-III processor Model 9 values and three notes to Table 11 on page 18.</p> |
| Nov 1998 | J | <p>In “Standard Functions” on page 12, clarified AMD’s vendor identification string stored in registers EBX, EDX, and ECX.</p> <p>In Table 11, “Values Returned By AMD-K6[®] Processors,” on page 18, changed function 8000_0001h, EDX value for the AMD-K6 processor Model 7 and deleted note 2.</p> |
| May 1998 | I | <p>Revised “Functions 8000_0002h, 8000_0003h, and 8000_0004h — Processor Name String” on page 16.</p> <p>Added return values for AMD-K6 processor Model 9 to Table 10 on page 18. Divided Appendix B table into two separate tables.</p> |
| Jan 1998 | H | Added revised bit 31 description and alternate test for AMD-K6-2 to “Identifying Supported Features” on page 6. |
| Dec 1997 | G | <p>Changed part names for AMD-K6 processor Models 8 and 9 in Table 2 on page 5.</p> <p>Added 3DNow![™] instructions feature (bit 31) to Table 4 on page 8 and Table 6 on page 15.</p> <p>Added AMD-K6[®]-2 processor return values to Table 12 on page 21.</p> |
| Sept 1997 | F | Moved SYSCALL/SYSRET instruction feature bit (in extended feature function 8000_0001h) from bit 10 to bit 11. See Table 6 on page 15 and Table 12 on page 21. |
| Sept 1997 | F | Added bit 31 to the extended feature function 8000_0001h for a new feature. See Table 4 on page 8 and Table 6 on page 15. |
| Sept 1997 | F | Added support for AMD-K6 [®] processor Models 7, 8, and 9 to Table 1 on page 4 and Table 2 on page 5. |
| Sept 1997 | F | Added return values for AMD-K6 processor Model 7 to Table 12 on page 21. |

Chapter 1 Introduction

As the number of choices available in the x86 Instruction Set Architecture (ISA) processor marketplace grew, the need for a simple way for hardware and software to identify the type of processor and its feature set became critical. The CPUID instruction was added to the x86 instruction set for this purpose. This document contains information on how to use the CPUID instruction to identify AMD processors and their features.

After detecting the processor and its capabilities, software can be tuned to the system for maximum performance and benefit to users. For example, software can roughly determine the performance level of a particular processor by detecting the type or speed of the processor. If the performance level is high enough, the software can enable additional capabilities or more advanced algorithms. Another example involves testing for the presence of 3DNow![™] instruction, SSE, or MMX[™] instruction support on the processor. (The combined support of 3DNow! instruction extensions and SSE is known as 3DNow! Professional technology.) If the software finds these features present when it checks the feature bits, it can utilize these more powerful extensions for dramatically better performance on new multimedia software.

Chapter 2 CPUID Instruction Overview

Software operating at any privilege level can execute the CPUID instruction to identify the processor and its feature set. The CPUID instruction implements multiple functions, each providing different information about the processor, including the vendor, model number, revision (stepping), features, cache organization, and processor name. The multiple-function approach allows the CPUID instruction to return a complete picture of the processor and its capabilities—more detailed information than could be returned by a single function. In addition to gathering all the information by calling multiple functions, the CPUID instruction provides the flexibility of making only one call to obtain the specific data requested.

The functions are divided into two types: *standard functions* and *extended functions*. Standard functions provide a simple method for software to access information common to all x86 ISA processors. Extended functions provide information on vendor-specific processor features (such as those by AMD).

The flexibility of the CPUID instruction allows for the addition of new CPUID functions in future generations of processors. Chapter 5, "CPUID Instruction Definition," contains a detailed description of the CPUID instruction.

Chapter 3 Using CPUID Instructions

3.1 Testing for the CPUID Instruction

To use the CPUID instruction, software must first determine if the processor supports the CPUID instruction.

Note: All AMD family processors, beginning with the Am486[®] DX4 processor, support the CPUID instruction.

CPUID support is determined in one of the following ways:

- *Illegal Instruction Exception:* Execute the CPUID instruction and check whether an illegal instruction exception occurs. If an exception occurs, the processor does not have CPUID support.
- *EFLAGS ID-Bit:* Check if the ID bit (bit 21) of the EFLAGS register is writable. If the bit is writable (that is, it can be modified), the CPUID instruction is supported.

The Operating System (OS) environment determines which approach is more appropriate. These methods are described in the following sections.

3.1.1 Illegal Instruction Exception Method

This method requires a way for a user program to detect and handle illegal instruction exceptions. Where such capabilities are present, this method represents a reliable way of detecting support for the CPUID instruction. The CPUID sample code starting on page 35 uses this method.

3.1.2 EFLAGS ID-Bit Method

This method retrieves the contents of EFLAGS using the PUSHFD instruction, toggles the ID bit, and uses the POPFD instruction to write the modified value of the ID bit into the EFLAGS register. It then retrieves the contents of EFLAGS using a second PUSHFD instruction and checks whether the value of the ID bit differs from the original value. If the value has changed, the CPUID instruction is available for identifying the processor and its features. The following code sample demonstrates the way a program uses the PUSHFD and POPFD instructions to test the ID bit.

```

pushfd          ; Save EFLAGS to stack
pop eax         ; Store EFLAGS in EAX
mov ebx, eax    ; Save in EBX for testing later
xor eax, 00200000h ; Switch bit 21
push eax       ; Copy changed value to stack
popfd          ; Save changed EAX to EFLAGS
pushfd         ; Push EFLAGS to top of stack
pop eax        ; Store EFLAGS in EAX
cmp eax, ebx   ; See if bit 21 has changed
jz NO_CPUID    ; If no change, no CPUID

```

A potential problem with this method is that an interrupt or a trap (such as a debug trap) can occur between the POPFD and the following PUSHFD, and that the interrupt or trap handler code destroys the value of the ID bit. Where possible, the preceding code should be preceded by a CLI instruction and followed by an STI instruction, which ensures that no interrupts occur between the POPFD and the PUSHFD. However, traps can still occur, even if the code is preceded by a CLI instruction and followed by an STI instruction.

3.2 Using CPUID Functions

When software uses the CPUID instruction to identify a processor, it is important that the software uses the instruction appropriately. The instruction has been defined to make it easy to identify the type and features of x86 ISA processors manufactured by many different vendors.

The standard functions (EAX=0 and EAX=1) are the same for all processors. Having standard functions simplifies the software task of testing for and implementing features common to x86 ISA processors. Software can test for these features and, as new x86 processors are released, benefit from these capabilities immediately.

Extended functions report information on vendor-specific processor features. These functions provide additional information about AMD processors that software can use to identify enhanced features and functions. To test for extended functions, software checks for a value of at least 8000_0001h in the EAX register returned by function 8000_0000h.

Within the AMD family of processors, different members can execute a different number of functions. Table 1 on page 20, Table 2 on page 21, and Table 3 on page 22 summarize the CPUID functions currently implemented on AMD processors.

Table 1. Summary of CPUID Functions for the AMD Athlon™ 64 and AMD Opteron™ Processor

| Standard Function | Extended Function | Description | AMD Athlon™ 64 and AMD Opteron™ Processors (Models 4 and 5) |
|-------------------|-------------------|---|---|
| 0 | — | Vendor String and Largest Standard Function Value | X |
| 1 | — | Processor Signature and Standard Feature Bits | X |

Table 1. Summary of CUID Functions for the AMD Athlon™ 64 and AMD Opteron™ Processor

| Standard Function | Extended Function | Description | AMD Athlon™ 64 and AMD Opteron™ Processors (Models 4 and 5) |
|-------------------|-------------------------------|--|---|
| – | 8000_0000h | Largest Extended Function Value | X |
| – | 8000_0001h | Extended Processor Signature and Extended Feature Bits | X |
| – | 8000_0002h | Processor Name | X |
| – | 8000_0003h | Processor Name | X |
| – | 8000_0004h | Processor Name | X |
| – | 8000_0005h | L1 TLB ¹ /Cache Information | X |
| – | 8000_0006h | L2 TLB/Cache Information | X |
| – | 8000_0007h | Advanced Power Management Feature Flags | X |
| – | 8000_0008h | Physical Address and Linear Address Size | X |
| – | 8000_0009h through 8000_0018h | Vendor-Specific Feature Flags | X |

Notes:
Future versions of these processors may implement additional functions.
Chapter 5, "CUID Instruction Definition," contains detailed descriptions of the functions.
 1. TLB = Translation Lookaside Buffer.

Table 2. Summary of CUID Functions in AMD Athlon™ and AMD Duron™ Processors

| Standard Function | Extended Function | Description | AMD Athlon™ Processor Models 1, 2, and 4 | AMD Duron™ Processor Model 3 | AMD Athlon and AMD Duron Processors Model 6 ² | AMD Duron Processor Model 7 ⁵ | AMD Athlon Processor Model 8 ⁴ | AMD Athlon Processor Model 10 ⁴ |
|-------------------|-------------------|--|--|------------------------------|--|--|---|--|
| 0 | – | Vendor String and Largest Standard Function Value | X | X | X | X | X | X |
| 1 | – | Processor Signature and Standard Feature Bits | X | X | X | X | X | X |
| – | 8000_0000h | Largest Extended Function Value | X | X | X | X | X | X |
| – | 8000_0001h | Extended Processor Signature and Extended Feature Bits | X | X | X | X | X | X |
| – | 8000_0002h | Processor Name | X | X | X | X | X | X |

Table 2. Summary of CUID Functions in AMD Athlon™ and AMD Duron™ Processors

| Standard Function | Extended Function | Description | AMD Athlon™ Processor Models 1, 2, and 4 | AMD Duron™ Processor Model 3 | AMD Athlon and AMD Duron Processors Model 6 ² | AMD Duron Processor Model 7 ³ | AMD Athlon Processor Model 8 ⁴ | AMD Athlon Processor Model 10 ⁴ |
|-------------------|-------------------|---|--|------------------------------|--|--|---|--|
| – | 8000_0003h | Processor Name | X | X | X | X | X | X |
| – | 8000_0004h | Processor Name | X | X | X | X | X | X |
| – | 8000_0005h | L1 TLB¹/Cache Information | X | X | X | X | X | X |
| – | 8000_0006h | L2 TLB/Cache Information | X | X | X | X | X | X |
| – | 8000_0007h | Advanced Power Management Feature Flags | – | – | X | X | X | X |
| – | 8000_0008h | Physical Address and Linear Address Size | – | – | X | X | X | X |

Notes:

Future versions of these processors may implement additional functions.

Chapter 5, "CUID Instruction Definition", contains detailed descriptions of the functions.

1. TLB = Translation Lookaside Buffer.

2. The AMD Athlon™ processor model 6 includes the AMD Athlon MP processor, the AMD Athlon XP processor, and the mobile AMD Athlon 4 processor. The AMD Duron™ processor model 6 includes the AMD Duron processor and the mobile AMD Duron processor.

3. The AMD Duron processor model 7 includes both the AMD Duron processor and the mobile AMD Duron processor.

4. The AMD Athlon processor models 8 and 10 include the AMD Athlon MP processor, the AMD Athlon XP processor, and the mobile AMD Athlon XP-M processor.

Table 3. Summary of CUID Functions in AMD Processors

| Standard Function | Extended Function | Description | AMD-K5 Processor (Model 0), Am486® DX4, and Am5x86 Processors | AMD-K5 Processor (Models 1, 2, and 3) | AMD-K6® Processor (Models 6, 7) AMD-K6-2 Processor (Model 8) | AMD-K6®-III Processor (Model 9) |
|-------------------|-------------------|---|---|---------------------------------------|--|---------------------------------|
| 0 | – | Vendor String and Largest Standard Function Value | X | X | X | X |
| 1 | – | Processor Signature and Standard Feature Bits | X | X | X | X |
| – | 8000_0000h | Largest Extended Function Value | – | X | X | X |
| – | 8000_0001h | Extended Processor Signature and Extended Feature Bits | – | X | X | X |
| – | 8000_0002h | Processor Name | – | X | X | X |
| – | 8000_0003h | Processor Name | – | X | X | X |

Table 3. Summary of CPUID Functions in AMD Processors

| Standard Function | Extended Function | Description | AMD-K5 Processor (Model 0), Am486 [®] DX4, and Am5 _x 86 Processors | AMD-K5 Processor (Models 1, 2, and 3) | AMD-K6 [®] Processor (Models 6, 7) AMD-K6-2 Processor (Model 8) | AMD-K6 [®] -III Processor (Model 9) |
|-------------------|-------------------|--|--|---------------------------------------|--|--|
| – | 8000_0004h | Processor Name | – | X | X | X |
| – | 8000_0005h | L1 TLB [*] /Cache Information | – | X | X | X |
| – | 8000_0006h | L2 TLB/Cache Information | – | – | – | X |
| – | 8000_0007h | Advanced Power Management Feature Flags | – | – | – | – |
| – | 8000_0008h | Physical Address and Linear Address Size | – | – | – | – |

Notes:
Future versions of these processors may implement additional functions.
Chapter 3, "Using CPUID Instructions", contains detailed descriptions of the functions.
** TLB = Translation Lookaside Buffer.*

3.3 Identifying the Processor Vendor

Software must execute the standard function EAX=0. The CPUID instruction returns a 12-character string that identifies the vendor of the processor. The instruction also returns the largest standard function input value defined for the CPUID instruction on the processor.

For AMD processors, function 0 returns a vendor string of “AuthenticAMD”. This string informs the software to follow AMD’s definition for subsequent CPUID functions and the registers returned for those functions.

Once the software identifies the vendor of the processor, it knows the definition for all the functions supplied by the CPUID instruction. By using these functions, the software obtains the processor information needed to tune its functionality to the capabilities of the processor.

3.4 Testing For Extended Functions

Software must test for extended functions with function 8000_0000h. The EAX register returns the largest extended function input value defined for the CPUID instruction on the processor. If this value is at least 8000_0001h, extended functions are supported.

3.5 Determining the Processor Signature

Standard function 1 (EAX=1) of the CPUID instruction returns the standard processor signature and feature bits. The standard processor signature is returned in the EAX register and provides information regarding the specific revision (stepping) and model of the processor and the instruction family level supported by the processor. The revision level can be used to determine if the processor supports specific features. However, it is not recommended that the revision level be used in this manner unless this information is not available through the standard or extended feature bits.

AMD Athlon™ 64 and AMD Opteron™ processors (Models 5 and 6) belong to family 0Fh. All AMD Athlon™ processor models and the AMD Duron™ processor belong to instruction family 6. All AMD-K6® processor models belong to instruction family 5 (as returned in EAX by function 1).

Figure 1 shows the contents of the EAX returned by function 1.

| | | | | | | | | | | | | | |
|---------------|----|-----------------|----|----|----------------|----|---------------|----|--------|---|-------|---|----------|
| 31 | 28 | 27 | 20 | 19 | 16 | 15 | 12 | 11 | 8 | 7 | 4 | 3 | 0 |
| Reserved, RAZ | | Extended Family | | | Extended Model | | Reserved, RAZ | | Family | | Model | | Stepping |

| Bits | Mnemonic | Definition |
|-------|------------------------------|---|
| 31–28 | Reserved | RAZ |
| 27–20 | Extended Family ¹ | if (Family = 0Fh), provides additional family information |
| 19–16 | Extended Model ¹ | if (Family = 0Fh), provides additional model information |
| 15–12 | Reserved | RAZ |
| 11–8 | Family | Processor/Instruction Family |
| 7–4 | Model | Processor Model |
| 3–0 | Stepping | Processor Stepping (revision) |

Note: 1. These bit fields are supported only on the AMD Athlon™ 64 and AMD Opteron™ processors. For the AMD Athlon and AMD Duron processors, and earlier AMD processors, these bit fields are reserved and RAZ.

Figure 1. Contents of EAX Register Returned by Function 1 and 8000_0001h

Table 4 summarizes the specific processor signature values returned for all AMD processors.

Table 4. Summary of Processor Signatures for AMD Processors

| Processor | Extended Instruction Family [27:20] | Extended Model [19:16] | Instruction Family [11:8] | Model [7:4] | Stepping ID ² [3:0] |
|---|-------------------------------------|------------------------|---------------------------|-------------------|--------------------------------|
| Am486 [®] and Am5 _x 86 Processors | 0 | 0 | 0100b (4h) | yyyy ¹ | xxxx |
| AMD-K5 Model 0 | 0 | 0 | 0101b (5h) | 0000b (0h) | xxxx |
| AMD-K5 Model 1 | 0 | 0 | 0101b (5h) | 0001b (1h) | xxxx |
| AMD-K5 Model 2 | 0 | 0 | 0101b (5h) | 0010b (2h) | xxxx |
| AMD-K5 Model 3 | 0 | 0 | 0101b (5h) | 0011b (3h) | xxxx |
| AMD-K6 [®] Model 6 | 0 | 0 | 0101b (5h) | 0110b (6h) | xxxx |
| AMD-K6 Model 7 | 0 | 0 | 0101b (5h) | 0111b (7h) | xxxx |
| AMD-K6 [®] -2 Model 8 | 0 | 0 | 0101b (5h) | 1000b (8h) | xxxx |
| AMD-K6 [®] -III Model 9 | 0 | 0 | 0101b (5h) | 1001b (9h) | xxxx |
| AMD Athlon™ Model 1 | 0 | 0 | 0110b (6h) | 0001b (1h) | xxxx |
| AMD Athlon Model 2 | 0 | 0 | 0110b (6h) | 0010b (2h) | xxxx |
| AMD Duron™ Model 3 | 0 | 0 | 0110b (6h) | 0011b (3h) | xxxxb |
| AMD Athlon Model 4 | 0 | 0 | 0110b (6h) | 0100b (4h) | xxxxb |
| AMD Athlon MP Model 6 | 0 | 0 | 0110b (6h) | 0110b (6h) | xxxxb |
| AMD Athlon XP Model 6 | 0 | 0 | 0110b (6h) | 0110b (6h) | xxxxb |
| Mobile AMD Athlon 4 Model 6 | 0 | 0 | 0110b (6h) | 0110b (6h) | xxxxb |
| AMD Duron Model 6 | 0 | 0 | 0110b (6h) | 0110b (6h) | xxxxb |
| Mobile AMD Duron Model 6 | 0 | 0 | 0110b (6h) | 0110b (6h) | xxxxb |
| AMD Duron Model 7 | 0 | 0 | 0110b (6h) | 0111b (7h) | xxxxb |
| Mobile AMD Duron Model 7 | 0 | 0 | 0110b (6h) | 0111b (7h) | xxxxb |
| AMD Athlon XP Model 8 | 0 | 0 | 0110b (6h) | 1000b (8h) | xxxxb |
| AMD Athlon MP Model 8 | 0 | 0 | 0110b (6h) | 1000b (8h) | xxxxb |
| Mobile AMD Athlon XP–M Model 8 | 0 | 0 | 0110b (6h) | 1010b (Ah) | xxxxb |
| Mobile AMD Athlon XP–M (LV) Model 8 | 0 | 0 | 0110b (6h) | 1010b (Ah) | xxxxb |
| AMD Athlon XP Model 10 | 0 | 0 | 0110b (6h) | 1010b (Ah) | xxxxb |
| AMD Athlon MP Model 10 | 0 | 0 | 0110b (6h) | 1010b (Ah) | xxxxb |
| Mobile AMD Athlon XP–M Model 10 | 0 | 0 | 0110b (6h) | 1010b (Ah) | xxxxb |
| Mobile AMD Athlon XP–M (LV) Model 10 | 0 | 0 | 0110b (6h) | 1010b (Ah) | xxxxb |

Notes:

1. Contact your AMD representative for model identifier information.
2. Stepping ID may change. Consult the appropriate processor revision guide, or contact your AMD representative for the latest stepping information. AMD Athlon processors of the same model numbers share the same revision guide. AMD Duron processors of the same model number share the same Revision Guide.

Table 4. Summary of Processor Signatures for AMD Processors (Continued)

| Processor | Extended Instruction Family [27:20] | Extended Model [19:16] | Instruction Family [11:8] | Model [7:4] | Stepping ID ² [3:0] |
|------------------------|-------------------------------------|------------------------|---------------------------|-------------|--------------------------------|
| AMD Athlon™ 64 Model 4 | 0 | 0 | 1111b (0Fh) | 0100b (04h) | xxxxb |
| AMD Opteron™ Model 5 | 0 | 0 | 1111b (0Fh) | 0101b (05h) | xxxxb |

Notes:

- Contact your AMD representative for model identifier information.
- Stepping ID may change. Consult the appropriate processor revision guide, or contact your AMD representative for the latest stepping information. AMD Athlon processors of the same model numbers share the same revision guide. AMD Duron processors of the same model number share the same Revision Guide.

3.6 Identifying Supported Features

The feature bits are returned in the EDX register for two CPUID functions: standard function 1 and extended function 8000_0001h. Each bit corresponds to a specific feature and indicates if that feature is present on the processor. For table summaries of the standard and extended feature bits, view the tables 10 through 7 in Chapter 5, "CPUID Instruction Definition".

Before using any of the enhanced features added to the latest generation of processors, software should test each feature bit returned by functions 1 and 8000_0001h to identify the capabilities available on the processor. For example, software must test feature bit 23 to determine if the processor executes the MMX™ technology instructions. Attempting to execute an unavailable feature can cause errors and exceptions.

Bit 31, as returned by extended function 8000_0001h, designates the presence of 3DNow!™ technology. Other processor vendors have adopted this technology, so bit 31 is now considered an open standard. Chapter 5, "CPUID Instruction Definition", and Appendix A, "Register Values Returned by the AMD Family Processors", contain details on bit locations and values.

3.6.1 Determining Instruction Set Support

It is preferable to use CPUID feature flags as much as possible, rather than deriving capabilities from vendor specifiers combined with CPUID model numbers.

To simplify the detection of the new instructions supported in the AMD Athlon 64 and AMD Opteron processors or in different models of AMD Athlon™ and AMD Duron™ family of processors, including the original 3DNow! and MMX instructions, Enhanced 3DNow!, and 3DNow! Professional (combining 3DNow! and SSE support), use the following algorithm.

CPUID Test

- Establish that the processor has support for CPUID. See "Using CPUID Instructions" on page 19.

Standard Function Test

2. Execute CPUID function 0, which returns the processor vendor string and the highest standard function supported.
3. If step 2 indicates that the highest standard function is at least 1, execute CPUID function 1, which returns the standard feature flags in the EDX register.

MMX™ Test

4. If bit 23 of the standard feature flags is set to “1”, MMX™ technology is supported. MMX instruction support is the basic minimum processor feature required to support other instruction extensions.

SSE Test

5. If bit 25 of the standard feature flags is set to “1” on an AMD Athlon 64 or an AMD Opteron processor or on either an AMD Athlon™ or AMD Duron™ processor model 6 or greater, SSE instructions are supported. Optionally, if bit 25 of the standard feature flags is set on any previous AMD processor, it has streaming SIMD extensions (SSE) capabilities. Further qualification of SSE is done by checking for OS support. SSE support might be present in the processor but is not usable due to a lack of OS support for the additional architected registers.

Extended Functions Test

6. Execute CPUID extended function 8000_0000h. This function returns the highest extended function supported in EAX. If EAX=0, there is no support for extended functions.
7. If the highest extended function supported is at least 8000_0001h, execute CPUID function 8000_0001h. This function returns the extended feature flags in EDX.

3DNow!™ Instruction Test

8. If bit 31 of the extended feature flags is set to “1”, the 3DNow!™ instructions are supported.

3DNow!™ Instruction Extensions Test

9. If bit 30 of the extended feature flags is set to “1”, the additions to the 3DNow! instruction set are supported.

MMX™ Extensions Test

10. If bit 22 of the extended feature flags is set to “1”, the new multimedia enhancement instructions that augment the MMX instruction set are supported.

Long Mode Test

11. If bit 29 of the extended feature flags is set to “1”, then the “long mode” (including 64-bit mode) of the x86-64 ISA is supported.

PREFETCH and PREFETCHW Test

12. If either bit 29 or bit 31 of the extended feature flags is set to 1 (either Long Mode or 3DNow! instructions are supported), then the PREFETCH and PREFETCHW instructions are supported.

No-Execute Page Protection Test

13. If bit 20 of the extended feature flags is set to “1”, then the No-Execute Page feature of the processor can be enabled.

3.6.2 AMD Processor Signature (Extended Function)

Extended function 8000_0001h returns the AMD processor signature. The signature is returned in the EAX register and provides generation, model, and stepping information for AMD processors. Starting with the AMD Athlon 64 and AMD Opteron processors, the 8000_0001h function supplements the family and model numbers with two new fields: *extended family* and *extended model* fields. These new fields expand the family and model numbering scheme.

Figure 1 on page 24 shows the contents returned in the EAX register.

The terms *effective family* and *effective model* describe the expanded 8-bit family and 8-bit model numbers as computed using the extended family, family, extended model, and model fields.

Software that displays or uses the processor family and model must be aware of how the extended family and extended model fields combine with the family and model fields to produce the effective family and effective model numbers. *Software must use the computed 8-bit effective family and effective model numbers when displaying or using the processor's family and model numbers. Failure to do so results in the display or use of incorrect values.*

If the family field (EAX bits 11–8) is equal to 1111b (0Fh), use the extended family and extended model fields to compute the 8-bit effective family and effective model numbers as shown in the following sample code:

```
EAX = CPUID(0000_0001)
Family = EAX.11:8
Model = EAX.7:4
ExtendedFamily = EAX.27:20 /* 8 bits */
ExtendedModel = EAX.19:16 /* 4 bits */

IF (Family == 0Fh)

    EFFECTIVE_FAMILY = ExtendedFamily /* 8 bits */
                      + Family /* 4 bits, zero extended to 8 bits */
    EFFECTIVE_MODEL = (ExtendedModel << 4) /* 8 bits */
                     + Model /* 4 bits, zero extended to 8 bits */
```

3.6.3 Displaying the Processor Name

Functions 8000_0002h, 8000_0003h, and 8000_0004h return an ASCII string containing the name of the processor. These functions eliminate the need for software to search for the processor name in a lookup table, a process requiring a large block of memory and frequent updates. Instead, software can simply call these three functions to obtain the name string (48 ASCII characters in little-endian format) and display it on the screen. Although the name string can be up to 48 characters in length, shorter names have the remaining byte locations filled with the ASCII NULL character (00h). To simplify the display routines and avoid using screen space, software only needs to display characters until a NULL character is detected.

Note: The processor name string supports up to 48 characters, but not all name strings are 48 characters. For example, the name string “AMD Athlon(tm)” uses 14 characters. Future name strings may be longer, so BIOS vendors should take this into consideration when displaying the name string on boot-up or in a system configuration screen.

Unlike previous generations of AMD processors, AMD Athlon 64 and AMD Opteron processors do not have a pre-programmed default name string. These processors return 48 ASCII NULLs until the name string is programmed by BIOS.

Therefore, AMD Athlon 64 and AMD Opteron processors must have the processor name string programmed by the BIOS before any general purpose application or OS software uses the extended functions that read the name string. All processors support a set of MSRs for programming the processor name string. For information about programming the name string, see Appendix B, “Programming the Name String of the AMD Athlon™ 64 and AMD Opteron™ Processors”.

AMD Athlon 64 and AMD Opteron processors implement extended functions 8000_0002h, 8000_0003h, and 8000_0004h in the same manner as previous AMD processors; therefore, it is not necessary to change software that displays the processor name string.

For sample code to display the name string, “Displaying the AMD Athlon™ 64, AMD Opteron™, AMD Athlon™, and AMD Duron™ Processor Name Strings” on page 44 for an example of how to properly obtain and display the processor name string.

3.6.3.1 Differentiation of Processors of the Same Model Number

AMD Athlon and AMD Duron processors model 6 and higher must have the name string programmed properly according to the values in Table 5 on page 31 depending on the processor’s L2 cache size. If the L2 cache size value reported by extended function 8000_0006h ECX bits[31:16] is 256 or greater, then the processor is an AMD Athlon family processor. If the L2 cache size reported is less than 256, then the processor is an AMD Duron family processor.

3.6.3.2 S3 State Considerations

Before entering the S3—Suspend to RAM (STR)—state, the BIOS must save off the processor name string MSRs. Upon exiting the S3 state, the BIOS must then reload the processor name string back into the appropriate MSRs.

3.6.3.3 Recommended Name String

The namestring of an AMD Athlon 64 or AMD Opteron processor must be programmed into the processor by the BIOS. See Appendix B "Programming the Name String of the AMD Athlon™ 64 and AMD Opteron™ Processors" on page 95 for more information.

Table 5 summarizes the recommended name strings for AMD Athlon and AMD Duron processors through models 6 and above.

Table 5. Recommended Name String by Platform Segment for AMD Athlon™ and AMD Duron™ Family of Processors Models 6 and Above

| Processor | CPUID | MP Capable (bit 19 of Extended Feature Flags) | Platform Segment | Recommended Name String ¹ |
|---------------------|------------------|---|---------------------|---|
| AMD Athlon™ Model 6 | 660 or 661 | Reserved | Multiprocessing | AMD Athlon(tm) MP |
| AMD Athlon Model 6 | 660 or 661 | Reserved | Desktop | AMD Athlon(tm) |
| AMD Athlon Model | 660 or 661 | Reserved | Mobile | mobile AMD Athlon(tm) 4 |
| AMD Athlon Model 6 | 662 | 0 | Multiprocessing | AMD Athlon(tm) XP [xxxxx] ² |
| AMD Athlon Model 6 | 662 | 1 | Multiprocessing | AMD Athlon(tm) MP [xxxxx] ² |
| AMD Athlon Model 6 | 662 | N/A | Desktop | AMD Athlon(tm) XP [xxxxx] ² |
| AMD Athlon Model 6 | 662 | N/A | Mobile | mobile AMD Athlon(tm) 4 |
| AMD Duron™ Model 6 | N/A ³ | N/A | Desktop | AMD Duron(tm) |
| AMD Duron Model 6 | N/A ³ | N/A | Mobile | mobile AMD Duron(tm) |
| AMD Duron Model 7 | N/A ³ | Reserved | Desktop | AMD Duron(tm) |
| AMD Duron Model 7 | N/A ³ | Reserved | Mobile | mobile AMD Duron(tm) |
| AMD Athlon Model 8 | N/A ³ | 0 | Multiprocessing | AMD Athlon(tm) XP [xxxxx] ² |
| AMD Athlon Model 8 | N/A ³ | 1 | Multiprocessing | AMD Athlon(tm) MP [xxxxx] ² |
| AMD Athlon Model 8 | N/A ³ | 0 | Desktop | AMD Athlon(tm) XP [xxxxx] ² |
| AMD Athlon Model 8 | N/A ³ | 1 | Desktop | AMD Athlon(tm) MP [xxxxx] ² |
| AMD Athlon Model 8 | N/A ³ | N/A | Mobile | mobile AMD Athlon(tm) XP [xxxxx] ² |
| AMD Athlon Model 10 | N/A ³ | 0 | Desktop | AMD Athlon(tm) XP [xxxxx] ² |
| AMD Athlon Model 10 | N/A ³ | 1 | Multiprocessing | AMD Athlon(tm) MP [xxxxx] ² |
| AMD Athlon Model 10 | N/A ³ | N/A | OPGA Mobile | mobile AMD Athlon(tm) XP-M [xxxxx] ² |
| AMD Athlon Model 10 | N/A ³ | N/A | μPGA Mobile | mobile AMD Athlon(tm) XP-M (LV) [xxxxx] ² |

Notes:

1. This name string must be programmed into the processor by the BIOS. See the document, Displaying and Programming the Processor Name String BIOS Application Note, order# 90056.
2. See Table 7 on page 33 and Table 5 on page 31 for proper model number to insert into name string.
3. Recommended name strings for the AMD Duron™ processors models 6 and 7 and the AMD Athlon™ processors models 8 and 10 do not vary by CPUID stepping value.

Table 6 summarizes the recommended name strings for AMD Athlon and AMD Duron processors through model 4.

Table 6. Processor Name Strings for AMD Athlon™ and AMD Duron™ Family of Processors Through Model 4

| Processor | ASCII Name String |
|--------------------------|-----------------------------------|
| AMD Athlon™ Model 1 | AMD-K7(tm) processor |
| AMD Athlon Model 2 | AMD Athlon(tm) processor |
| AMD Duron™ Model 3 | AMD Duron(tm) ¹ |
| Mobile AMD Duron Model 3 | mobile AMD Duron(tm) ¹ |
| AMD Athlon Model 4 | AMD Athlon(tm) ¹ |

Notes:

1. This name string must be programmed into the processor by the BIOS. See the document, Displaying and Programming the Processor Name String BIOS Application Note, order# 90056.

Table 7 and Table 8 on page 34 summarizes the recommended name strings for AMD Athlon processors through model 6 through 10.

Table 7. Model Number Mappings for AMD Athlon™ Family of Processors with 256-Kbyte L2 Cache

| Frequency ¹ (MHz) | Model Number |
|------------------------------|--------------|
| 950 ² | 1100+ |
| 1000 ² | 1200+ |
| 1100 ² | 1300+ |
| 1200 ² | 1400+ |
| 1300 ^{3,4} | 1500+ |
| 1333 | 1500+ |
| 1400 | 1600+ |
| 1467 | 1700+ |
| 1500 ⁴ | 1800+ |
| 1533 | 1800+ |
| 1600 | 1900+ |
| 1667 | 2000+ |
| 1733 | 2100+ |
| 1800 | 2200+ |
| 2000 | 2400+ |
| 2083 ⁵ | 2600+ |
| 2133 | 2600+ |
| 2167 ⁵ | 2700+ |
| 2250 ^{5, 6} | 2800+ |

Notes:

1. It is recommended that the BIOS display the processor name string, including the model number, whenever displaying processor information during a bootup. If the processor frequency is displayed, the processor name string, including the model number, must also be displayed. Motherboards will not pass AMD validation or be posted on the AMD recommended motherboard Web site, if during a bootup the processor frequency is displayed by the BIOS without also displaying the name string and model number for the AMD Athlon™ model 6, model 8, or model 10 processors having frequencies with corresponding model numbers.
2. The model number at 1200 MHz, 1100 MHz, 1000 MHz, and 950 MHz should be displayed only on the mobile AMD Athlon™ model 8 processor.
3. For mobile AMD Athlon™ model 6 processors, at any frequency below 1300 MHz, no model number should be shown in the name string. Also, mobile AMD Athlon™ model 6 processors below 1300 MHz have a name string of "mobile AMD Athlon(tm) 4".
4. Frequencies of 1300 MHz and 1500 MHz are only offered as mobile or low-power desktop processors using a 200 Front Side Bus.
5. Frequencies of 2083 MHz, 2167 MHz, and 2250 MHz are only offered as desktop processors using a 333 Front Side Bus.
6. At any frequency above 2250 MHz, the model number should be omitted from the name string to show simply "AMD Athlon(tm) MP" for the multiprocessing segment, "AMD Athlon(tm) XP" for desktop and low-power desktop, "mobile AMD Athlon(tm) XP-M" for OPGA mobile, or "mobile AMD Athlon(tm) XP-M (LV)" for μPGA mobile.

Table 8. Model Number Mappings for AMD Athlon™ Family Processors with 512-Kbyte L2 Cache

| Frequency ¹ (MHz) | Model Number |
|------------------------------|--------------|
| 1300 ² | 1700+ |
| 1400 ² | 1800+ |
| 1467 ² | 1900+ |
| 1533 ² | 2000+ |
| 1600 ² | 2100+ |
| 1667 ² | 2200+ |
| 1800 ² | 2400+ |
| 1833 ³ | 2500+ |
| 1867 ² | 2500+ |
| 1917 ³ | 2600+ |
| 2000 ² | 2600+ |
| 2083 ³ | 2800+ |
| 2100 ⁴ | 3000+ |
| 2133 ⁵ | 2800+ |
| 2167 ³ | 3000+ |
| 2200 ^{4,6} | 3200+ |

Notes:

1. It is recommended that the BIOS display the processor name string, including the model number, whenever displaying processor information during a bootup. If the processor frequency is displayed, the processor name string, including the model number, must also be displayed. Motherboards will not pass AMD validation or be posted on the AMD recommended motherboard Web site, if during a bootup the processor frequency is displayed by the BIOS without also displaying the name string and model number for the AMD Athlon™ model 10 processors having frequencies with corresponding model numbers.
2. Frequencies of 1300 MHz, 1400 MHz, 1467 MHz, 1533 MHz, 1600 MHz, 1667 MHz, 1800 MHz, 1867 MHz, and 2000 MHz are only offered as mobile processors using a 266 Front Side Bus.
3. Frequencies of 1833 MHz, 1917 MHz, 2083 MHz, and 2167 MHz are only offered as desktop processors using a 333 Front Side Bus.
4. Frequencies of 2100 MHz and 2200 MHz are only offered as desktop processors using a 400 Front Side Bus.
5. Frequency of 2133 MHz is offered in mobile and workstation/server processors using a 266 Front Side Bus.
6. At any frequency above 2200 MHz, the model number should be omitted from the name string to show simply "AMD Athlon(tm) MP" for the multiprocessing segment, "AMD Athlon(tm) XP" for desktop and low-power desktop, "mobile AMD Athlon(tm) XP-M" for OPGA mobile, or "mobile AMD Athlon(tm) XP-M (LV)" for μPGA mobile.

3.6.4 Displaying Cache Information

Functions 8000_0005h and 8000_0006h provide cache information for the processor, although function 8000_0006h is only supported on AMD Athlon 64 and AMD Opteron processors, the AMD Athlon processors, the AMD Duron processors, and on the AMD-K6[®]-III processor model 9. Some diagnostic software displays information about the system and the processor configuration. It is common for this type of software to provide cache size and organization of information.

Functions 8000_0005h and 8000_0006h provide a simple way for software to obtain information about the on-chip cache and Translation Lookaside Buffer (TLB) structures. The size and organization information is returned in the registers as described in Chapter 5, "CPUID Instruction Definition". Software can simply display these values, eliminating the need for large pieces of code to test the memory structures.

3.6.5 Determining Power Management Capabilities

AMD Athlon 64 and AMD Opteron processors support the detection of power management features through the use of function 8000_0007h. These features include on-chip thermal diode, Voltage ID transitioning, Frequency ID transitioning, and thermal trip.

The AMD Athlon family of processors model 6 or greater and the AMD Duron family of processors model 7 also support the detection of power management features through the use of function 8000_0007h. These features include an on-chip thermal diode, Voltage ID transitioning, and Frequency ID transitioning. Desktop varieties of model 6 and model 7 processors will have support only for the thermal diode. Mobile varieties of model 6 and model 7 processors support the thermal diode, Voltage ID (VID) transitioning, and Frequency ID (FID) transitioning.

3.6.6 Determining Maximum Physical and Linear Address Size

AMD Athlon 64 and AMD Opteron processors, the AMD Athlon family of processors model 6 or greater, and the AMD Duron family processors model 7 support function 8000_0008h, which provides the maximum physical and maximum linear address size supported by the processor.

3.6.7 Determining Vendor-Specific Feature Flags

The AMD Athlon 64 and AMD Opteron processor introduces several new Extended CPUID functions. Functions 8000_0009h through 8000_0018h are reserved for future expansion of vendor-specific feature flags. See Chapter 5, "CPUID Instruction Definition" for more information.

3.7 Code Samples

Developers who want to create their own processor-features detection code should follow the sample code described in "Example CPUID Code."

A more elaborate function call, which detects the full range of CPUID information, is provided as sample code in “Example Function Call” on page 43.

3.7.1 Example CPUID Code

Developers who want to create their own processor detection program should follow the algorithm in the “cpuid_ex” program. The code sample is available from AMD’s website at the following URL:

http://www.amd.com/products/cpg/bin/cpuid_ex.zip

The source code is included, along with an executable that is compiled with Microsoft[®] Visual Studio C/C++ Versions 5 and 6. This example provides a simple algorithm for the developer to follow and can be accommodated by many different processors. The source code, cpuid_ex.c, follows the recommendations described in this document.

To display a list of supported features for the processor, run the program by typing
cpuid_ex

For convenience, the example CPUID code is displayed as follows:

```
/* The following code follows the guidelines described in this document,  
It is meant to serve as only an example, as there are other ways to accomplish  
processor detection. */
```

```
#include <stdio.h>  
#include <excpt.h>
```

```
/* Symbolic constants for feature flags in CPUID standard feature flags */
```

```
#define CPUID_STD_FPU          0x00000001  
#define CPUID_STD_VME         0x00000002  
#define CPUID_STD_DEBUGEXT    0x00000004  
#define CPUID_STD_4MPAGE      0x00000008  
#define CPUID_STD_TSC         0x00000010  
#define CPUID_STD_MSR         0x00000020  
#define CPUID_STD_PAE         0x00000040  
#define CPUID_STD_MCHKXCP     0x00000080  
#define CPUID_STD_CMPXCHG8B   0x00000100  
#define CPUID_STD_APIC        0x00000200  
#define CPUID_STD_SYSENTER    0x00000800  
#define CPUID_STD_MTRR        0x00001000  
#define CPUID_STD_GPE         0x00002000  
#define CPUID_STD_MCHKARCH    0x00004000  
#define CPUID_STD_CMOV        0x00008000  
#define CPUID_STD_PAT         0x00010000  
#define CPUID_STD_PSE36       0x00020000  
#define CPUID_STD_MMX         0x00800000  
#define CPUID_STD_FXSAVE      0x01000000  
#define CPUID_STD_SSE         0x02000000
```

```
/* Symbolic constants for feature flags in CPUID extended feature flags */
```

```
#define CPUID_EXT_3DNOW        0x80000000  
#define CPUID_EXT_AMD_3DNOWEXT 0x40000000  
#define CPUID_EXT_AMD_MMXEXT   0x00400000
```

```
/* Symbolic constants for application specific feature flags */
```

```
#define FEATURE_CPUID          0x00000001  
#define FEATURE_STD_FEATURES  0x00000002  
#define FEATURE_EXT_FEATURES  0x00000004  
#define FEATURE_TSC           0x00000010  
#define FEATURE_MMX           0x00000020  
#define FEATURE_CMOV          0x00000040  
#define FEATURE_3DNOW         0x00000080  
#define FEATURE_3DNOWEXT      0x00000100  
#define FEATURE_MMXEXT        0x00000200
```

```

#define FEATURE_SSEFP          0x00000400
#define FEATURE_K6_MTRR       0x00000800
#define FEATURE_P6_MTRR       0x00001000

/* Older compilers do not support the CPUID instruction in inline assembly */

#define cpuid _asm _emit 0x0f _asm _emit 0xa2

/* get_feature_flags extracts all features the application wants to know
   about from CPUID information and returns a bit string of application
   specific feature bits. The following design criteria apply:

1. Processor capabilities should be directly derived from CPUID feature bits
   wherever possible, instead of being derived from vendor strings and
   processor signatures. However, some features are not indicated by CPUID
   feature flags (whether basic or extended) and do require looking at
   vendor strings and processor signatures. Applications may also choose to
   implement pseudo capabilities, for example indicating performance
   levels.
2. The basic feature flags returned by CPUID function #1 are compatible
   across all x86 processor vendors with very few exceptions and therefore
   common feature checks for things like MMX or TSC support do not require
   a vendor check before evaluating the basic feature flag information.
   If unsure about a particular feature, review the processor vendor's
   literature.
3. 3DNow! technology is an open standard. Therefore 3DNow! instruction
   capabilities are indicated by bit 31 in the extended feature flags
   regardless of processor vendor.
4. Applications should always treat the floating-point part of SSE and
   the MMX part of SSE as separate capabilities because SSE FP requires
   OS support that might not be available, while SSE MMX works with all
   operating systems.
*/

unsigned int get_feature_flags(void)
{
    unsigned int result      = 0;
    unsigned int signature = 0;
    char vendor[13]         = "UnknownVendr"; /* Needs to be exactly 12 chars */

    /* Define known vendor strings here */

    char vendorAMD[13]      = "AuthenticAMD"; /* Needs to be exactly 12 chars */
    /*;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
    ;; Step 1: Check if processor has CPUID support. The processor faults
    ;; with an illegal instruction exception if the instruction is not
    ;; supported. This step catches the exception and immediately returns
    ;; with feature string bits with all 0s, if the exception occurs.
    ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;*/

```

```

__try {
    __asm xor    eax, eax
    __asm xor    ebx, ebx
    __asm xor    ecx, ecx
    __asm xor    edx, edx
    __asm cpuid
}

__except (EXCEPTION_EXECUTE_HANDLER) {
    return (0);
}

result |= FEATURE_CPUID;

__asm {

    ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
    ;; Step 2: Check if CPUID supports function 1 (signature/std features)
    ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

    xor    eax, eax                ; CPUID function #0
    cpuid                ; largest std func/vendor string
    mov    dword ptr [vendor], ebx ; save
    mov    dword ptr [vendor+4], edx ; vendor
    mov    dword ptr [vendor+8], ecx ; string
    test   eax, eax                ; largest standard function==0?
    jz    $no_standard_features    ; yes, no standard features func
    or    [result], FEATURE_STD_FEATURES; does have standard features

    ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
    ;; Step 3: Get standard feature flags and signature
    ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

    mov    eax, 1                ; CPUID function #1
    cpuid                ; get signature/std feature flgs
    mov    [signature], eax       ; save processor signature

    ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
    ;; Step 4: Extract desired features from standard feature flags
    ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

    ;; Check for time stamp counter support

    mov    ecx, CPUID_STD_TSC     ; bit 4 indicates TSC support
    and    ecx, edx                ; supports TSC ? CPUID_STD_TSC:0
    neg    ecx                    ; supports TSC ? CY : NC
    sbb    ecx, ecx                ; supports TSC ? 0xffffffff:0
    and    ecx, FEATURE_TSC       ; supports TSC ? FEATURE_TSC:0
    or    [result], ecx           ; merge into feature flags

    ;; Check for MMX support

```

```

mov     ecx, CPUID_STD_MMX           ; bit 23 indicates MMX support
and     ecx, edx                     ; supports MMX ? CPUID_STD_MMX:0
neg     ecx                           ; supports MMX ? CY : NC
sbb     ecx, ecx                     ; supports MMX ? 0xffffffff:0
and     ecx, FEATURE_MMX             ; supports MMX ? FEATURE_MMX:0
or      [result], ecx                ; merge into feature flags

;; Check for CMOV support

mov     ecx, CPUID_STD_CMOV          ; bit 15 indicates CMOV support
and     ecx, edx                     ; supports CMOV?CPUID_STD_CMOV:0
neg     ecx                           ; supports CMOV ? CY : NC
sbb     ecx, ecx                     ; supports CMOV ? 0xffffffff:0
and     ecx, FEATURE_CMOV           ; supports CMOV ? FEATURE_CMOV:0
or      [result], ecx                ; merge into feature flags

;; Check support for P6-style MTRRs

mov     ecx, CPUID_STD_MTRR         ; bit 12 indicates MTRR support
and     ecx, edx                     ; supports MTRR?CPUID_STD_MTRR:0
neg     ecx                           ; supports MTRR ? CY : NC
sbb     ecx, ecx                     ; supports MTRR ? 0xffffffff:0
and     ecx, FEATURE_P6_MTRR       ; supports MTRR ? FEATURE_MTRR:0
or      [result], ecx                ; merge into feature flags

;; Check for initial SSE support. There can still be partial SSE
;; support. Step 9 will check for partial support.

mov     ecx, CPUID_STD_SSE           ; bit 25 indicates SSE support
and     ecx, edx                     ; supports SSE ? CPUID_STD_SSE:0
neg     ecx                           ; supports SSE ? CY : NC
sbb     ecx, ecx                     ; supports SSE ? 0xffffffff:0
and     ecx, (FEATURE_MMXEXT+FEATURE_SSEFP) ; supports SSE ?
                                           ; FEATURE_MMXEXT+FEATURE_SSEFP:0
or      [result], ecx                ; merge into feature flags

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;; Step 5: Check for CPUID extended functions
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

mov     eax, 0x80000000               ; extended function 0x80000000
cpuid                                       ; largest extended function
cmp     eax, 0x80000000               ; no function > 0x80000000 ?
jbe     $no_extended_features         ; yes, no extended feature flags
or      [result], FEATURE_EXT_FEATURES ; does have ext. feature flags

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;; Step 6: Get extended feature flags
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

```



```

mov     eax, 0x80000001          ; CPUID ext. function 0x80000001
cpuid   ; EDX = extended feature flags
;::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::
;; Step 7: Extract vendor independent features from extended flags
;::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::

;; Check for 3DNow! instruction support (vendor independent)

mov     ecx, CPUID_EXT_3DNow    ; bit 31 indicates 3DNow! support
and     ecx, edx                ; supports 3DNow! ? CPUID_EXT_3DNow:0
neg     ecx                     ; supports 3DNow! ? CY : NC
sbb     ecx, ecx                ; supports 3DNow! ? 0xffffffff:0
and     ecx, FEATURE_3DNow      ; support 3DNow!?FEATURE_3DNow:0
or      [result], ecx           ; merge into feature flags

;::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::
;; Step 8: Determine CPU vendor
;::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::

lea     esi, vendorAMD          ; AMD's vendor string
lea     edi, vendor              ; this CPU's vendor string
mov     ecx, 12                  ; strings are 12 characters
cld                                         ; compare lowest to highest
repe   cmpsb                     ; current vendor string == AMD's ?
jnz     $not_AMD                 ; no, CPU vendor is not AMD

;::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::
;; Step 9: Check AMD specific extended features
;::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::

mov     ecx, CPUID_EXT_AMD_3DNowEXT ; bit 30 indicates 3DNow! ext.
and     ecx, edx                ; 3DNow! ext?
neg     ecx                     ; 3DNow! ext ? CY : NC
sbb     ecx, ecx                ; 3DNow! ext ? 0xffffffff : 0
and     ecx, FEATURE_3DNowEXT    ; 3DNow! ext?FEATURE_3DNowEXT:0
or      [result], ecx           ; merge into feature flags

test    [result], FEATURE_MMXEXT ; determined SSE MMX support?
jnz     $has_mmxext             ; yes, don't need to check again

;; Check support for AMD's multimedia instruction set additions

mov     ecx, CPUID_EXT_AMD_MMXEXT ; bit 22 indicates MMX extension
and     ecx, edx                ; MMX ext?CPUID_EXT_AMD_MMXEXT:0
neg     ecx                     ; MMX ext? CY : NC
sbb     ecx, ecx                ; MMX ext? 0xffffffff : 0
and     ecx, FEATURE_MMXEXT     ; MMX ext ? FEATURE_MMXEXT:0
or      [result], ecx           ; merge into feature flags

$has_mmxext:

```



```

        __except (EXCEPTION_EXECUTE_HANDLER) {
            return (result & (~FEATURE_SSEFP));
        }
    }
    else {
        return (result);
    }
}

/* The sample "application" */

int main (void)
{
    unsigned int capabilities = get_feature_flags();

    printf ("features = %08x\n", capabilities);
    printf ("CPU supports CPUID:      %c\n",
            capabilities & FEATURE_CPUID ? 'y' : 'n');
    printf ("CPU supports CPUID STD:      %c\n",
            capabilities & FEATURE_STD_FEATURES ? 'y' : 'n');
    printf ("CPU supports CPUID EXT:      %c\n",
            capabilities & FEATURE_EXT_FEATURES ? 'y' : 'n');
    printf ("CPU supports TSC:            %c\n",
            capabilities & FEATURE_TSC ? 'y' : 'n');
    printf ("CPU supports CMOV:          %c\n",
            capabilities & FEATURE_CMOV ? 'y' : 'n');
    printf ("CPU supports MMX:           %c\n",
            capabilities & FEATURE_MMX ? 'y' : 'n');
    printf ("CPU supports 3DNOW:         %c\n",
            capabilities & FEATURE_3DNOW ? 'y' : 'n');
    printf ("CPU supports 3DNOW_EXT:     %c\n",
            capabilities & FEATURE_3DNOWEXT ? 'y' : 'n');
    printf ("CPU supports AMD-K6-MTRR:   %c\n",
            capabilities & FEATURE_K6_MTRR ? 'y' : 'n');
    printf ("CPU supports P6-MTRR:      %c\n",
            capabilities & FEATURE_P6_MTRR ? 'y' : 'n');
    printf ("CPU supports SSE MMX:       %c\n",
            capabilities & FEATURE_MMXEXT ? 'y' : 'n');
    printf ("CPU supports SSE FPU:       %c\n",
            capabilities & FEATURE_SSEFP ? 'y' : 'n');
    return (0);
}

```

3.7.2 Example Function Call

The function call code sample detects the full range of CPUID information and allows the user to query capabilities through a simple function call. The code sample is available from AMD's website at the following URL:

http://www.amd.com/products/cpg/bin/getcpu_caps.zip

The zip file contains two files—DETECT.C and ADETECT.H. Follow these steps to use the function call:

1. Copy DETECT.C and ADETECT.H into your project directory.
2. Add DETECT.C to your source project.

Now the user can make calls to GetCPUCaps() in any module that includes ADETECT.H. Add the function call with the following statement:

```
#include "ADETECT.H"
```

This source code compiles under Microsoft® Visual Studio C/C++ Versions 5 and 6.

3.7.3 Displaying the AMD Athlon™ 64, AMD Opteron™, AMD Athlon™, and AMD Duron™ Processor Name Strings

The AMD Athlon 64 and AMD Opteron processor and all AMD Athlon and AMD Duron family of processors support CPUID extended functions 8000_0002h, 8000_0003h, and 8000_0004h. These functions return an ASCII string containing the name of the processor. These functions eliminate the need for operating systems and application software to search for the processor name in a look-up table. Instead, software can simply call these three functions to obtain the name string (up to 48 ASCII characters in little-endian format) and display it on the screen. The character string is terminated with a 00h (ASCII null character).

The following code samples illustrate methods that can be used to display the processor name string as required by the AMD Athlon 64, AMD Opteron, AMD Athlon, and AMD Duron processors branding strategy.

3.7.4 DisplayNameString Subroutine

The name string of AMD Athlon 64 and AMD Opteron processors, as well as the AMD Athlon and AMD Duron family of processors, can be displayed by calling the DisplayNameString subroutine. The following code sample displays the processor name string.

```
-----
; DisplayNameString:
;
;
; Returns:
;   cf=0 all 48 possible characters displayed
;   cf=1 end of string reached
;
-----
DisplayNameString proc near
    push  eax
    push  ebx
    push  ecx
```

```

    push  edx                ;
    mov   eax, 80000002h
    db   0Fh, 0A2h          ;CPUID instruction
    call  DisplayNameSubstring;
    jc   @f                  ;End of string?
    mov   eax, 80000003h
    db   0Fh, 0A2h          ;CPUID instruction
    call  DisplayNameSubstring;
    jc   @f                  ;End of string?
    mov   eax, 80000004h
    db   0Fh, 0A2h          ;CPUID instruction
    call  DisplayNameSubstring;
@@:   pop   edx                ;
    pop   ecx                ;
    pop   ebx                ;
    pop   eax                ;
    ret
DisplayNameString endp
;-----

```

3.7.5 DisplayNameSubstring

The `DisplayNameSubstring` subroutine is called up to three times to display the ASCII characters returned by each CPUID function call.

```

;-----
; DisplayNameSubstring:
;
;
; Returns:
;   cf=0 no errors
;   cf=1 end of string reached
;-----
DisplayNameSubstring proc near;Displays eax, ebx, ecx, edx
    call  DisplayEaxAscii    ; eax
    jc   @f                  ;End of string?
    xchg  eax, ebx          ;
    call  DisplayEaxAscii    ; ebx
    jc   @f                  ;End of string?
    xchg  eax, ecx          ;
    call  DisplayEaxAscii    ; ecx
    jc   @f                  ;End of string?
    xchg  eax, edx          ;
    call  DisplayEaxAscii    ; edx
@@:   ret
DisplayNameSubstring endp
;-----

```

DisplayEaxAscii

The DisplayNameSubstring subroutine calls the DisplayEaxAscii subroutine up to four times. DisplayEaxAscii displays the four bytes of the EAX register as ASCII characters starting with the least-significant byte (little endian). The subroutine DisplayAlChar used in the example is a generic name for a subroutine that displays the value in the AL register as an ASCII character. This type of subroutine is common to all type of BIOS under a variety of names.

```
-----  
; DisplayEaxAscii:  
;  
; Returns:  
;   cf=0 no errors  
;   cf=1 end of string reached  
-----  
DisplayEaxAscii proc near      ;  
    push  eax                    ;  
    push  cx                     ;  
    mov   cx, 4                  ;  
;  
-----;   
@@:  or    al, al                ;End of string?  
     stc                      ;(assume end of string)  
     jz   @f                    ; YES--assumed correctly  
     call DisplayAlChar        ; NO---display character  
     ror  eax, 8                ;next char in al  
     loop @b                    ;repeat  
;  
-----;   
     cld                        ;  
@@:  pop   cx                    ;Restore regs  
     pop   eax                  ;  
     ret                        ;  
DisplayEaxAscii endp          ;  
-----;
```

Chapter 4 Summary of CUID Differences

The CUID instruction provides complete information about the processor (vendor, type, name, etc.) and its features. The CUID instruction is designed to be flexible and extensible, so that it can provide new information for future generations of processors.

AMD Athlon™ 64 and AMD Opteron™ processors introduce several new CUID functions, as well as changes to existing functions. This section summarizes new features and changes.

Chapter 5 “CUID Instruction Definition” for a detailed description of each CUID function.

4.1 Changed Functions

The CUID instruction implements multiple functions, each providing information about specific processor features. The following sections describe changes to the CUID functions as they exist on the AMD Athlon™ and the AMD Duron™ family of processors.

4.1.1 Standard Function 0000_0001h—Processor Version Information and Feature Flags

Standard Function 1 has been enhanced to return the following new fields and flags.

4.1.1.1 Extended Family and Extended Model (in EAX)

These new fields, in conjunction with the existing family and model fields, expand the family and model numbering scheme to 8 bits. See “AMD Processor Signature (Extended Function)” on page 28 for important information about calculating and displaying family and model numbers for the AMD Athlon 64 and AMD Opteron processors.

4.1.1.2 8-Bit Brand ID (in EBX)

On certain models, the brand ID is an 8-bit field that identifies a processor with a unique set of features as a specific brand. Other models have a 12-bit Brand ID. See “12-Bit Brand ID (in EBX)” on page 48 for details. The BIOS can use the 8-bit or 12-bit brand ID to program the ASCII processor name string to be returned by CUID functions 8000_0002h, 8000_0003h, and 8000_0004h. See “8-Bit Brand ID” on page 54 for details.

4.1.1.3 CLFLUSH size (in EBX)

This field reports the size of the cache line flushed by the CLFLUSH instruction. See “CLFLUSH Size” on page 54 for details.

4.1.1.4 Initial APIC_ID (in EBX)

The Initial APIC ID field reports the node ID. See “Initial APIC_ID” on page 54 for details.

4.1.1.5 Standard Feature Flags (in EDX)

The AMD Athlon 64 and AMD Opteron processors report the same standard features as the AMD Athlon XP processor, with the following additions:

| | |
|------------|---------------------|
| EDX bit 19 | CLFLUSH instruction |
| EDX bit 26 | SSE2 |

4.1.2 Extended Function 8000_0000h—Highest Extended Function Available

The AMD Athlon 64 and AMD Opteron processors return 8000_0018h as the highest extended function available.

4.1.3 Extended Function 8000_0001h—Processor Version Information and Extended Feature Flags

Extended Function 8000_0001h has been enhanced to return several new fields and flags.

4.1.3.1 Extended Family and Extended Model (in EAX)

These new fields, in conjunction with the existing family and model fields, expand the family and model numbering scheme to 8 bits. See “AMD Processor Signature (Extended Function)” on page 28 for important information on calculating and displaying the family and model numbers for AMD Athlon 64 and AMD Opteron processors.

4.1.3.2 12-Bit Brand ID (in EBX)

On certain models, the brand ID is a 12-bit field that identifies a processor with a unique set of features as a specific brand. Other models have an 8-bit brand ID. See “8-Bit Brand ID (in EBX)” on page 47 for details. The BIOS can use the 8-bit or 12-bit brand ID to program the ASCII processor name string to be returned by CPUID functions 8000_0002h, 8000_0003h, and 8000_0004h. See “EBX—12-bit Brand ID” on page 61 for details.

4.1.3.3 Extended Feature Flags (in EDX)

The AMD Athlon 64 and AMD Opteron processors add these new extended feature flags:

| | |
|------------|----------------------------------|
| EDX bit 20 | No-execute page protections (NX) |
| EDX bit 29 | Long Mode capable (LM) |

See “Function 8000_0001h—Processor Version Information and Extended Feature Flags” on page 60 for details.

4.1.4 Extended Functions 8000_0005h and 8000_0006h—Cache and TLB Information

These functions return information about the processor TLBs and caches. The format for the information returned by these functions is identical to the AMD Athlon and the AMD Duron processors, although the field values may differ. See “Extended Function 8000_0005h—L1 Cache and L1 TLB Information for AMD Athlon™ 64, AMD Opteron™, AMD Athlon™, and AMD Duron™ Processors” on page 70 and “Extended Function 8000_0006h—L2 Cache and L2 TLB Information for the AMD Athlon™ 64 and AMD Opteron™, AMD Athlon™, and AMD Duron™ Processors” on page 72 for details.

4.1.5 Extended Function 8000_0007h—Advanced Power Management Information

This function returns the following new flag:

| | |
|-----------|--------------------|
| EDX bit 3 | Thermal Trip (TTP) |
|-----------|--------------------|

4.1.6 Extended Function 8000_0008h—Address Size Information

The AMD Athlon 64 and AMD Opteron processors return 48 bits (30h) for the maximum linear address (Virtual Address) size and 40 bits (28h) for the maximum physical address size. See “Function 8000_0008h — Physical Address and Linear Address Size” on page 76 for details.

4.2 New Functions

The AMD Athlon 64 and AMD Opteron processors introduce several new extended CPUID functions.

4.2.1 Extended Functions 8000_0009h–8000_0018h—Vendor-Specific Feature Flags

Functions 8000_0009h through 8000_0018h are reserved for future expansion of vendor-specific feature flags. Each function is reserved for a specific vendor. See “Extended Functions 8000_0009h–8000_0018h—Vendor-Specific Feature Flags” on page 77 for details.

Chapter 5 CPUID Instruction Definition

This chapter contains a detailed description of the CPUID instruction.

5.1 CPUID Instruction

| <i>Mnemonic</i> | <i>Opcode</i> | <i>Description</i> |
|-----------------------|--------------------|--|
| CPUID | 0F A2h | Identify the processor and its feature set |
| Privilege: | none | |
| Registers Affected: | EAX, EBX, ECX, EDX | |
| Flags Affected: | none | |
| Exceptions Generated: | none | |

The CPUID instruction is an application-level instruction that software executes to identify the processor and its feature set. This instruction offers multiple functions, each providing a different set of information about the processor. The CPUID instruction can be executed from any privilege level. Software can use the information returned by this instruction to tune its functionality for the specific processor and its features.

Not all processors implement the CPUID instruction. Therefore, software must test to determine if the instruction is present on the processor. If the ID bit (21) in the EFLAGS register is writeable, the CPUID instruction is implemented.

The CPUID instruction supports multiple functions. The information associated with each function is obtained by executing the CPUID instruction with the function number in the EAX register. Functions are divided into two types: standard functions and extended functions. Standard functions are found in the low function space, 0000_0000h through 7FFF_FFFFh. In general, all x86 processors have the same standard function definitions.

Extended functions are defined specifically for processors supplied by the vendor listed in the vendor identification string. Extended functions are found in the high function space, 8000_0000h through 8FFF_FFFFh. Because not all vendors have defined extended functions, software must test for their presence on the processor. AMD processors have extended functions if the 8000_0000h function returns a value of at least 8000_0001h in the EAX register.

5.2 Standard Functions

Standard functions provide a simple method for software to access information common to all x86 ISA processors.

5.2.1 Function 0—Largest Standard Function Input Value and Vendor Identification String

Input: EAX = 0

Output: EAX = Largest function input value recognized by the CPUID instruction
EBX, EDX, ECX = Vendor identification string

This is a standard function found in all processors implementing the CPUID instruction. It returns two values. The first value is returned in the EAX register and indicates the largest standard function value recognized by the processor. The second value is the vendor identification string. This 12-character ASCII string is returned in the EBX, EDX, and ECX registers in little endian format. AMD processors return a vendor identification string of “AuthenticAMD” as follows:

| EBX | EDX | ECX | |
|-------------|-------------|-------------|--------------------|
| h t u A | i t n e | D M A c | ← Registers |
| 68 74 75 41 | 69 74 6E 65 | 44 4D 41 63 | ← Alpha Characters |
| | | | ← ASCII Codes |

Software uses the vendor identification string as follows:

- To identify the processor as an AMD processor
- To apply AMD’s definition of the CPUID instruction for all additional function calls

5.2.2 Function 1—Processor Signature and Standard Feature Flags

Function 1 returns two values—the Processor Signature and the Standard Feature Flags.

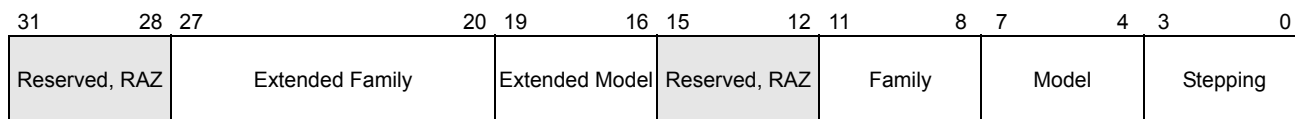
Input: EAX = 0000_0001h

Output: EAX = Version (family, model and stepping) information
EBX = 8-Bit Brand ID, CLFLUSH and APIC information¹
ECX = 0 (Reserved)
EDX = Standard Feature Flags

Note: 1. EBX is Reserved in the AMD Athlon™, AMD Duron™, and earlier AMD processors

5.2.2.1 EAX—Version (Family, Model and Stepping) Information

A processor belongs to a certain family of processors (for example—AMD-K6[®] microprocessor, AMD Athlon, AMD Athlon 64 and AMD Opteron™ processors). Within that family, several models may exist. Additionally, each processor has a stepping or revision number. This function returns information about the processor instruction family, model, and stepping numbers in the EAX register, as shown in Figure 2.



| Bits | Mnemonic | Definition |
|-------|------------------------------|---|
| 31–28 | Reserved | RAZ |
| 27–20 | Extended Family ¹ | If (Family = 0Fh), provides additional family information |
| 19–16 | Extended Model ¹ | If (Family = 0Fh), provides additional model information |
| 15–12 | Reserved | RAZ |
| 11–8 | Family | Processor/Instruction Family |
| 7–4 | Model | Processor Model |
| 3–0 | Stepping | Processor Stepping (revision) |

Note: 1. These bits are only returned for the AMD Athlon™ 64 and AMD Opteron™ processors. For the AMD Athlon™ and AMD Duron™ processors these bits are reserved.

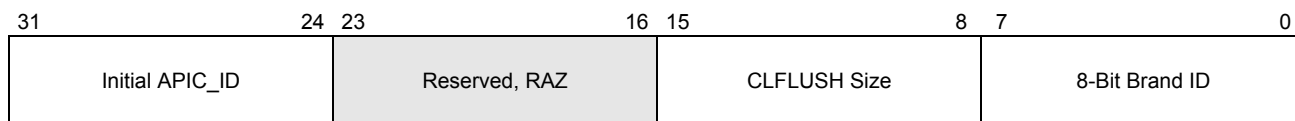
Figure 2. EAX Bit Fields for Standard Function 0000_0001h and Extended Function 8000_0001h

The *extended family* and *extended model* fields are new to the AMD Athlon 64 and AMD Opteron processors and will be implemented in all future processor families.

These fields, in conjunction with the existing family and stepping fields, form an 8-bit *effective family* and *effective model* number as described in “AMD Processor Signature (Extended Function)” on page 28.

5.2.2.2 EBX—8-Bit Brand ID, CFLUSH, and APIC Information

This function returns information regarding the processor brand in the EBX register, along with CLFLUSH and APIC information, as shown in Figure 3.



| Bits | Mnemonic | Description |
|-------|-----------------|--------------------------------|
| 31-24 | Initial APIC_ID | Initial local APIC physical ID |
| 23-16 | Reserved | RAZ |
| 15-8 | CLFLUSH Size | Cache line size (in quadwords) |
| 7-0 | 8-Bit Brand ID | Processor Brand Identification |

Figure 3. EBX Bit Fields for Standard Function 0000_0001h

5.2.2.2.1 8-Bit Brand ID

On certain models, the brand ID is an 8-bit field that identifies a processor with a unique set of features as a specific brand. Other models have a 12-bit brand ID. See “EBX—12-bit Brand ID” on page 61 for details. The BIOS can use the 8-bit or 12-bit brand ID to program the processor’s ASCII name string to be returned by CPUID functions 8000_0002h, 8000_0003h, and 8000_0004h. See “Extended Functions 8000_0002h, 8000_0003h, and 8000_0004h—Processor Name String” on page 69 for details. A value of 0 in this field indicates either that the processor reports a 12-bit brand ID through CPUID function 8000_0001h or that it is an engineering sample.

BIOS programmers should see Appendix B on page 95 for information about the procedure to program the processor name string that corresponds to each brand ID value.

This field is new to the AMD Opteron processors.

5.2.2.2.2 CLFLUSH Size

The 8-bit CLFLUSH Size field reports the size of the cache line flushed by the CLFLUSH instruction. The number reported is the cache line size in quadword (8-byte) increments.

This field is implemented only if the CLFLUSH instruction is supported. Software must test the CLFLUSH feature bit in the standard feature flags returned in EDX to determine if the CLFLUSH instruction is implemented. For information about the returned flag values, see “EDX—Standard Feature Flags.”

This field is new to the AMD Athlon 64 and AMD Opteron processors.

5.2.2.2.3 Initial APIC_ID

The 8-bit initial APIC_ID field contains the initial value of the processor’s local APIC physical ID. The AMD Athlon 64 and AMD Opteron processors derive the initial value of the local APIC physical ID from the node ID.

Subsequent writes by software to the local APIC ID register do not change the initial APIC ID value returned by the CPUID instruction, as shown in Table 9. This value continues to reflect the node ID.

Table 9. Initial APIC_ID Bit Definitions

| Bit | Name | Function |
|-------|----------|----------|
| 26–24 | NodeID | Node ID |
| 31–27 | Reserved | |

This field is new to the AMD Athlon 64 and AMD Opteron processors.

5.2.2.3 EDX—Standard Feature Flags

The standard feature flags are returned in the EDX register and indicate the presence of specific features. In most cases, a “1” indicates the feature is present, and a “0” indicates the feature is not present.

Table 10 on page 55 contains a list of the currently defined standard feature flags for the AMD Athlon 64 and AMD Opteron processors. Table 11 on page 57 contains a list of the currently defined standard feature flags for the AMD Athlon family of processors. Table 12 on page 58 contains a list of the currently defined standard feature flags for the AMD Duron family of processors. Table 13 on page 59 contains a list of the currently defined standard feature flags for the AMD-K6[®] processor models 8 and 9. (See Table 32 through Table 36 in Appendix A, “Register Values Returned by the AMD Family Processors,” for all K86 family processor register definitions, including the AMD-K6 processor models 6 and 7.) Reserved bits will be used for new features as they are added. For more information, see Chapter 2, “CPLID Instruction Overview”.

Table 10. Standard Feature Flag Descriptions for AMD Athlon™ 64 and AMD Opteron™ Processors

| Bit | Feature ¹ | AMD Athlon™ 64 and AMD Opteron™ Processors |
|-----|---|--|
| | | Models 0, 1, 4, 5, and 8 |
| 0 | Floating-Point Unit | 1 |
| 1 | Virtual Mode Extensions | 1 |
| 2 | Debugging Extensions | 1 |
| 3 | Page Size Extensions (4-Mbyte pages) | 1 |
| 4 | Time Stamp Counter (with RDTSC and CR4 disable bit) | 1 |
| 5 | AMD K86 Family of Processors Model-Specific Registers (with RDMSR and WRMSR) | 1 |
| 6 | PAE (Page Address Extensions) | 1 |

Notes:

1. Bit definitions: 0 = No Support, 1 = Support.
2. The AMD processor contains a local APIC. The BIOS must enable the local APIC for bit 9 to return a 1 (supported).
3. The SYSENTER and SYSEXIT instructions have different implementations than the SYSCALL and SYSRET instructions.

Table 10. Standard Feature Flag Descriptions for AMD Athlon™ 64 and AMD Opteron™ Processors (Continued)

| Bit | Feature ¹ | AMD Athlon™ 64 and AMD Opteron™ Processors |
|-------|--|--|
| | | Models 0, 1, 4, 5, and 8 |
| 7 | Machine Check Exception | 1 |
| 8 | CMPXCHG8B Instruction | 1 |
| 9 | APIC | 1 ² |
| 10 | Reserved on all AMD processors | 0 |
| 11 | SYSENTER/SYSEXIT Instructions ³ | 1 |
| 12 | MTRR (Memory Type Range Registers) | 1 |
| 13 | Global Paging Extension | 1 |
| 14 | Machine Check Architecture | 1 |
| 15 | Conditional Move Instruction | 1 |
| 16 | PAT (Page Attribute Table) | 1 |
| 17 | PSE-36 (Page Size Extensions) | 1 |
| 18 | Reserved on all AMD processors | 0 |
| 19 | CLFLUSH Instruction | 1 |
| 20–22 | Reserved on all AMD processors | 0 |
| 23 | MMX™ Instructions | 1 |
| 24 | FXSAVE/FXRSTOR | 1 |
| 25 | SSE Instructions | 1 |
| 26 | SSE2 | 1 |
| 27–31 | Reserved on all AMD processors | 0 |

Notes:

1. Bit definitions: 0 = No Support, 1 = Support.
2. The AMD processor contains a local APIC. The BIOS must enable the local APIC for bit 9 to return a 1 (supported).
3. The SYSENTER and SYSEXIT instructions have different implementations than the SYSCALL and SYSRET instructions.

Table 11. Standard Feature Flag Descriptions for AMD Athlon™ Processors

| Bit | Feature ¹ | AMD Athlon™ Processor | | | | | |
|-------|--|-----------------------|----------------|----------------|----------------|----------------|----------------|
| | | Model 1 | Model 2 | Model 4 | Model 6 | Model 8 | Model 10 |
| 0 | Floating-Point Unit | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | Virtual Mode Extensions | 1 | 1 | 1 | 1 | 1 | 1 |
| 2 | Debugging Extensions | 1 | 1 | 1 | 1 | 1 | 1 |
| 3 | Page Size Extensions (4-Mbyte pages) | 1 | 1 | 1 | 1 | 1 | 1 |
| 4 | Time Stamp Counter (with RDTSC and CR4 disable bit) | 1 | 1 | 1 | 1 | 1 | 1 |
| 5 | AMD K86 Family of Processors Model-Specific Registers (with RDMSR and WRMSR) | 1 | 1 | 1 | 1 | 1 | 1 |
| 6 | PAE (Page Address Extensions) | 1 | 1 | 1 | 1 | 1 | 1 |
| 7 | Machine Check Exception | 1 | 1 | 1 | 1 | 1 | 1 |
| 8 | CMPXCHG8B Instruction | 1 | 1 | 1 | 1 | 1 | 1 |
| 9 | APIC | 0 | 1 ² | 1 ² | 1 ² | 1 ² | 1 ² |
| 10 | Reserved on all AMD processors | 0 | 0 | 0 | 0 | 0 | 0 |
| 11 | SYSENTER/SYSEXIT ³ | 1 | 1 | 1 | 1 | 1 | 1 |
| 12 | MTRR (Memory Type Range Registers) | 1 | 1 | 1 | 1 | 1 | 1 |
| 13 | Global Paging Extension | 1 | 1 | 1 | 1 | 1 | 1 |
| 14 | Machine Check Architecture | 1 | 1 | 1 | 1 | 1 | 1 |
| 15 | Conditional Move Instruction | 1 | 1 | 1 | 1 | 1 | 1 |
| 16 | PAT (Page Attribute Table) | 1 | 1 | 1 | 1 | 1 | 1 |
| 17 | PSE-36 (Page Size Extensions) | 0 | 1 | 1 | 1 | 1 | 1 |
| 18–22 | Reserved on all AMD processors | 0 | 0 | 0 | 0 | 0 | 0 |
| 23 | MMX™ Instructions | 1 | 1 | 1 | 1 | 1 | 1 |
| 24 | FXSAVE/FXRSTOR | 0 | 1 | 1 | 1 | 1 | 1 |
| 25 | SSE Instructions ⁴ | 0 | 0 | 0 | 1 | 1 | 1 |
| 26–31 | Reserved on all AMD processors | 0 | 0 | 0 | 0 | 0 | 0 |

Notes:

1. Bit definitions: 0 = No Support, 1 = Support.
2. The AMD processor contains a local APIC. The BIOS must enable the local APIC in order for bit 9 to return a 1 (supported).
3. The SYSENTER and SYSEXIT instructions have different implementations than the SYSCALL and SYSRET instructions.
4. SSE instruction support is only present when the processor is set up to support it by the BIOS. See the AMD Athlon™ and AMD Duron™ Processor BIOS, Software, and Debug Developers Guide, order# 21656.

Table 12. Standard Feature Flag Descriptions for AMD Duron™ Processors

| Bit | Feature ¹ | AMD Duron™ Processor | | |
|-------|--|----------------------|----------------|----------------|
| | | Model 3 | Model 6 | Model 7 |
| 0 | Floating-Point Unit | 1 | 1 | 1 |
| 1 | Virtual Mode Extensions | 1 | 1 | 1 |
| 2 | Debugging Extensions | 1 | 1 | 1 |
| 3 | Page Size Extensions (4-Mbyte pages) | 1 | 1 | 1 |
| 4 | Time Stamp Counter (with RDTSC and CR4 disable bit) | 1 | 1 | 1 |
| 5 | AMD K86 Family of Processors Model-Specific Registers (with RDMSR and WRMSR) | 1 | 1 | 1 |
| 6 | PAE (Page Address Extensions) | 1 | 1 | 1 |
| 7 | Machine Check Exception | 1 | 1 | 1 |
| 8 | CMPXCHG8B Instruction | 1 | 1 | 1 |
| 9 | APIC | 1 ² | 1 ² | 1 ² |
| 10 | Reserved on all AMD processors | 0 | 0 | 0 |
| 11 | SYSENTER/SYSEXIT ³ | 1 | 1 | 1 |
| 12 | MTRR (Memory Type Range Registers) | 1 | 1 | 1 |
| 13 | Global Paging Extension | 1 | 1 | 1 |
| 14 | Machine Check Architecture | 1 | 1 | 1 |
| 15 | Conditional Move Instruction | 1 | 1 | 1 |
| 16 | PAT (Page Attribute Table) | 1 | 1 | 1 |
| 17 | PSE-36 (Page Size Extensions) | 1 | 1 | 1 |
| 18–22 | Reserved on all AMD processors | 0 | 0 | 0 |
| 23 | MMX™ Instructions | 1 | 1 | 1 |
| 24 | FXSAVE/FXRSTOR | 1 | 1 | 1 |
| 25 | SSE Instructions ⁴ | 0 | 1 | 1 |
| 26–31 | Reserved on all AMD processors | 0 | 0 | 0 |

Notes:

1. Bit definitions: 0 = No Support, 1 = Support.
2. The AMD processor contains a local APIC. The BIOS must enable the local APIC in order for bit 9 to return a 1 (supported).
3. The SYSENTER and SYSEXIT instructions have different implementations than the SYSCALL and SYSRET instructions.
4. SSE instruction support is only present when the processor is set up to support it by the BIOS. See the AMD Athlon™ and AMD Duron™ Processor BIOS, Software, and Debug Developers Guide, order# 21656.

Table 13. Standard Feature Flag Descriptions for AMD-K6[®]-2 and AMD-K6[®]-III Processors

| Bit | Feature ¹ | AMD-K6 [®] -2 Processor (Model 8) | AMD-K6 [®] -III Processor (Model 9) |
|-----------|--|--|--|
| 0 | Floating-Point Unit | 1 | 1 |
| 1 | Virtual Mode Extensions | 1 | 1 |
| 2 | Debugging Extensions | 1 | 1 |
| 3 | Page Size Extensions (4-Mbyte pages) | 1 | 1 |
| 4 | Time Stamp Counter (with RDTSC and CR4 disable bit) | 1 | 1 |
| 5 | K86 Family of Processors Model-Specific Registers (with RDMSR and WRMSR) | 1 | 1 |
| 6 | PAE (Page Address Extensions) | 0 | 0 |
| 7 | Machine Check Exception | 1 | 1 |
| 8 | CMPXCHG8B Instruction | 1 | 1 |
| 9 | APIC | 0 | 0 |
| 10 | Reserved on all AMD-K6 [®] processors | 0 | 0 |
| 11 | SYSENTER/SYSEXIT ² | 0 | 0 |
| 12 | Memory Type Range Registers | 0 | 0 |
| 13 | Global Paging Extension | 1 ³ | 1 |
| 14 | Machine Check Architecture | 0 | 0 |
| 15 | Conditional Move Instruction | 0 | 0 |
| 16 | PAT (Page Attribute Table) | 0 | 0 |
| 17 | PSE-36 (Page Size Extensions) | 0 | 0 |
| 18– 22 | Reserved on all AMD-K6 processors | 0 | 0 |
| 23 | MMX™ Instructions | 1 | 1 |
| 24 | FXSAVE/FXRSTOR | 0 | 0 |
| 25– 31 | Reserved on all AMD-K6 processors | 0 | 0 |

Notes:

1. Bit definitions: 0 = No Support, 1 = Support.
2. The SYSENTER and SYSEXIT instructions have different implementations than the SYSCALL and SYSRET instructions.
3. See Table 35 on page 91 for more information about Global Paging Extensions in the AMD-K6[®]-2 processor model 8.

5.3 Extended Functions

Extended functions provide information on extensions specific to a vendor's processor.

5.3.1 Function 8000_0000h—Largest Extended Function Input Value

Extended function 8000_0000h returns the highest extended function input value defined for the processor. Software must test for the existence of extended functions by using this function. If the value (reported in EAX) is at least 8000_0000h, the processor supports extended functions.

Input: EAX = 8000_0000h

Output: EAX = 8000_0018h

EBX = Reserved

ECX = Reserved

EDX = Reserved

5.3.2 Function 8000_0001h—Processor Version Information and Extended Feature Flags

Function 8000_0001h of the CUID instruction returns two types of information about the processor—version and features. The version information identifies the specific processor by providing its family, model, and revision (stepping). This information is the same as that provided by function 1. This function also returns the extended feature flags, which indicate the presence of specific features introduced in AMD processors.

Input: EAX = 8000_0001h

Output: EAX = Version (family, model, and stepping) information

EBX = 0 or 12-bit Brand ID¹

ECX = 0 (Reserved for Future Features)

EDX = Extended Feature Flags

Note: 1. This EBX field is only returned for the AMD Athlon™ 64 and AMD Opteron™ processors. It is reserved on the AMD Athlon™, AMD Duron™, and earlier AMD processors.

5.3.2.1 EAX—Version (Family, Model, and Stepping) Information

A processor belongs to a certain family of processors (for example—AMD-K6 microprocessor, AMD Athlon, and AMD Athlon 64 and AMD Opteron processors). Within that family, several models may exist. Additionally each processor has a revision number or stepping number. This function returns information about the processor instruction family, model, and stepping numbers in the EAX register.

This information is identical to that returned in EAX by standard function 1. For a diagram of the EAX bit fields, see Figure 2 on page 53.

5.3.2.2 EBX—12-bit Brand ID

On certain models of the AMD Athlon 64 and AMD Opteron processors, the brand ID is a 12-bit field that identifies a processor with a unique set of features as a specific brand. Other models have an 8-bit brand ID. See “8-Bit Brand ID” on page 54 for details. The BIOS can use the 8-bit or 12-bit brand ID to program the processor’s ASCII name string to be returned by CPUID functions 8000_0002h, 8000_0003h, and 8000_0004h. See “Extended Functions 8000_0002h, 8000_0003h, and 8000_0004h—Processor Name String” on page 69 for details. A value of 0 in this field indicates either that the processor reports an 8-bit brand ID through CPUID function 0000_0001h or that it is an engineering sample.

BIOS programmers should see Appendix B, “Programming the Name String of the AMD Athlon™ 64 and AMD Opteron™ Processors” on page 95, for information about the procedure to program the processor name string that corresponds to each Brand ID value.

This field is new to the AMD Athlon 64 and AMD Opteron processors. This bit is reserved on the AMD Athlon, AMD Duron, and earlier AMD processors.

5.3.2.3 ECX—Extended Feature Flag

ECX is reserved for future AMD features.

5.3.2.4 EDX—Extended Feature Flags

The extended feature flags are returned in the EDX register. Each bit corresponds to a specific feature. A ‘1’ indicates that the feature is present, and a ‘0’ indicates that feature is not present.

Most of the standard feature bits from function 1 (See “Function 1—Processor Signature and Standard Feature Flags” on page 52) are replicated in the extended feature flags, along with bits for specific AMD extensions to the x86 architecture. See Table 18 for a list of the differences between the standard function feature flags and the extended function feature flags.

Table 14 on page 62 shows the complete extended feature flags for the AMD Athlon 64 and AMD Opteron processors.

Table 14. Extended Feature Flags—AMD Athlon™ 64 and AMD Opteron™ Processors

| Bit | Feature ¹ | AMD Athlon™ 64 and AMD Opteron™ Processors |
|-----|--|--|
| | | Models 0, 1, 4, 5, and 8 |
| 0 | Floating-Point Unit | 1 |
| 1 | Virtual Mode Extensions | 1 |
| 2 | Debugging Extensions | 1 |
| 3 | Page Size Extensions (4-Mbyte Pages) | 1 |
| 4 | Time Stamp Counter (with RDTSC and CR4 disable bit) | 1 |
| 5 | AMD K86 Family of Processors Model-Specific Registers (with RDMSR and WRMSR) | 1 |
| 6 | PAE (Page Address Extensions) | 1 |
| 7 | Machine Check Exception | 1 |
| 8 | CMPXCHG8B Instruction | 1 |
| 9 | APIC | 1 ² |
| 10 | Reserved on all AMD processors | 0 |
| 11 | SYSCALL and SYSRET Instructions ³ | 1 |
| 12 | MTRR (Memory Type Range Registers) | 1 |
| 13 | Global Paging Extension | 1 |
| 14 | Machine Check Architecture | 1 |
| 15 | Conditional Move Instruction | 1 |
| 16 | PAT (Page Attribute Table) | 1 |
| 17 | PSE-36 (Page Size Extensions) | 1 |
| 18 | Reserved on all AMD Athlon™ 64 and AMD Opteron™ processors | 0 |
| 19 | Reserved on all AMD Athlon 64 and AMD Opteron processors | 0 |
| 20 | No-execute Page Protection (NX) | 1 |
| 21 | Reserved on all AMD processors | 0 |

Notes:

1. Bit definitions: 0 = No Support, 1 = Support.
2. The AMD processor contains a local APIC. The BIOS must enable the local APIC in order for bit 9 to return a 1 (supported).
3. The implementation of the SYSCALL and SYSRET instructions is the same on the AMD Athlon 64 and AMD Opteron processors, AMD Athlon, AMD Duron processor and the AMD-K6® processor models 8 through D. The SYSENTER and SYSEXIT instructions have different implementations than the SYSCALL and SYSRET instructions.

Table 14. Extended Feature Flags—AMD Athlon™ 64 and AMD Opteron™ Processors (Continued)

| Bit | Feature ¹ | AMD Athlon™ 64 and AMD Opteron™ Processors |
|-------|--|--|
| | | Models 0, 1, 4, 5, and 8 |
| 22 | AMD Extensions to the MMX™ Instruction Set | 1 |
| 23 | MMX Instructions | 1 |
| 24 | FXSAVE/FXRSTOR Instructions | 1 |
| 25–28 | Reserved on all AMD processors | 0 |
| 29 | Long Mode Capable (LM) | 1 |
| 30 | 3DNow!™ Instruction Extensions | 1 |
| 31 | 3DNow! Instructions | 1 |

Notes:

1. Bit definitions: 0 = No Support, 1 = Support.
2. The AMD processor contains a local APIC. The BIOS must enable the local APIC in order for bit 9 to return a 1 (supported).
3. The implementation of the SYSCALL and SYSRET instructions is the same on the AMD Athlon 64 and AMD Opteron processors, AMD Athlon, AMD Duron processor and the AMD-K6[®] processor models 8 through D. The SYSENTER and SYSEXIT instructions have different implementations than the SYSCALL and SYSRET instructions.

Table 15 contains a list of the currently defined feature flags for the AMD Athlon processors.

Table 15. Extended Feature Flag Descriptions for AMD Athlon™ Processors

| Bit | Feature ¹ | AMD Athlon™ Processor | | | | | |
|-----|--|-----------------------|----------------|----------------|----------------|----------------|----------------|
| | | Model 1 | Model 2 | Model 4 | Model 6 | Model 8 | Model 10 |
| 0 | Floating-Point Unit | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | Virtual Mode Extensions | 1 | 1 | 1 | 1 | 1 | 1 |
| 2 | Debugging Extensions | 1 | 1 | 1 | 1 | 1 | 1 |
| 3 | Page Size Extensions (4-Mbyte Pages) | 1 | 1 | 1 | 1 | 1 | 1 |
| 4 | Time Stamp Counter (with RDTSC and CR4 disable bit) | 1 | 1 | 1 | 1 | 1 | 1 |
| 5 | AMD K86 Family of Processors Model-Specific Registers (with RDMSR and WRMSR) | 1 | 1 | 1 | 1 | 1 | 1 |
| 6 | PAE (Page Address Extensions) | 1 | 1 | 1 | 1 | 1 | 1 |
| 7 | Machine Check Exception | 1 | 1 | 1 | 1 | 1 | 1 |
| 8 | CMPXCHG8B Instruction | 1 | 1 | 1 | 1 | 1 | 1 |
| 9 | APIC | 0 | 1 ² | 1 ² | 1 ² | 1 ² | 1 ² |
| 10 | Reserved on all AMD processors | 0 | 0 | 0 | 0 | 0 | 0 |
| 11 | SYSCALL and SYSRET Instructions ³ | 1 | 1 | 1 | 1 | 1 | 1 |
| 12 | MTRR (Memory Type Range Registers) | 1 | 1 | 1 | 1 | 1 | 1 |
| 13 | Global Paging Extension | 1 | 1 | 1 | 1 | 1 | 1 |
| 14 | Machine Check Architecture | 1 | 1 | 1 | 1 | 1 | 1 |
| 15 | Conditional Move Instruction | 1 | 1 | 1 | 1 | 1 | 1 |
| 16 | PAT (Page Attribute Table) | 1 | 1 | 1 | 1 | 1 | 1 |
| 17 | PSE-36 (Page Size Extensions) | 0 | 1 | 1 | 1 | 1 | 1 |
| 18 | Reserved on all AMD processors | 0 | 0 | 0 | 0 | 0 | 0 |

Notes:

1. Bit definitions: 0 = No Support, 1 = Support.
2. The AMD processor contains a local APIC. The BIOS must enable the local APIC in order for bit 9 to return a 1 (supported).
3. The implementation of the SYSCALL and SYSRET instructions is the same on the AMD Athlon™ processors, the AMD Duron™ processors, as well as on the AMD-K6® processors models 8 and 9. The SYSENTER and SYSEXIT instructions have different implementations than the SYSCALL and SYSRET instructions.
4. This value is a "1" on AMD Athlon™ MP model 6 processors with a CPUID value of 662 or greater. Although the value is a "0" for all AMD Athlon MP processors model 6 with a CPUID value of 660 or 661, these processors are also multiprocessing capable. AMD reserves the right to report a "0" or a "1" for all other model 6 processors which are not tested, supported, or intended by AMD to be used for operation in multiprocessing platforms. See the AMD Athlon Processor Model 6 Revision Guide, order# 24332, for the processor revision information corresponding to these model 6 CPUID values.
5. This value is a "1" for AMD Athlon MP model 8 and model 10 processors and is a "0" for all other AMD Athlon model 8 and model 10 processors, including the AMD Athlon XP processor and mobile AMD Athlon XP processor.

Table 15. Extended Feature Flag Descriptions for AMD Athlon™ Processors (Continued)

| Bit | Feature ¹ | AMD Athlon™ Processor | | | | | |
|-------|--|-----------------------|---------|---------|----------------|----------------|----------------|
| | | Model 1 | Model 2 | Model 4 | Model 6 | Model 8 | Model 10 |
| 19 | Multiprocessing Capable | 0 | 0 | 0 | 1 ⁴ | 1 ⁵ | 1 ⁵ |
| 20–21 | Reserved on all AMD processors | 0 | 0 | 0 | 0 | 0 | 0 |
| 22 | AMD Extensions to the MMX™ Instruction Set | 1 | 1 | 1 | 1 | 1 | 1 |
| 23 | MMX Instructions | 1 | 1 | 1 | 1 | 1 | 1 |
| 24 | FXSAVE/FXRSTOR Instructions | 0 | 1 | 1 | 1 | 1 | 1 |
| 25–29 | Reserved on all AMD processors | 0 | 0 | 0 | 0 | 0 | 0 |
| 30 | 3DNow!™ Instruction Extensions | 1 | 1 | 1 | 1 | 1 | 1 |
| 31 | 3DNow! Instructions | 1 | 1 | 1 | 1 | 1 | 1 |

Notes:

1. Bit definitions: 0 = No Support, 1 = Support.
2. The AMD processor contains a local APIC. The BIOS must enable the local APIC in order for bit 9 to return a 1 (supported).
3. The implementation of the SYSCALL and SYSRET instructions is the same on the AMD Athlon™ processors, the AMD Duron™ processors, as well as on the AMD-K6® processors models 8 and 9. The SYSENTER and SYSEXIT instructions have different implementations than the SYSCALL and SYSRET instructions.
4. This value is a "1" on AMD Athlon™ MP model 6 processors with a CPUID value of 662 or greater. Although the value is a "0" for all AMD Athlon MP processors model 6 with a CPUID value of 660 or 661, these processors are also multiprocessing capable. AMD reserves the right to report a "0" or a "1" for all other model 6 processors which are not tested, supported, or intended by AMD to be used for operation in multiprocessing platforms. See the AMD Athlon Processor Model 6 Revision Guide, order# 24332, for the processor revision information corresponding to these model 6 CPUID values.
5. This value is a "1" for AMD Athlon MP model 8 and model 10 processors and is a "0" for all other AMD Athlon model 8 and model 10 processors, including the AMD Athlon XP processor and mobile AMD Athlon XP processor.

Table 16 contains a list of the currently defined feature flags for the AMD Duron processor.

Table 16. Extended Feature Flag Descriptions for AMD Duron™ Processors

| Bit | Feature ¹ | AMD Duron™ Processor | | |
|-----|--|----------------------|----------------|----------------|
| | | Model 3 | Model 6 | Model 7 |
| 0 | Floating-Point Unit | 1 | 1 | 1 |
| 1 | Virtual Mode Extensions | 1 | 1 | 1 |
| 2 | Debugging Extensions | 1 | 1 | 1 |
| 3 | Page Size Extensions (4-Mbyte Pages) | 1 | 1 | 1 |
| 4 | Time Stamp Counter (with RDTSC and CR4 disable bit) | 1 | 1 | 1 |
| 5 | AMD K86 Family of Processors Model-Specific Registers (with RDMSR and WRMSR) | 1 | 1 | 1 |
| 6 | PAE (Page Address Extensions) | 1 | 1 | 1 |
| 7 | Machine Check Exception | 1 | 1 | 1 |
| 8 | CMPXCHG8B Instruction | 1 | 1 | 1 |
| 9 | APIC | 1 ² | 1 ² | 1 ² |
| 10 | Reserved on all AMD processors | 0 | 0 | 0 |
| 11 | SYSCALL and SYSRET Instructions ³ | 1 | 1 | 1 |
| 12 | MTRR (Memory Type Range Registers) | 1 | 1 | 1 |
| 13 | Global Paging Extension | 1 | 1 | 1 |
| 14 | Machine Check Architecture | 1 | 1 | 1 |
| 15 | Conditional Move Instruction | 1 | 1 | 1 |
| 16 | PAT (Page Attribute Table) | 1 | 1 | 1 |
| 17 | PSE-36 (Page Size Extensions) | 1 | 1 | 1 |
| 18 | Reserved on all AMD processors | 0 | 0 | 0 |
| 19 | Multiprocessing Capable | 0 | 0 ⁴ | 0 ⁴ |

Notes:

1. Bit definitions: 0 = No Support, 1 = Support.
2. The AMD processor contains a local APIC. The BIOS must enable the local APIC in order for bit 9 to return a 1 (supported).
3. The implementation of the SYSCALL and SYSRET instructions is the same on the AMD Athlon™ processors and the AMD Duron™ processors, as well as on the AMD-K6® processors models 8 and 9. The SYSENTER and SYSEXIT instructions have different implementations than the SYSCALL and SYSRET instructions.
4. AMD reserves the right to report a "0" or a "1" for all AMD Duron model 6 and model 7 processors which are not tested, supported, or intended by AMD to be used for operation in multiprocessing platforms.

Table 16. Extended Feature Flag Descriptions for AMD Duron™ Processors (Continued)

| Bit | Feature ¹ | AMD Duron™ Processor | | |
|-------|--|----------------------|---------|---------|
| | | Model 3 | Model 6 | Model 7 |
| 20–21 | Reserved on all AMD processors | 0 | 0 | 0 |
| 22 | AMD Extensions to the MMX™ Instruction Set | 1 | 1 | 1 |
| 23 | MMX Instructions | 1 | 1 | 1 |
| 24 | FXSAVE/FXRSTOR Instructions | 1 | 1 | 1 |
| 25–29 | Reserved on all AMD processors | 0 | 0 | 0 |
| 30 | 3DNow!™ Instruction Extensions | 1 | 1 | 1 |
| 31 | 3DNow! Instructions | 1 | 1 | 1 |

Notes:

1. Bit definitions: 0 = No Support, 1 = Support.
2. The AMD processor contains a local APIC. The BIOS must enable the local APIC in order for bit 9 to return a 1 (supported).
3. The implementation of the SYSCALL and SYSRET instructions is the same on the AMD Athlon™ processors and the AMD Duron™ processors, as well as on the AMD-K6® processors models 8 and 9. The SYSENTER and SYSEXIT instructions have different implementations than the SYSCALL and SYSRET instructions.
4. AMD reserves the right to report a "0" or a "1" for all AMD Duron model 6 and model 7 processors which are not tested, supported, or intended by AMD to be used for operation in multiprocessing platforms.

Table 17 contains a list of the currently defined feature flags for the AMD-K6 processor models 8 and 9.

Table 17. Extended Feature Flag Descriptions for AMD-K6[®]-2 and AMD-K6[®]-III Processors

| Bit | Feature ¹ | AMD-K6 [®] -2 Processor (Model 8) | AMD-K6 [®] -III Processor (Model 9) |
|-------|---|--|--|
| 0 | Floating-Point Unit | 1 | 1 |
| 1 | Virtual Mode Extensions | 1 | 1 |
| 2 | Debugging Extensions | 1 | 1 |
| 3 | Page Size Extensions (4-Mbyte Pages) | 1 | 1 |
| 4 | Time Stamp Counter (with RDTSC and CR4 disable bit) | 1 | 1 |
| 5 | K86 Family of Processors' Model-Specific Registers (with RDMSR and WRMSR) | 1 | 1 |
| 6 | PAE (Page Address Extensions) | 0 | 0 |
| 7 | Machine Check Exception | 1 | 1 |
| 8 | CMPXCHG8B Instruction | 1 | 1 |
| 9 | APIC | 0 | 0 |
| 10 | Reserved on all AMD-K6 [®] processors | 0 | 0 |
| 11 | SYSCALL and SYSRET Instructions ² | 1 | 1 |
| 12 | Memory Type Range Registers | 0 | 0 |
| 13 | Global Paging Extension | 1 | 1 |
| 14 | Machine Check Architecture | 0 | 0 |
| 15 | Conditional Move Instruction | 0 | 0 |
| 16 | PAT (Page Attribute Table) | 0 | 0 |
| 17 | PSE-36 (Page Size Extensions) | 0 | 0 |
| 18–21 | Reserved on all AMD-K6 processors | 0 | 0 |
| 22 | AMD Extensions to the MMX [™] Instruction Set | 0 | 0 |
| 23 | MMX Instructions | 1 | 1 |
| 24 | FXSAVE/FXRSTOR | 0 | 0 |
| 25–29 | Reserved on all AMD-K6 processors | 0 | 0 |
| 30 | 3DNow! [™] Instruction Extensions | 0 | 0 |
| 31 | 3DNow! Instructions | 1 | 1 |

Notes:

1. Bit definitions: 0 = No Support, 1 = Support.
2. The SYSENTER and SYSEXIT instructions have different implementations than the SYSCALL and SYSRET instructions.

Before the AMD Athlon 64 and AMD Opteron processors, most standard feature bits returned by function 1 were duplicated in the extended feature flags returned by function 8000_0001h. Starting with the AMD Athlon 64 and AMD Opteron processors, new standard feature bits will not be replicated in the extended feature flags. Extended feature bits are only added for AMD extensions to the x86 architecture. Table 18 lists the differences between the standard function feature flags and the extended function feature flags.

Table 18. Standard Feature Flags Versus Extended Feature Flags

| Bit | Standard Feature Flag | Extended Feature Flag |
|-----|-----------------------------------|---------------------------------|
| 11 | SYSENTER and SYSEXIT Instructions | SYSCALL and SYSRET Instructions |
| 19 | CFLUSH Instruction | Reserved |
| 20 | Reserved | No-execute Page Protection (NX) |
| 22 | Reserved | MMX™ Instruction Extensions |
| 25 | SSE Instructions | Reserved |
| 26 | SSE2 | Reserved |
| 29 | Reserved | Long Mode Capable (LM) |
| 30 | Reserved | 3DNow!™ Instruction Extensions |
| 31 | Reserved | 3DNow! Instructions |

Features that are compatible with extensions made by other vendors will be reported in the feature function reserved for that vendor. For details, see “Extended Functions 8000_0009h–8000_0018h—Vendor-Specific Feature Flags” on page 77.

See Tables 32 through 36 in Appendix A, “Register Values Returned by the AMD Family Processors” on page 79 for all K86 family processor register definitions.

5.3.3 Extended Functions 8000_0002h, 8000_0003h, and 8000_0004h—Processor Name String

Functions 8000_0002h, 8000_0003h and 8000_0004h each return part of the processor name string in the EAX, EBX, ECX, and EDX registers.

Input: EAX = 8000_0002h, 8000_0003h, or 8000_0004h

Output: EAX = Processor Name String
 EBX = Processor Name String
 ECX = Processor Name String
 EDX = Processor Name String

These three functions use four registers to return an ASCII string of up to 48 characters in little-endian byte order. Function 8000_0002h returns the first 16 characters of the processor name. The first character resides in the least significant byte of EAX, and the last character (of this group of 16) resides in the most significant byte of EDX. Functions 8000_0003h and 8000_0004h return the

second and third group of 16 characters in a similar fashion. The ASCII NUL character (00h) indicates the end of the processor name string.

With the AMD Athlon 64 and AMD Opteron processor, the processor name string is set to NULs (ASCII 00h) upon reset and must be programmed by the BIOS during system initialization. See Appendix B “Programming the Name String of the AMD Athlon™ 64 and AMD Opteron™ Processors” for information about how to program the processor name string.

For some versions of the AMD Athlon and the AMD Duron processors, the processor name string must be reprogrammed.

5.3.4 Extended Function 8000_0005h—L1 Cache and L1 TLB Information for AMD Athlon™ 64, AMD Opteron™, AMD Athlon™, and AMD Duron™ Processors

Function 8000_0005h returns L1 cache and L1 TLB information.

Input: EAX = 8000_0005h

Output: EAX = L1 TLB Large Page Information
 EBX = L1 TLB 4-Kbyte Page Information
 ECX = L1 Data Cache Information
 EDX = L1 Instruction Cache Information

Function 8000_0005h returns information about the processor L1 TLBs and caches. The format for the information returned by the 8000_0005h function for the AMD Athlon 64 and AMD Opteron processors is the same as the format used by AMD Athlon and the AMD Duron processors, although the field values may differ. Table 19 through Table 22 on page 71 list the values returned by function 8000_0005h for the AMD Athlon 64 and AMD Opteron, AMD Athlon, and the AMD Duron processors.

Table 19. EAX Format Returned by Function 8000_0005h

| | Two-Mbyte/4-Mbyte Pages | | | |
|-----|----------------------------|------------------------|----------------------------|------------------------|
| | Data TLB | | Instruction TLB | |
| | Associativity ¹ | # Entries ² | Associativity ¹ | # Entries ² |
| EAX | Bits 31–24 | Bits 23–16 | Bits 15–8 | Bits 7–0 |

Notes:

1. See “Associativity for L1 Caches and L1 TLBs” on page 74 for more information.
2. The number of entries returned is the number of entries available for 2-Mbyte large pages. Because 4-Mbyte large pages require two 2-Mbyte entries, the number of entries available for 4-Mbyte large pages is one-half the returned value.

Table 20. EBX Format Returned by Function 8000_0005h

| | Four-Kbyte Pages | | | |
|-----|------------------|------------|-----------------|-----------|
| | Data TLB | | Instruction TLB | |
| | Associativity* | # Entries | Associativity* | # Entries |
| EBX | Bits 31–24 | Bits 23–16 | Bits 15–8 | Bits 7–0 |

Note:
* See “Associativity for L1 Caches and L1 TLBs” on page 74 for more information.

Table 21. ECX Format Returned by Function 8000_0005h

| | L1 Data Cache | | | |
|-----|---------------|----------------|---------------|-------------------|
| | Size (Kbytes) | Associativity* | Lines per Tag | Line Size (bytes) |
| ECX | Bits 31–24 | Bits 23–16 | Bits 15–8 | Bits 7–0 |

Note:
* See “Associativity for L1 Caches and L1 TLBs” on page 74 for more information.

Table 22. EDX Format Returned by Function 8000_0005h

| | L1 Instruction Cache | | | |
|-----|----------------------|----------------|---------------|-------------------|
| | Size (Kbytes) | Associativity* | Lines per Tag | Line Size (bytes) |
| EDX | Bits 31–24 | Bits 23–16 | Bits 15–8 | Bits 7–0 |

Note:
* See “Associativity for L1 Caches and L1 TLBs” on page 74 for more information.

5.3.5 Function 8000_0005h—L1 Cache Information for AMD-K5 and All AMD-K6[®] Processors

Input: EAX = 8000_0005h

Output: EAX = Reserved
 EBX = TLB Page Information
 ECX = L1 Data Cache Information
 EDX = L1 Instruction Cache Information

Function 8000_0005h returns information about the processor’s on-chip L1 caches and associated TLBs. Tables 23, 24, and 25 provide the format for the information returned by the 8000_0005h function for the AMD-K5 and all AMD-K6[®] processors.

Table 23. EBX Format Returned by Function 8000_0005h

| | Data TLB | | Instruction TLB | |
|-----|----------------|------------|-----------------|-----------|
| | Associativity* | # Entries | Associativity* | # Entries |
| EBX | Bits 31–24 | Bits 23–16 | Bits 15–8 | Bits 7–0 |

Note:
* See “Associativity for L1 Caches and L1 TLBs” on page 74 for more information.

Table 24. ECX Format Returned by Function 8000_0005h

| | L1 Data Cache | | | |
|-----|---------------|----------------|---------------|-------------------|
| | Size (Kbytes) | Associativity* | Lines per Tag | Line Size (bytes) |
| ECX | Bits 31–24 | Bits 23–16 | Bits 15–8 | Bits 7–0 |

Note:
* See “Associativity for L1 Caches and L1 TLBs” on page 74 for more information.

Table 25. EDX Format Returned by Function 8000_0005h

| | L1 Instruction Cache | | | |
|-----|----------------------|----------------|---------------|-------------------|
| | Size (Kbytes) | Associativity* | Lines per Tag | Line Size (bytes) |
| EDX | Bits 31–24 | Bits 23–16 | Bits 15–8 | Bits 7–0 |

Note:
* See “Associativity for L1 Caches and L1 TLBs” on page 74 for more information.

5.3.6 Extended Function 8000_0006h—L2 Cache and L2 TLB Information for the AMD Athlon™ 64 and AMD Opteron™, AMD Athlon™, and AMD Duron™ Processors

Note: The L2 cache for the AMD Athlon processor model 1 and model 2 must be configured prior to invoking this function.

Function 8000_0006h returns information about the processor L2 TLBs and L2 cache. The format for the information returned by the 8000_0006h function for the AMD Athlon 64 and AMD Opteron processors is the same as the format used by AMD Athlon and the AMD Duron processors, although the field values may differ. Tables 26 through 28 list the values returned by function 8000_0006h for the AMD Athlon 64 and AMD Opteron processors.

Input: EAX = 8000_0006h

Output: EAX = L2 TLB Large Page Information
 EBX = L2 TLB 4-Kbyte Page Information
 ECX = L2 Unified Cache Information
 EDX = Reserved (0)

Table 26. EAX Format Returned by Function 8000_0006h

| | Two-Mbyte/4-Mbyte Pages | | | |
|-----|----------------------------|------------|-------------------------------|-----------|
| | L2 Data TLB ² | | L2 Instruction or Unified TLB | |
| | Associativity ¹ | # Entries | Associativity ¹ | # Entries |
| EAX | Bits 31–28 | Bits 27–16 | Bits 15–12 | Bits 11–0 |

Notes:

1. See “Associativity for L2 Caches and L2 TLBs” on page 74 for more information.
2. A unified L2 TLB is indicated by a value of 0000h in the upper 16 bits of the EBX register. Unified TLB information is then referenced in the lower 16 bits of the EBX register.

Table 27. EBX Format Returned by Function 8000_0006h

| | Four-Kbyte Pages | | | |
|-----|----------------------------|------------|-------------------------------|-----------|
| | L2 Data TLB ² | | L2 Instruction or Unified TLB | |
| | Associativity ¹ | # Entries | Associativity ¹ | # Entries |
| EBX | Bits 31–28 | Bits 27–16 | Bits 15–12 | Bits 11–0 |

Notes:

1. See “Associativity for L2 Caches and L2 TLBs” on page 74 for more information.
2. A unified L2 TLB is indicated by a value of 0000h in the upper 16 bits of the EBX register. Unified TLB information is then referenced in the lower 16 bits of the EBX register.

Table 28. ECX Format Returned by Function 8000_0006h

| | L2 Cache | | | |
|-----|---------------|----------------------------|---------------|-------------------|
| | Size (Kbytes) | Associativity [*] | Lines per Tag | Line Size (bytes) |
| ECX | Bits 31–16 | Bits 15–12 | Bits 11–8 | Bits 7–0 |

Note:

* See “Associativity for L2 Caches and L2 TLBs” on page 74 for more information.

5.3.7 Function 8000_0006h—L2 Cache Information for the AMD-K6[®]-III Processor

Function 8000_0006h returns information about the processor's L2 cache.

Input: EAX = 8000_0006h
 Output: EAX = Reserved (0)
 EBX = Reserved (0)
 ECX = L2 Unified Cache Information
 EDX = Reserved (0)

Table 29 provides the format for the information returned by the 8000_0006h function.

Table 29. ECX Format Returned by Function 8000_0006h for the AMD-K6[®]-III Processor

| L2 Cache | | | | |
|--|---------------|----------------|---------------|-------------------|
| | Size (Kbytes) | Associativity* | Lines per Tag | Line Size (bytes) |
| ECX | Bits 31–16 | Bits 15–12 | Bits 11–8 | Bits 7–0 |
| Note: * See "Associativity for L2 Caches and L2 TLBs" on page 74 for more information. | | | | |

5.3.7.1 Associativity Field Definitions

This section describes the values returned in the associativity fields.

5.3.7.1.1 Associativity for L1 Caches and L1 TLBs

The associativity fields for the L1 data cache, L1 instruction cache, L1 data TLB, and L1 instruction TLB are all eight bits wide. Except for 00h (Reserved) and FFh (Full), the number returned in the associativity field represents the actual number of ways, with a range of 01h through FEh. For example, a returned value of 02h indicates two-way associativity and a returned value of 04h indicates four-way associativity.

5.3.7.1.2 Associativity for L2 Caches and L2 TLBs

The associativity fields for the L2 cache, L2 data TLB, and L2 instruction TLB are four bits wide. Table 30 shows the values returned in these associativity fields.

Table 30. Associativity Values For L2 Caches and TLBs

| Bits 15–12 | Associativity |
|------------|---------------|
| 0000b | L2 off |
| 0001b | Direct mapped |

Table 30. Associativity Values For L2 Caches and TLBs

| Bits 15–12 | Associativity |
|-------------------|----------------------|
| 0010b | 2-way |
| 0011b | <i>Reserved</i> |
| 0100b | 4-way |
| 0101b | <i>Reserved</i> |
| 0110b | 8-way |
| 0111b | <i>Reserved</i> |
| 1000b | 16-way |
| 1001b | <i>Reserved</i> |
| 1010b | <i>Reserved</i> |
| 1011b | <i>Reserved</i> |
| 1100b | <i>Reserved</i> |
| 1101b | <i>Reserved</i> |
| 1110b | <i>Reserved</i> |
| 1111b | Full |

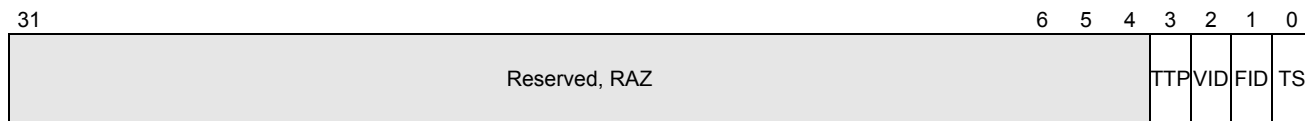
5.3.8 Function 8000_0007h — Advanced Power Management Feature Flags

Function 8000_0007h returns information about the advanced power management features supported by the processor. The function returns the power management feature flags in the EDX register, as shown in Figure 4. Each bit corresponds to a specific feature. A 1 indicates that the feature is present and a 0 indicates that the feature is not present.

EAX, EBX, and ECX are reserved for future advanced power management features.

Input EAX = 8000_0007h

Output EAX = Reserved
 EBX = Reserved
 ECX = Reserved
 EDX = Advanced Power Management feature flags



| Bits | Mnemonic | Definition | Value |
|------|----------|---------------------------|-------|
| 31–4 | Reserved | RAZ | |
| 3 | TTP | Thermal Trip ¹ | 1 |
| 2 | VID | Voltage ID Control | 1 |
| 1 | FID | Frequency ID Control | 1 |
| 0 | TS | Temperature Sensor | 1 |

Note:

1. This function is available only on the AMD Athlon™ 64 and AMD Opteron™ processors.

Figure 4. EDX Bit Fields for Extended Function 8000_0007h

For more details, see the *BIOS Requirements for AMD PowerNow!™ Technology Application Note*, order# 25264, and the *BIOS Requirements for AMD PowerNow!™ Technology Low-Power Desktop Processors Application Note*, order# 25541.

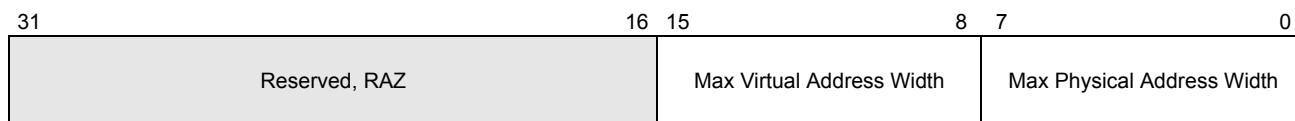
5.3.9 Function 8000_0008h — Physical Address and Linear Address Size

Function 8000_0008h returns information about the maximum physical and linear address width (in bits) supported by the processor, as shown in Figure 5 on page 77. The width reported is the maximum supported in any mode. For long mode capable processors, the size reported is independent of whether long mode is enabled.

Input: EAX = 8000_0008h

Output: EAX = Max Physical and Linear Address Width
 EBX = Reserved
 ECX = Reserved
 EDX = Reserved

The AMD Athlon 64 and AMD Opteron processors return 30h (48 bits) for the maximum linear address (Virtual Address) size and 28h (40 bits) for the maximum physical address size.



| Bits | Definition | Value |
|-------|--------------------------------|---------------|
| 31–16 | Reserved | RAZ |
| 15–8 | Maximum Virtual Address Width | 30h (48 bits) |
| 7–0 | Maximum Physical Address Width | 28h (40 bits) |

Figure 5. EAX Bit Fields for Extended Function 8000_0008h

5.3.10 Extended Functions 8000_0009h–8000_0018h—Vendor-Specific Feature Flags

Functions 8000_0009h through 8000_0018h are reserved for future expansion of vendor-specific feature flags. Each function is reserved for a specific vendor.

Input: EAX = 8000_0009h to 8000_0018h

Output: EAX = 0 (Reserved for vendor-specific features)
 EBX = 0 (Reserved for vendor-specific features)
 ECX = 0 (Reserved for vendor-specific features)
 EDX = 0 (Reserved for vendor-specific features)

Features that are compatible with extensions made by other vendors will be reported in the feature function reserved for that vendor. So, to check for a certain feature across multiple vendors, software need only check the vendor-specific feature flags for the vendor that first implemented that feature.

Currently, Intel features are reported by function 0000_0001h and AMD features are reported by function 8000_0001h. Functions 8000_0009h and 8000_000Ah are reserved for expansion by Intel and AMD respectively.

- 8000_0009h reserved for Intel feature flag expansion
- 8000_000Ah reserved for AMD feature flag expansion
- 8000_000B–8000_0018h reserved for vendors to be determined

Appendix A Register Values Returned by the AMD Family Processors

Tables 31–36 contain all the values returned for AMD processors by the CPUID instruction.

A.1 AMD Athlon™ 64 and AMD Opteron™ Processor Values

Table 31. Values Returned by the AMD Athlon™ 64 and AMD Opteron™ Processors

| Function Register | AMD Athlon™ 64 Processor (Model 4) | AMD Athlon™ 64 FX and AMD Opteron™ Processors (Model 5) |
|--|------------------------------------|---|
| Function: 0 | | |
| EAX | 0000_0001h | 0000_0001h |
| EBX | 6874_7541h | 6874_7541h |
| ECX | 444D_4163h | 444D_4163h |
| EDX | 6974_6E65h | 6974_6E65h |
| Function: 1 | | |
| EAX | 0000_0F4Xh | 0000_0F5Xh |
| EBX | XX00_08XXh ¹ | XX00_08XXh ¹ |
| ECX | Reserved | Reserved |
| EDX | 078B_F9FFh ² | 078B_F9FFh ² |
| Function: 8000_0000h | | |
| EAX | 8000_0018h | 8000_0018h |
| EBX | Reserved | Reserved |
| ECX | Reserved | Reserved |
| EDX | Reserved | Reserved |
| Notes: | | |
| <ol style="list-style-type: none"> Function 1, EBX byte 0 returns an 8-bit Brand ID on some versions of Opteron (see section 5.2.2.2.1.) and byte 3 returns an initial APIC ID which is system-dependent (see section 5.2.2.2.3.). The processor contains an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be 078B_FBFFh. 8000_0001h returns the 12-bit Brand ID in EBX. For more information, see Appendix B "Programming the Name String of the AMD Athlon™ 64 and AMD Opteron™ Processors". 8000_0002/3/4 all return 0 until the name string is programmed by the BIOS. For more information, see Appendix B "Programming the Name String of the AMD Athlon™ 64 and AMD Opteron™ Processors". The processor contains an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value is E1D3_FBFFh. | | |

Table 31. Values Returned by the AMD Athlon™ 64 and AMD Opteron™ Processors

| Function Register | AMD Athlon™ 64 Processor (Model 4) | AMD Athlon™ 64 FX and AMD Opteron™ Processors (Model 5) |
|--------------------------------------|------------------------------------|---|
| Function: 8000_0001h | | |
| EAX | 0000_0F4Xh | 0000_0F5Xh |
| EBX | 0000_0XXXh ³ | 0000_0XXX ³ |
| ECX | Reserved | Reserved |
| EDX | E1D3_F9FFh ⁵ | E1D3_F9FFh ⁵ |
| Function: 8000_0002h ⁴ | | |
| EAX | 0000_0000h | 0000_0000h |
| EBX | 0000_0000h | 0000_0000h |
| ECX | 0000_0000h | 0000_0000h |
| EDX | 0000_0000h | 0000_0000h |
| Function: 8000_0003h ⁴ | | |
| EAX | 0000_0000h | 0000_0000h |
| EBX | 0000_0000h | 0000_0000h |
| ECX | 0000_0000h | 0000_0000h |
| EDX | 0000_0000h | 0000_0000h |
| Function: 8000_0004h ⁴ | | |
| EAX | 0000_0000h | 0000_0000h |
| EBX | 0000_0000h | 0000_0000h |
| ECX | 0000_0000h | 0000_0000h |
| EDX | 0000_0000h | 0000_0000h |

Notes:

1. Function 1, EBX byte 0 returns an 8-bit Brand ID on some versions of Opteron (see section 5.2.2.2.1.) and byte 3 returns an initial APIC ID which is system-dependent (see section 5.2.2.2.3.).
2. The processor contains an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be 078B_FBFFh.
3. 8000_0001h returns the 12-bit Brand ID in EBX. For more information, see Appendix B "Programming the Name String of the AMD Athlon™ 64 and AMD Opteron™ Processors".
4. 8000_0002/3/4 all return 0 until the name string is programmed by the BIOS. For more information, see Appendix B "Programming the Name String of the AMD Athlon™ 64 and AMD Opteron™ Processors".
5. The processor contains an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value is E1D3_FBFFh.

Table 31. Values Returned by the AMD Athlon™ 64 and AMD Opteron™ Processors

| Function Register | AMD Athlon™ 64 Processor (Model 4) | AMD Athlon™ 64 FX and AMD Opteron™ Processors (Model 5) |
|--|------------------------------------|---|
| Function: 8000_0005h | | |
| EAX | 0408_FF08h | 0408_FF08h |
| EBX | FF20_FF10h | FF20_FF10h |
| ECX | 4002_0140h | 4002_0140h |
| EDX | 4002_0140h | 4002_0140h |
| Function: 8000_0006h | | |
| EAX | 0000_0000h | 0000_0000h |
| EBX | 4100_4100h | 4100_4100h |
| ECX | 0400_8140h | 0400_8140h |
| EDX | Reserved | Reserved |
| Function: 8000_0007h | | |
| EAX | Reserved | Reserved |
| EBX | Reserved | Reserved |
| ECX | Reserved | Reserved |
| EDX | ****_***Fh | ****_***Fh |
| Function: 8000_0008h | | |
| EAX | 0000_3028h | 0000_3028h |
| EBX | Reserved | Reserved |
| ECX | Reserved | Reserved |
| EDX | Reserved | Reserved |
| Function: 8000_0009h | | |
| EAX | 0000_0000h | 0000_0000h |
| EBX | 0000_0000h | 0000_0000h |
| ECX | 0000_0000h | 0000_0000h |
| EDX | 0000_0000h | 0000_0000h |
| Notes: | | |
| <ol style="list-style-type: none"> Function 1, EBX byte 0 returns an 8-bit Brand ID on some versions of Opteron (see section 5.2.2.2.1.) and byte 3 returns an initial APIC ID which is system-dependent (see section 5.2.2.2.3.). The processor contains an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be 078B_FBFFh. 8000_0001h returns the 12-bit Brand ID in EBX. For more information, see Appendix B "Programming the Name String of the AMD Athlon™ 64 and AMD Opteron™ Processors". 8000_0002/3/4 all return 0 until the name string is programmed by the BIOS. For more information, see Appendix B "Programming the Name String of the AMD Athlon™ 64 and AMD Opteron™ Processors". The processor contains an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value is E1D3_FBFFh. | | |

Table 31. Values Returned by the AMD Athlon™ 64 and AMD Opteron™ Processors

| Function Register | AMD Athlon™ 64 Processor (Model 4) | AMD Athlon™ 64 FX and AMD Opteron™ Processors (Model 5) |
|--|------------------------------------|---|
| Function: 8000_000Ah | | |
| EAX | 0000_0000h | 0000_0000h |
| EBX | 0000_0000h | 0000_0000h |
| ECX | 0000_0000h | 0000_0000h |
| EDX | 0000_0000h | 0000_0000h |
| Function: 8000_000Bh– 8000_0018h | | |
| EAX | 0000_0000h | 0000_0000h |
| EBX | 0000_0000h | 0000_0000h |
| ECX | 0000_0000h | 0000_0000h |
| EDX | 0000_0000h | 0000_0000h |
| Notes: | | |
| <ol style="list-style-type: none"> Function 1, EBX byte 0 returns an 8-bit Brand ID on some versions of Opteron (see section 5.2.2.2.1.) and byte 3 returns an initial APIC ID which is system-dependent (see section 5.2.2.2.3.). The processor contains an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be 078B_FBFFh. 8000_0001h returns the 12-bit Brand ID in EBX. For more information, see Appendix B “Programming the Name String of the AMD Athlon™ 64 and AMD Opteron™ Processors”. 8000_0002/3/4 all return 0 until the name string is programmed by the BIOS. For more information, see Appendix B “Programming the Name String of the AMD Athlon™ 64 and AMD Opteron™ Processors”. The processor contains an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value is E1D3_FBFFh. | | |

A.2 AMD Athlon™ Processor and AMD Duron™ Processor Values

Table 32. Values Returned by AMD Athlon™ and AMD Duron™ Processors Models 6 and Higher

| Function Register | Processor (Model 6) ¹ | Processor (Model 7) ¹ | Processor (Model 8) ¹ | Processor (Model 10) ¹ |
|-------------------------|-------------------------------------|-------------------------------------|-------------------------------------|--------------------------------------|
| Function: 0 | | | | |
| EAX | 0000_0001h | 0000_0001h | 0000_0001h | 0000_0001h |
| EBX | 6874_7541h | 6874_7541h | 6874_7541h | 6874_7541h |
| ECX | 444D_4163h | 444D_4163h | 444D_4163h | 444D_4163h |
| EDX | 6974_6E65h | 6974_6E65h | 6974_6E65h | 6974_6E65h |
| Function: 1 | | | | |
| EAX | 0000_066Xh | 0000_067Xh | 0000_068Xh | 0000_068Xh |
| EBX | Reserved | Reserved | Reserved | Reserved |
| ECX | Reserved | Reserved | Reserved | Reserved |
| EDX | 0183_F9FFh ² | 0183_F9FFh ² | 0183_F9FFh ² | 0183_F9FFh ² |
| Function: 8000_0000h | | | | |
| EAX | 8000_0008h | 8000_0008h | 8000_0008h | 8000_0008h |
| EBX | Reserved | Reserved | Reserved | Reserved |
| ECX | Reserved | Reserved | Reserved | Reserved |
| EDX | Reserved | Reserved | Reserved | Reserved |
| Function: 8000_0001h | | | | |
| EAX | 0000_076Xh | 0000_077Xh | 0000_078Xh | 0000_078Xh |
| EBX | Reserved | Reserved | Reserved | Reserved |
| ECX | Reserved | Reserved | Reserved | Reserved |
| EDX | C1C3_F9FFh ³ | C1C3_F9FFh ³ | C1C3_F9FFh ³ | C1C3_F9FFh ³ |

Notes:

1. The returned values for the AMD Athlon™ and AMD Duron™ processors models 6 and higher are for all non-mobile processors, including the AMD Athlon XP, AMD Athlon MP, AMD Duron processors.
2. The AMD processors models 6 and higher contain an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be 0183_FBFFh.
3. The AMD processors models 6 and higher contain an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be C1C3_FBFFh. This value also varies based on the setting of the MP bit 19. See Table 15 on page 64 and Table 16 on page 66 for details.
4. The L2 cache size and associativity on AMD processors are product specific. AMD Athlon processor model 10 has an L2 cache size of 512-Kbyte with 16-way set associativity. AMD Athlon processor models 6 and 8 have an L2 cache size of 256-Kbyte with 16-way set associativity. AMD Duron processor models 6 and greater have an L2 cache size of 64-Kbyte with 16-way set associativity.

Table 32. Values Returned by AMD Athlon™ and AMD Duron™ Processors Models 6 and Higher (Continued)

| Function Register | Processor (Model 6) ¹ | Processor (Model 7) ¹ | Processor (Model 8) ¹ | Processor (Model 10) ¹ |
|---|-------------------------------------|-------------------------------------|-------------------------------------|--------------------------------------|
| Function: 8000_0002h | | | | |
| EAX | 2044_4D41h | 2044_4D41h | 2044_4D41h | 2044_4D41h |
| EBX | 6C68_7441h | 6F72_7544h | 6C68_7441h | 6C68_7441h |
| ECX | 7428_6E6Fh | 6D74_286Eh | 7428_6E6Fh | 7428_6E6Fh |
| EDX | 5020_296Dh | 7250_2029h | 5020_296Dh | 5020_296Dh |
| Function: 8000_0003h | | | | |
| EAX | 6563_6F72h | 7365_636Fh | 6563_6F72h | 6563_6F72h |
| EBX | 726F_7373h | 0072_6F73h | 726F_7373h | 726F_7373h |
| ECX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| EDX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| Function: 8000_0004h | | | | |
| EAX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| EBX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| ECX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| EDX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| Function: 8000_0005h | | | | |
| EAX | 0408_FF08h | 0408_FF08h | 0408_FF08h | 0408_FF08h |
| EBX | FF20_FF10h | FF20_FF10h | FF20_FF10h | FF20_FF10h |
| ECX | 4002_0140h | 4002_0140h | 4002_0140h | 4002_0140h |
| EDX | 4002_0140h | 4002_0140h | 4002_0140h | 4002_0140h |
| Notes: | | | | |
| <ol style="list-style-type: none"> 1. The returned values for the AMD Athlon™ and AMD Duron™ processors models 6 and higher are for all non-mobile processors, including the AMD Athlon XP, AMD Athlon MP, AMD Duron processors. 2. The AMD processors models 6 and higher contain an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be 0183_FBFFh. 3. The AMD processors models 6 and higher contain an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be C1C3_FBFFh. This value also varies based on the setting of the MP bit 19. See Table 15 on page 64 and Table 16 on page 66 for details. 4. The L2 cache size and associativity on AMD processors are product specific. AMD Athlon processor model 10 has an L2 cache size of 512-Kbyte with 16-way set associativity. AMD Athlon processor models 6 and 8 have an L2 cache size of 256-Kbyte with 16-way set associativity. AMD Duron processor models 6 and greater have an L2 cache size of 64-Kbyte with 16-way set associativity. | | | | |

Table 32. Values Returned by AMD Athlon™ and AMD Duron™ Processors Models 6 and Higher (Continued)

| Function Register | Processor (Model 6) ¹ | Processor (Model 7) ¹ | Processor (Model 8) ¹ | Processor (Model 10) ¹ |
|-------------------------|-------------------------------------|-------------------------------------|-------------------------------------|--------------------------------------|
| Function: 8000_0006h | | | | |
| EAX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| EBX | 4100_4100h | 4100_4100h | 4100_4100h | 4100_4100h |
| ECX | ****_*140h ⁴ | ****_*140h ⁴ | ****_*140h ⁴ | ****_*140h ⁴ |
| EDX | Reserved | Reserved | Reserved | Reserved |
| Function: 8000_0007h | | | | |
| EAX | Reserved | Reserved | Reserved | Reserved |
| EBX | Reserved | Reserved | Reserved | Reserved |
| ECX | Reserved | Reserved | Reserved | Reserved |
| EDX | ****_*1h | ****_*1h | ****_*1h | ****_*1h |
| Function: 8000_0008h | | | | |
| EAX | 0000_2022h | 0000_2022h | 0000_2022h | 0000_2022h |
| EBX | Reserved | Reserved | Reserved | Reserved |
| ECX | Reserved | Reserved | Reserved | Reserved |
| EDX | Reserved | Reserved | Reserved | Reserved |

Notes:

1. The returned values for the AMD Athlon™ and AMD Duron™ processors models 6 and higher are for all non-mobile processors, including the AMD Athlon XP, AMD Athlon MP, AMD Duron processors.
2. The AMD processors models 6 and higher contain an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be 0183_FBFh.
3. The AMD processors models 6 and higher contain an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be C1C3_FBFh. This value also varies based on the setting of the MP bit 19. See Table 15 on page 64 and Table 16 on page 66 for details.
4. The L2 cache size and associativity on AMD processors are product specific. AMD Athlon processor model 10 has an L2 cache size of 512-Kbyte with 16-way set associativity. AMD Athlon processor models 6 and 8 have an L2 cache size of 256-Kbyte with 16-way set associativity. AMD Duron processor models 6 and greater have an L2 cache size of 64-Kbyte with 16-way set associativity.

Table 33. Values Returned by Mobile AMD Athlon™ Processors Models 6 Higher, and Mobile AMD Duron™ Processors Models 3, 6, and 7

| Function Register | Mobile AMD Duron™ Processor (Model 3) ¹ | Mobile Processor (Model 6) ¹ | Mobile Processor (Model 7) ¹ | Mobile Processor (Model 8) ¹ | Mobile Processor (Model 10) ¹ |
|----------------------|--|---|---|---|--|
| Function: 0 | | | | | |
| EAX | 0000_0001h | 0000_0001h | 0000_0001h | 0000_0001h | 0000_0001h |
| EBX | 6874_7541h | 6874_7541h | 6874_7541h | 6874_7541h | 6874_7541h |
| ECX | 444D_4163h | 444D_4163h | 444D_4163h | 444D_4163h | 444D_4163h |
| EDX | 6974_6E65h | 6974_6E65h | 6974_6E65h | 6974_6E65h | 6974_6E65h |
| Function: 1 | | | | | |
| EAX | 0000_063Xh | 0000_066Xh | 0000_067Xh | 0000_066Xh | 0000_066Xh |
| EBX | Reserved | Reserved | Reserved | Reserved | Reserved |
| ECX | Reserved | Reserved | Reserved | Reserved | Reserved |
| EDX | 0183_F9FFh ² | 0183_F9FFh ² | 0183_F9FFh ² | 0183_F9FFh ² | 0183_F9FFh ² |
| Function: 8000_0000h | | | | | |
| EAX | 8000_0006h | 8000_0008h | 8000_0008h | 8000_0008h | 8000_0008h |
| EBX | Reserved | Reserved | Reserved | Reserved | Reserved |
| ECX | Reserved | Reserved | Reserved | Reserved | Reserved |
| EDX | Reserved | Reserved | Reserved | Reserved | Reserved |
| Function: 8000_0001h | | | | | |
| EAX | 0000_073Xh | 0000_076Xh | 0000_077Xh | 0000_076Xh | 0000_076Xh |
| EBX | Reserved | Reserved | Reserved | Reserved | Reserved |
| ECX | Reserved | Reserved | Reserved | Reserved | Reserved |
| EDX | C1C3_F9FFh ³ | C1C3_F9FFh ³ | C1C3_F9FFh ³ | C1C3_F9FFh ³ | C1C3_F9FFh ³ |

Notes:

1. The returned values for mobile AMD Athlon™ processors models 6 and higher, and AMD Duron™ processors models 3, 6, and 7 are for the mobile AMD Athlon™ 4, mobile AMD Athlon XP, and mobile AMD Duron™ processors.
2. The AMD processors models 6 and higher contain an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be 0183_FBFFh.
3. The AMD processors models 6 and higher contain an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be C1C3_FBFFh. This value also varies based on the setting of the MP bit 19. See Tables 7 and 8 for details.
4. The L2 cache size and associativity on AMD processors are product specific. AMD Athlon processor model 10 has an L2 cache size of 512-Kbyte with 16-way set associativity. AMD Athlon processor models 6 and 8 have an L2 cache size of 256-Kbyte with 16-way set associativity. AMD Duron processor models 6 and greater have an L2 cache size of 64-Kbyte with 16-way set associativity. The Mobile AMD Duron processor model 3 has an L2 cache size of 64-Kbyte with 16-way set associativity.

Table 33. Values Returned by Mobile AMD Athlon™ Processors Models 6 Higher, and Mobile AMD Duron™ Processors Models 3, 6, and 7 (Continued)

| Function Register | Mobile AMD Duron™ Processor (Model 3) ¹ | Mobile Processor (Model 6) ¹ | Mobile Processor (Model 7) ¹ | Mobile Processor (Model 8) ¹ | Mobile Processor (Model 10) ¹ |
|-------------------------|--|---|---|---|--|
| Function: 8000_0002h | | | | | |
| EAX | 2044_4D41h | 2044_4D41h | 2044_4D41h | 2044_4D41h | 2044_4D41h |
| EBX | 6F72_7544h | 6C68_7441h | 6F72_7544h | 6C68_7441h | 6C68_7441h |
| ECX | 6D74_286Eh | 7428_6E6Fh | 6D74_286Eh | 7428_6E6Fh | 7428_6E6Fh |
| EDX | 7250_2029h | 5020_296Dh | 7250_2029h | 5020_296Dh | 5020_296Dh |
| Function: 8000_0003h | | | | | |
| EAX | 7365_636Fh | 6563_6F72h | 7365_636Fh | 6563_6F72h | 6563_6F72h |
| EBX | 0072_6F73h | 726F_7373h | 0072_6F73h | 726F_7373h | 726F_7373h |
| ECX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| EDX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| Function: 8000_0004h | | | | | |
| EAX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| EBX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| ECX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| EDX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| Function: 8000_0005h | | | | | |
| EAX | 0408_FF08h | 0408_FF08h | 0408_FF08h | 0408_FF08h | 0408_FF08h |
| EBX | FF18_FF10h | FF20_FF10h | FF20_FF10h | FF20_FF10h | FF20_FF10h |
| ECX | 4002_0140h | 4002_0140h | 4002_0140h | 4002_0140h | 4002_0140h |
| EDX | 4002_0140h | 4002_0140h | 4002_0140h | 4002_0140h | 4002_0140h |

Notes:

1. The returned values for mobile AMD Athlon™ processors models 6 and higher, and AMD Duron™ processors models 3, 6, and 7 are for the mobile AMD Athlon™ 4, mobile AMD Athlon XP, and mobile AMD Duron™ processors.
2. The AMD processors models 6 and higher contain an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be 0183_FBFh.
3. The AMD processors models 6 and higher contain an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be C1C3_FBFh. This value also varies based on the setting of the MP bit 19. See Tables 7 and 8 for details.
4. The L2 cache size and associativity on AMD processors are product specific. AMD Athlon processor model 10 has an L2 cache size of 512-Kbyte with 16-way set associativity. AMD Athlon processor models 6 and 8 have an L2 cache size of 256-Kbyte with 16-way set associativity. AMD Duron processor models 6 and greater have an L2 cache size of 64-Kbyte with 16-way set associativity. The Mobile AMD Duron processor model 3 has an L2 cache size of 64-Kbyte with 16-way set associativity.

Table 33. Values Returned by Mobile AMD Athlon™ Processors Models 6 Higher, and Mobile AMD Duron™ Processors Models 3, 6, and 7 (Continued)

| Function Register | Mobile AMD Duron™ Processor (Model 3) ¹ | Mobile Processor (Model 6) ¹ | Mobile Processor (Model 7) ¹ | Mobile Processor (Model 8) ¹ | Mobile Processor (Model 10) ¹ |
|-------------------------|---|--|--|--|---|
| Function: 8000_0006h | | | | | |
| EAX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| EBX | 4100_4100h | 4100_4100h | 4100_4100h | 4100_4100h | 4100_4100h |
| ECX | ****_*140h ⁴ | ****_*140h ⁴ | ****_*140h ⁴ | ****_*140h ⁴ | ****_*140h ⁴ |
| EDX | Reserved | Reserved | Reserved | Reserved | Reserved |
| Function: 8000_0007h | | | | | |
| EAX | Not Supported | Reserved | Reserved | Reserved | Reserved |
| EBX | | Reserved | Reserved | Reserved | Reserved |
| ECX | | Reserved | Reserved | Reserved | Reserved |
| EDX | | ****_*7h | ****_*7h | ****_*7h | ****_*7h |
| Function: 8000_0008h | | | | | |
| EAX | Not Supported | 0000_2022h | 0000_2022h | 0000_2022h | 0000_2022h |
| EBX | | Reserved | Reserved | Reserved | Reserved |
| ECX | | Reserved | Reserved | Reserved | Reserved |
| EDX | | Reserved | Reserved | Reserved | Reserved |

Notes:

1. The returned values for mobile AMD Athlon™ processors models 6 and higher, and AMD Duron™ processors models 3, 6, and 7 are for the mobile AMD Athlon™ 4, mobile AMD Athlon XP, and mobile AMD Duron™ processors.
2. The AMD processors models 6 and higher contain an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be 0183_FBFFh.
3. The AMD processors models 6 and higher contain an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be C1C3_FBFFh. This value also varies based on the setting of the MP bit 19. See Tables 7 and 8 for details.
4. The L2 cache size and associativity on AMD processors are product specific. AMD Athlon processor model 10 has an L2 cache size of 512-Kbyte with 16-way set associativity. AMD Athlon processor models 6 and 8 have an L2 cache size of 256-Kbyte with 16-way set associativity. AMD Duron processor models 6 and greater have an L2 cache size of 64-Kbyte with 16-way set associativity. The Mobile AMD Duron processor model 3 has an L2 cache size of 64-Kbyte with 16-way set associativity.

Table 34. Values Returned by AMD Athlon™ Processors Models 1, 2, and 4, and AMD Duron™ Processors Model 3

| Function Register | AMD Athlon™ Processor (Model 1) | AMD Athlon Processor (Model 2) | AMD Athlon Processor (Model 4) | AMD Duron™ Processor (Model 3) |
|----------------------|---------------------------------|--------------------------------|--------------------------------|--------------------------------|
| Function: 0 | | | | |
| EAX | 0000_0001h | 0000_0001h | 0000_0001h | 0000_0001h |
| EBX | 6874_7541h | 6874_7541h | 6874_7541h | 6874_7541h |
| ECX | 444D_4163h | 444D_4163h | 444D_4163h | 444D_4163h |
| EDX | 6974_6E65h | 6974_6E65h | 6974_6E65h | 6974_6E65h |
| Function: 1 | | | | |
| EAX | 0000_061Xh | 0000_062Xh | 0000_064Xh | 0000_063Xh |
| EBX | Reserved | Reserved | Reserved | Reserved |
| ECX | Reserved | Reserved | Reserved | Reserved |
| EDX | 0081_F9FFh | 0183_F9FFh ¹ | 0183_F9FFh ¹ | 0183_F9FFh ¹ |
| Function: 8000_0000h | | | | |
| EAX | 8000_0006h | 8000_0006h | 8000_0006h | 8000_0006h |
| EBX | Reserved | Reserved | Reserved | Reserved |
| ECX | Reserved | Reserved | Reserved | Reserved |
| EDX | Reserved | Reserved | Reserved | Reserved |
| Function: 8000_0001h | | | | |
| EAX | 0000_071Xh | 0000_072Xh | 0000_074Xh | 0000_073Xh |
| EBX | Reserved | Reserved | Reserved | Reserved |
| ECX | Reserved | Reserved | Reserved | Reserved |
| EDX | C0C1_F9FFh | C1C3_F9FFh ² | C1C3_F9FFh ² | C1C3_F9FFh ² |
| Function: 8000_0002h | | | | |
| EAX | 2D44_4D41h | 2044_4D41h | 2044_4D41h | 2044_4D41h |
| EBX | 7428_374Bh | 6C68_7441h | 6C68_7441h | 6F72_7544h |
| ECX | 5020_296Dh | 7428_6E6Fh | 7428_6E6Fh | 6D74_286Eh |
| EDX | 6563_6F72h | 5020_296Dh | 5020_296Dh | 7250_2029h |

Notes:

1. The AMD Duron™ processor and AMD Athlon™ processor models 2 and 4 contain an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be 0183_FBFFh.
2. The AMD Duron processor and AMD Athlon processor models 2 and 4 contain an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be C1C3_FBFFh.
3. The L2 cache size and associativity on AMD processors are product specific. The AMD Athlon processor models 1 and 2 have an L2 cache size of 512-Kbyte with two-way set associativity. The AMD Athlon processor model 4 has an L2 cache size of 256-Kbyte with 16-way set associativity. The AMD Duron processor has an L2 cache size of 64-Kbyte with 16-way set associativity.

Table 34. Values Returned by AMD Athlon™ Processors Models 1, 2, and 4, and AMD Duron™ Processors Model 3 (Continued)

| Function Register | AMD Athlon™ Processor (Model 1) | AMD Athlon Processor (Model 2) | AMD Athlon Processor (Model 4) | AMD Duron™ Processor (Model 3) |
|-------------------------|---------------------------------|--------------------------------|--------------------------------|--------------------------------|
| Function: 8000_0003h | | | | |
| EAX | 726F_7373h | 6563_6F72h | 6563_6F72h | 7365_636Fh |
| EBX | 0000_0000h | 726F_7373h | 726F_7373h | 0072_6F73h |
| ECX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| EDX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| Function: 8000_0004h | | | | |
| EAX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| EBX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| ECX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| EDX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| Function: 8000_0005h | | | | |
| EAX | 0408_FF08h | 0408_FF08h | 0408_FF08h | 0408_FF08h |
| EBX | FF18_FF10h | FF18_FF10h | FF18_FF10h | FF18_FF10h |
| ECX | 4002_0140h | 4002_0140h | 4002_0140h | 4002_0140h |
| EDX | 4002_0140h | 4002_0140h | 4002_0140h | 4002_0140h |
| Function: 8000_0006h | | | | |
| EAX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| EBX | 4100_4100h | 4100_4100h | 4100_4100h | 4100_4100h |
| ECX | ****_*140h ³ | ****_*140h ³ | ****_*140h ³ | ****_*140h ³ |
| EDX | Reserved | Reserved | Reserved | Reserved |

Notes:

1. The AMD Duron™ processor and AMD Athlon™ processor models 2 and 4 contain an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be 0183_FBFFh.
2. The AMD Duron processor and AMD Athlon processor models 2 and 4 contain an APIC, but it is not reflected in this value. If the BIOS enables the APIC, the value would be C1C3_FBFFh.
3. The L2 cache size and associativity on AMD processors are product specific. The AMD Athlon processor models 1 and 2 have an L2 cache size of 512-Kbyte with two-way set associativity. The AMD Athlon processor model 4 has an L2 cache size of 256-Kbyte with 16-way set associativity. The AMD Duron processor has an L2 cache size of 64-Kbyte with 16-way set associativity.

A.3 AMD-K6[®] Processor Values

Table 35. Values Returned by AMD-K6[®] Processors

| Function Register | AMD-K6 [®] Processor (Model 6) | AMD-K6 Processor (Model 7) | AMD-K6 [®] -2 Processor (Model 8) | AMD-K6 [®] -III Processor (Model 9) |
|-------------------------|---|----------------------------------|--|--|
| Function: 0 | | | | |
| EAX | 0000_0001h | 0000_0001h | 0000_0001h | 0000_0001h |
| EBX | 6874_7541h | 6874_7541h | 6874_7541h | 6874_7541h |
| ECX | 444D_4163h | 444D_4163h | 444D_4163h | 444D_4163h |
| EDX | 6974_6E65h | 6974_6E65h | 6974_6E65h | 6974_6E65h |
| Function: 1 | | | | |
| EAX | 0000_056Xh | 0000_057Xh | 0000_058Xh | 0000_059Xh |
| EBX | Reserved | Reserved | Reserved | Reserved |
| ECX | Reserved | Reserved | Reserved | Reserved |
| EDX | 0080_01BFh | 0080_01BFh | 0080_21BFh ¹ | 0080_21BFh |
| Function: 8000_0000h | | | | |
| EAX | 8000_0005h | 8000_0005h | 8000_0005h | 8000_0006h |
| EBX | Reserved | Reserved | Reserved | Reserved |
| ECX | Reserved | Reserved | Reserved | Reserved |
| EDX | Reserved | Reserved | Reserved | Reserved |
| Function: 8000_0001h | | | | |
| EAX | 0000_066Xh | 0000_067Xh | 0000_068Xh | 0000_069Xh |
| EBX | Reserved | Reserved | Reserved | Reserved |
| ECX | Reserved | Reserved | Reserved | Reserved |
| EDX | 0080_05BFh | 0080_05BFh | 8080_29BFh ² | 8080_29BFh |

Notes:

1. AMD-K6[®]-2 processor model 8/[F:8], EDX = 0080_21BFh – Global Paging Extension supported.
AMD-K6-2 processor model 8/[7:0], EDX = 0080_01BFh.
2. AMD-K6-2 processor model 8/[F:8], EDX = 8080_29BFh – Global Paging Extension supported.
AMD-K6-2 processor model 8/[7:0], EDX = 8080_09BFh.
3. Extended functions 8000_0002h, 8000_0003h, and 8000_0004h each return part of the processor name string. Some AMD-K6-2 processors may have the following name string: function 8000_0002h, ECX = 322D_296Dh and EDX = 6F72_5020h, and function 8000_0003h, EAX = 7373_6563h and EBX = 0000_726Fh.
4. Extended functions 8000_0002h, 8000_0003h, and 8000_0004h each return part of the processor name string. Some AMD-K6-III processors may have the following name string: function 8000_0002h, ECX = 492D_296Dh and EDX = 5020_4949h, and function 8000_0003h, EAX = 6563_6F72h and EBX = 726F_7373h.

Table 35. Values Returned by AMD-K6® Processors (Continued)

| Function Register | AMD-K6® Processor (Model 6) | AMD-K6 Processor (Model 7) | AMD-K6®-2 Processor (Model 8) | AMD-K6®-III Processor (Model 9) |
|-------------------------|-----------------------------------|----------------------------------|-------------------------------------|---------------------------------------|
| Function: 8000_0002h | | | | |
| EAX | 2D44_4D41h | 2D44_4D41h | 2D44_4D41h | 2D44_4D41h |
| EBX | 6D74_364Bh | 6D74_364Bh | 7428_364Bh | 7428_364Bh |
| ECX | 202F_7720h | 202F_7720h | 3320_296Dh ³ | 3320_296Dh ⁴ |
| EDX | 746C_756Dh | 746C_756Dh | 7270_2044h ³ | 5020_2B44h ⁴ |
| Function: 8000_0003h | | | | |
| EAX | 6465_6D69h | 6465_6D69h | 7365_636Fh ³ | 6563_6F72h ⁴ |
| EBX | 6520_6169h | 6520_6169h | 0072_6F73h ³ | 726F_7373h ⁴ |
| ECX | 6E65_7478h | 6E65_7478h | 0000_0000h | 0000_0000h |
| EDX | 6E6F_6973h | 6E6F_6973h | 0000_0000h | 0000_0000h |
| Function: 8000_0004h | | | | |
| EAX | 0000_0073h | 0000_0073h | 0000_0000h | 0000_0000h |
| EBX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| ECX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| EDX | 0000_0000h | 0000_0000h | 0000_0000h | 0000_0000h |
| Function: 8000_0005h | | | | |
| EAX | Reserved | Reserved | Reserved | Reserved |
| EBX | 0280_0140h | 0280_0140h | 0280_0140h | 0280_0140h |
| ECX | 2002_0220h | 2002_0220h | 2002_0220h | 2002_0220h |
| EDX | 2002_0220h | 2002_0220h | 2002_0220h | 2002_0220h |
| Function: 8000_0006h | | | | |
| EAX | Undefined | Undefined | Undefined | Reserved |
| EBX | Undefined | Undefined | Undefined | Reserved |
| ECX | Undefined | Undefined | Undefined | 0100_4220h |
| EDX | Undefined | Undefined | Undefined | Reserved |

Notes:

1. AMD-K6®-2 processor model 8/[F:8], EDX = 0080_21BFh – Global Paging Extension supported.
AMD-K6-2 processor model 8/[7:0], EDX = 0080_01BFh.
2. AMD-K6-2 processor model 8/[F:8], EDX = 8080_29BFh – Global Paging Extension supported.
AMD-K6-2 processor model 8/[7:0], EDX = 8080_09BFh.
3. Extended functions 8000_0002h, 8000_0003h, and 8000_0004h each return part of the processor name string. Some AMD-K6-2 processors may have the following name string: function 8000_0002h, ECX = 322D_296Dh and EDX = 6F72_5020h, and function 8000_0003h, EAX = 7373_6563h and EBX = 0000_726Fh.
4. Extended functions 8000_0002h, 8000_0003h, and 8000_0004h each return part of the processor name string. Some AMD-K6-III processors may have the following name string: function 8000_0002h, ECX = 492D_296Dh and EDX = 5020_4949h, and function 8000_0003h, EAX = 6563_6F72h and EBX = 726F_7373h.

A.4 Am486[®], Am5_x86, and AMD-K5 Processor Values

Table 36. Values Returned by Am486[®], Am5_x86, and AMD-K5 Processors

| Function Register | Am486 [®] and Am5 _x 86 Processors | AMD-K5 Processor (Model 0) | AMD-K5 Processor (Model 1) | AMD-K5 Processor (Model 2) | AMD-K5 Processor (Model 3) |
|----------------------|---|----------------------------|----------------------------|----------------------------|----------------------------|
| Function: 0 | | | | | |
| EAX | 0000_0001h | 0000_0001h | 0000_0001h | 0000_0001h | 0000_0001h |
| EBX | 6874_7541h | 6874_7541h | 6874_7541h | 6874_7541h | 6874_7541h |
| ECX | 444D_4163h | 444D_4163h | 444D_4163h | 444D_4163h | 444D_4163h |
| EDX | 6974_6E65h | 6974_6E65h | 6974_6E65h | 6974_6E65h | 6974_6E65h |
| Function: 1 | | | | | |
| EAX | 0000_04XXh | 0000_050Xh | 0000_051Xh | 0000_052Xh | 0000_053Xh |
| EBX | Reserved | Reserved | Reserved | Reserved | Reserved |
| ECX | Reserved | Reserved | Reserved | Reserved | Reserved |
| EDX | 0000_0001h | 0000_03BFh* | 0000_21BFh | 0000_21BFh | 0000_21BFh |
| Function: 8000_0000h | | | | | |
| EAX | 0000_0000h | 0000_0000h | 8000_0005h | 8000_0005h | 8000_0005h |
| EBX | Undefined | Undefined | Reserved | Reserved | Reserved |
| ECX | Undefined | Undefined | Reserved | Reserved | Reserved |
| EDX | Undefined | Undefined | Reserved | Reserved | Reserved |
| Function: 8000_0001h | | | | | |
| EAX | Undefined | Undefined | 0000_051Xh | 0000_052Xh | 0000_053Xh |
| EBX | Undefined | Undefined | Reserved | Reserved | Reserved |
| ECX | Undefined | Undefined | Reserved | Reserved | Reserved |
| EDX | Undefined | Undefined | 0000_21BFh | 0000_21BFh | 0000_21BFh |
| Function: 8000_0002h | | | | | |
| EAX | Undefined | Undefined | 2D44_4D41h | 2D44_4D41h | 2D44_4D41h |
| EBX | Undefined | Undefined | 7428_354Bh | 7428_354Bh | 7428_354Bh |
| ECX | Undefined | Undefined | 5020_296Dh | 5020_296Dh | 5020_296Dh |
| EDX | Undefined | Undefined | 6563_6F72h | 6563_6F72h | 6563_6F72h |

Note:

* The AMD-K5 processor model 0 reserves bit 13 and implements feature bit 9 to indicate support for Global Paging Extensions instead of support for APIC.

Table 36. Values Returned by Am486[®], Am5_x86, and AMD-K5 Processors

| Function Register | Am486 [®] and Am5 _x 86 Processors | AMD-K5 Processor (Model 0) | AMD-K5 Processor (Model 1) | AMD-K5 Processor (Model 2) | AMD-K5 Processor (Model 3) |
|----------------------|---|----------------------------|----------------------------|----------------------------|----------------------------|
| Function: 8000_0003h | | | | | |
| EAX | Undefined | Undefined | 726F_7373h | 726F_7373h | 726F_7373h |
| EBX | Undefined | Undefined | 0000_0000h | 0000_0000h | 0000_0000h |
| ECX | Undefined | Undefined | 0000_0000h | 0000_0000h | 0000_0000h |
| EDX | Undefined | Undefined | 0000_0000h | 0000_0000h | 0000_0000h |
| Function: 8000_0004h | | | | | |
| EAX | Undefined | Undefined | 0000_0000h | 0000_0000h | 0000_0000h |
| EBX | Undefined | Undefined | 0000_0000h | 0000_0000h | 0000_0000h |
| ECX | Undefined | Undefined | 0000_0000h | 0000_0000h | 0000_0000h |
| EDX | Undefined | Undefined | 0000_0000h | 0000_0000h | 0000_0000h |
| Function: 8000_0005h | | | | | |
| EAX | Undefined | Undefined | Reserved | Reserved | Reserved |
| EBX | Undefined | Undefined | 0480_0000h | 0480_0000h | 0480_0000h |
| ECX | Undefined | Undefined | 0804_0120h | 0804_0120h | 0804_0120h |
| EDX | Undefined | Undefined | 1004_0120h | 1004_0120h | 1004_0120h |
| Note: | * The AMD-K5 processor model 0 reserves bit 13 and implements feature bit 9 to indicate support for Global Paging Extensions instead of support for APIC. | | | | |

Appendix B Programming the Name String of the AMD Athlon™ 64 and AMD Opteron™ Processors

This section, for BIOS programmers, describes how to program the *processor name string* that is returned by the CPUID instruction.

The AMD Athlon™ 64 and AMD Opteron™ processors support a set of MSRs for programming the processor name string, which can be read with the CPUID functions 8000_0002h, 8000_0003h, and 8000_0004h. The default value of the name string is 48 ASCII NUL characters. See “Extended Functions 8000_0002h, 8000_0003h, and 8000_0004h—Processor Name String” on page 69 for details concerning the name string functions.

The AMD Athlon 64 and AMD Opteron processors require that the BIOS code properly program the processor name string according to the values shown in Table 37 on page 96.

Note: *Motherboards that do not program the proper processor name string and model number will not pass AMD validation and will not be posted on the AMD Recommended Motherboard Website.*

It is common practice for the BIOS to display the processor name string and model number whenever it displays processor information during boot up.

B.1 Brand ID

The BIOS code uses the brand ID value to construct the proper name string from tables of ASCII name string information. The brand ID is either an 8-bit field returned in by CPUID function 1 (see “8-Bit Brand ID” on page 54) or a 12-bit field returned by CPUID function 8000_0001h (see “EBX—12-bit Brand ID” on page 61). The brand ID field is new to the AMD Athlon 64 and AMD Opteron processors and will be implemented in future AMD processor families as well.

The brand ID uniquely identifies a collection of processor features as a particular brand of the AMD Athlon 64 and AMD Opteron processors. Further, each brand has an associated processor name string that is required by the AMD branding strategy.

The BIOS reads the 8-bit brand ID using CPUID function 1 and the 12-bit brand ID using CPUID function 8000_0001h, and uses whichever is nonzero to index into a name string table and a model number table. The BIOS then constructs the name string from the entries in these tables and uses the resulting string to program the processor name string using a set of Model Specific Registers (MSRs) described below.

If the 8-bit brand ID and the 12-bit brand ID are both zero, the processor is an engineering sample. All AMD Athlon 64 and AMD Opteron processors support the brand ID.

B.2 Constructing the Name String

The BIOS must construct the processor name string from information in a table that is a BIOS data structure. The bulk of the name string comes from the name string table, which contains the required processor name string for each AMD Athlon 64 and AMD Opteron processor with placeholders for the specific model number.

If the processor has a nonzero 8-bit brand ID, the three most-significant bits are used to index into the name strings listed in Table 13, and the five least-significant bits are used to calculate two digits of the model number to be inserted into the appropriate name string.

Otherwise, if the processor has a 12-bit brand ID that is nonzero, the four most-significant bits are used to index into the name strings listed in Table 13, and the eight least-significant bits are used to calculate two digits of the model number to be inserted into the appropriate name string.

The processor name string should be NUL terminated and no longer than 48 bytes including the NUL.

Table 37. Processor Name String Values for AMD Athlon™ 64 and AMD Opteron™ Processors

| Brand ID MSBs | Name String | Processor |
|---------------|---|--------------------|
| 00h | AMD Engineering Sample NN ¹ | Reserved |
| 01h | AMD Athlon(tm) 64 Processor XX00+ ² | Desktop/DTR Client |
| 02h | Mobile AMD Athlon(tm) 64 Processor XX00+ ² | Mobile Client |
| 03h | AMD Opteron(tm) Processor 1YY ³ | UP Server |
| 04h | AMD Opteron(tm) Processor 2YY ³ | 2P Server |
| 05h | AMD Opteron(tm) Processor 8YY ³ | MP Server |
| 06h–08h | Reserved | Reserved |
| 09h | AMD Athlon(tm) 64 FX-ZZ Processor ⁴ | Desktop Client |
| 0A–0Fh | Reserved | Reserved |

Notes: For more information, see “8-Bit Brand ID” on page 54 and “EBX—12-bit Brand ID” on page 61.

1. NN = two digit decimal equivalent of bits 4–0.
2. XX = 22 + NN. For example, 00001b stands for “23”, 11111b stands for “53”, and 01001101b stands for “99”.
3. YY = 38 + 2 * NN. For example, 00001b stands for “40” and 11110b stands for “98”. Encoding 11111b is reserved.
4. ZZ = 24 + NN. For example, 00011011b stands for “51” and 00100011b stands for “59”.

BIOS software must be prepared to handle these cases:

- The brand ID value returned indexes to a reserved entry. This case can occur if the user has upgraded his or her processor, but not the BIOS. For this case, it is recommended that the BIOS program the name string as "AMD Athlon(tm) or Opteron(tm) CPU-model unknown".
- The 8-bit brand ID and the 12-bit brand ID are both zero, indicating that the processor is an engineering sample.

B.3 Programming the Processor Name String

After the BIOS has found the proper string in the name table and inserted the correct model number, the BIOS programs the processor name string by writing to six MSRs.

These MSRs (C001_0030h through C001_0035h) are used to set the 48 character processor name string returned by CPUID functions 8000_0002h, 8000_0003h, and 8000_0004h. Each MSR sets eight of the 48 characters in little-endian byte order. The first character resides in the least significant byte of MSR C001_0030h and the last character (always a NUL) resides in the most significant byte of MSR C001_0035h.

