AMD64 Flexible Return and Event Delivery (FRED) Virtualization

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Future AMD APM releases that describe this feature supersede the information in this document

Revision History

Date	Revision	Change Description
January 2026	1.00	Initial release

Flexible Return and Event Delivery (FRED) Virtualization

Introduction

This document describes AMD Flexible Return and Event Delivery (FRED) virtualization.

Presence

CPUID Fn0000_0007_x1 EAX[FRED], bit 17 indicates support for Flexible Return and Event Delivery (FRED).

FRED MSR Virtualization

The following 8-byte fields are added to host and guest state save areas for FRED MSRs:

Offset	Register Name	MSR Address	Swap Type
8B8h	FRED_RSP0	1CCh	A
8C0h	FRED_RSP1	1CDh	A
8C8h	FRED_RSP2	1CEh	A
8D0h	FRED_RSP3	1CFh	A
8D8h	FRED_STKLVLS	1D0h	A
8E0h	FRED_SSP1	1D1h	A
8E8h	FRED_SSP2	1D2h	A
8F0h	FRED_SSP3	1D3h	A
8F8h	FRED_CONFIG	1D4h	A

For SEV-ES and SEV-SNP guests, FRED MSRs are saved to the host state save area and loaded from the VMSA on VMRUN, and stored to the VMSA and loaded from the host state save area on VMEXIT.

For all other guests, FRED virtualization is enabled when bit 4 at offset B8h in the VMCB is set to 1. When FRED virtualization is enabled, all FRED MSRs except FRED_RSP0 are saved to the host state save area and loaded from the VMCB on VMRUN, and stored to the VMCB and loaded from the host state save area on VMEXIT.

FRED_SSP0 (same as PL0_SSP, MSR address 6A4h) is unconditionally saved and restored on all VMRUN and VMEXIT context switches.

The following checks are performed when FRED registers are loaded on VMRUN or VMEXIT:

- FRED_CFG: bit 2, bits 5:4, and bit 11 must be zero
- FRED_RSPn: bits 5:0 must be zero (n = 1 to 3 or n= 0 to 3)

- FRED_SSPn: bits 2:0 must be zero (n = 1 to 3)

If any of the above consistency checks fail during the VMRUN instruction, a #VMEXIT(INVALID) is generated. If any of the above consistency checks fail during VMEXIT, the processor enters the shutdown state.

The upper bits of FRED_CFG, FRED_RSPn, and FRED_SSPn addresses are made canonical by sign-extension from the most-significant implemented linear address bit on VMRUN and VMEXIT context switches.

FRED Exception Intercepts and Event Injection

SVM architecture is extended to provide additional information when an exception is intercepted, or an event is injected into a guest with FRED enabled.

EXITINTINFO field is extended and EXITINTDATA field is added to provide additional information about intercepted FRED exceptions that happen during FRED event delivery.

EXITINTINFO has the following format when FRED is enabled:

Bits	Name	Description
63:32	ERRORCODE	Error Code
31	V	EXITINTINFO Valid
13	NESTEDEXCP	Nested Exception
11	EV	Error Code Valid
10:8	TYPE	Event Type 0: INTR or VINTR 2: NMI or VNMI 3: Exception, INT3, INTO 4: Software Interrupt (INTn instruction) 7: SYSCALL
7:0	VECTOR	Interrupt or exception vector

Nested Exception (bit 13) is set if the event reported in EXITINTINFO is a nested exception and the event is exception other than #DF.

SYSCALL event type is reported with vector value equal to 1.

EXITINTDATA (VMCB offset 170h) field has FRED Event Data information. If Alternate Injection or Secure AVIC is active in an SEV-SNP guest, FRED Event Data is stored in GUEST_EXITINTDATA (VMSA offset 8A8h).

EVENTINJ field is extended and EVENTINJDATA (Event Injection Data) field is added to provide additional information required for FRED event injection. EVENTINJ field had the same format as EXITINTINFO field when FRED is enabled in the guest.

EXITINJDATA (VMCB offset 178h) field has FRED Event Injection Data information. If Alternate Injection or Secure AVIC is active in an SEV-SNP guest, FRED Event Injection Data is stored in GUEST_EVENTINJDATA (VMSA offset 8B0h).

On an intercepted #DB, EXITINFO2 has DR6 register value.

FRED VMRUN Mode and Event Injection Checks

If guest CR4.FRED is 1 in the guest state save area, the following checks are performed during the VMRUN instruction:

- CPL must be 0 or 3.
- If CPL is 0, CS.L must be 1.
- If CPL is 3, IOPL must be 0.
- SS.DPL must be 0 or 3.
- If SS.DPL is 0, CS.L must be 1.
- If SS.DPL is 3, IOPL and the interrupt shadow flag must be 0.

If the event injection field is valid, the following checks are performed:

- If injected Type is 7, Vector must be 1.
- If Error Code is valid or it is a nested exception, injected Type must be 3.

If any of the above FRED related mode and event injection consistency checks fail during the VMRUN instruction, a #VMEXIT(INVALID) is generated.

If FRED virtualization is enabled, NMI virtualization must be enabled in order to properly handle guest NMIs.

Guest Controlled FRED MSR Intercepts

Guest controlled FRED MSR intercepts are defined in VMSA INTERCEPT_MSR_VEC2 field (offset 930h) as follows:

RDMSR Intercept Bit	WRMSR Intercept Bit	MSR Name	MSR Address
12	13	FRED_RSP0	1CCh
14	15	FRED_RSP1	1CDh
16	17	FRED_RSP2	1CEh
18	19	FRED_RSP3	1CFh
20	21	FRED_STKLVLS	1D0h
22	23	FRED_SSP1	1D1h
24	25	FRED_SSP2	1D2h
26	27	FRED_SSP3	1D3h
28	29	FRED_CONFIG	1D4h

For more information, see "*AMD64 Architecture Programmer's Manual*", Volume 2 (Revision 3.43 or later), Section 15.36.23 "Guest Intercept Control".