AMD64 Collaborative Processor Performance Control (CPPC) Performance Priority

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Future AMD APM releases that describe this feature supersede the information in this document

Revision History

Date	Revision	Change Description
March 2026	1.00	Initial release

CPPC Performance Priority

Introduction

This document describes Collaborative Processor Performance Control (CPPC) Performance Priority which is a CPPC extension available on some Zen6 products. Collaborative Processor Performance Control is described in *"AMD64 Architecture Programmer's Manual"*, Volume 2, Section 17.6 *"Collaborative Processor Performance Control"*. With CPPC Performance Priority software can specify different performance floor frequencies on different cores which the platform firmware considers when throttling CPU frequency due to power or thermal constraints.

Support for CPPC Performance Priority is indicated by CPUID Fn8000_0007_EDX[CppcPerfPriority] (bit 27)=1.

CPPC_CAPABILITY_1 Register (MSRC001_02B0)

The following bits are added to CPPC_CAPABILITY_1:

Bits	Mnemonic	Description	Access Type
39:32	FloorPerfCnt	Floor Performance Count	RO

The new fields of CPPC_CAPABILITY_1 are further described below.

- *FloorPerfCnt (Floor Performance Count)* – Bits 39:32. This field reports the number of distinct Floor Perf values supported by the platform. For example, if this value is 2, then the number of unique values of CPPC_REQUEST_2[FloorPerf] across the system should be at most 2 for the throttling behavior described for CPPC_REQUEST_2[FloorPerf] to take effect. A zero value implies that the platform supports unlimited Floor Perf levels. When the Floor Performance Count is non-zero, then the throttling behavior is undefined if the number of unique values of Floor Perf on the system exceeds Floor Perf Count.

CPPC_REQUEST_2 Register (MSRC001_02B5)

Bits	Mnemonic	Description	Access Type
63:8	Reserved		MBZ
7:0	FloorPerf	Floor Performance	RW

The fields of CPPC_REQUEST_2 are further described below:

- *FloorPerf (Floor Performance)* – Bits 7:0. This field contains the floor performance level associated with that core. Software can write any value between CPPC_CAPABILITY_1[LowestPerf] and CPPC_CAPABILITY_1[HighestPerf] to this field. When the system is under power/thermal constraints, the platform firmware will attempt to throttle the CPU frequency to the value corresponding to Floor Performance before throttling further. This allows software to specify different floor frequencies for different cores.