AMD64 UPPER ADDRESS IGNORE VERSION 2

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Future AMD APM releases that describe this feature supersede the information in this document

Revision History

Date	Revision	Change Description
March 2026	1.00	Initial release

Upper Address Ignore Version 2

The Upper Address Ignore Version 2 feature allows software to use bits 62:57 of a data pointer as an arbitrary software-assigned and software-interpreted tag. This feature can be enabled independently for pointers with bit 63 set (which are considered supervisor pointers) and pointers with bit 63 cleared (which are considered user pointers). When enabled, the address bits are excluded from the canonical check if the pointer is used for data access.

Support for Upper Address Ignore Version 2 is indicated by CPUID Fn8000_00021_EAX[UpperAddressIgnoreV2] (bit 26) = 1.

Upper Address Ignore Version 2 introduces 2 types of ignoring bits 62:57 of a 64-bit data pointer address for the canonical check:

- **6-bit User Address Ignore**: ignores bits 62:57 of an effective address that has bit 63 cleared and sets them to zero. This is enabled by setting both CR3[UAI_U6] (bit 61) and EFER[UAI_U_EN] (bit 23).
- **6-bit Supervisor Address Ignore**: ignores bits 62:57 of an effective address that has bit 63 set and sets them to one. This is enabled by setting EFER[UAI_S6] (bit 22)

The Upper Address Ignore Version 2 address-bit ignoring is performed after calculating the data pointer effective address and before the canonical check, the possible addition of a FS/GS segment base address and virtual address translation. In contrast to Upper Address Ignore (Version 1), see *"AMD64 Architecture Programmer's Manual"*, Volume 2, Section 5.10 *"Upper Address Ignore"*, Upper Address Ignore Version 2 does not consider the segment used for data access.

Upper Address Ignore Version 2 is only available in 64-bit mode.

With 6-bit User Address Ignore or 6-bit Supervisor Address Ignore active, the following canonical checks remain:

- 4-level paging: bit 47 of the pointer must match bits 63 and 56:48
- 5-level paging: bit 56 of the pointer must match bit 63

Debug Breakpoint Behavior

Upper Address Ignore Version 2 changes how an address match is performed for data address breakpoints. With 6-bit User Address Ignore or 6-bit Supervisor Address Ignore active the value in DR0-3 bits 62:57 is ignored, and the linear address of the memory access is only compared against DR0-3 bits 63 and 56:0.

Address Tag Storage

The linear address stored in the CR2 register remains canonical when Upper Address Ignore Version 2 is enabled.

Other registers such as Last x87 Data Pointer and IBS Data Cache Linear Address Register, which hold virtual addresses, may no longer be canonical and include the software tag when Upper Address Ignore Version 2 is enabled.