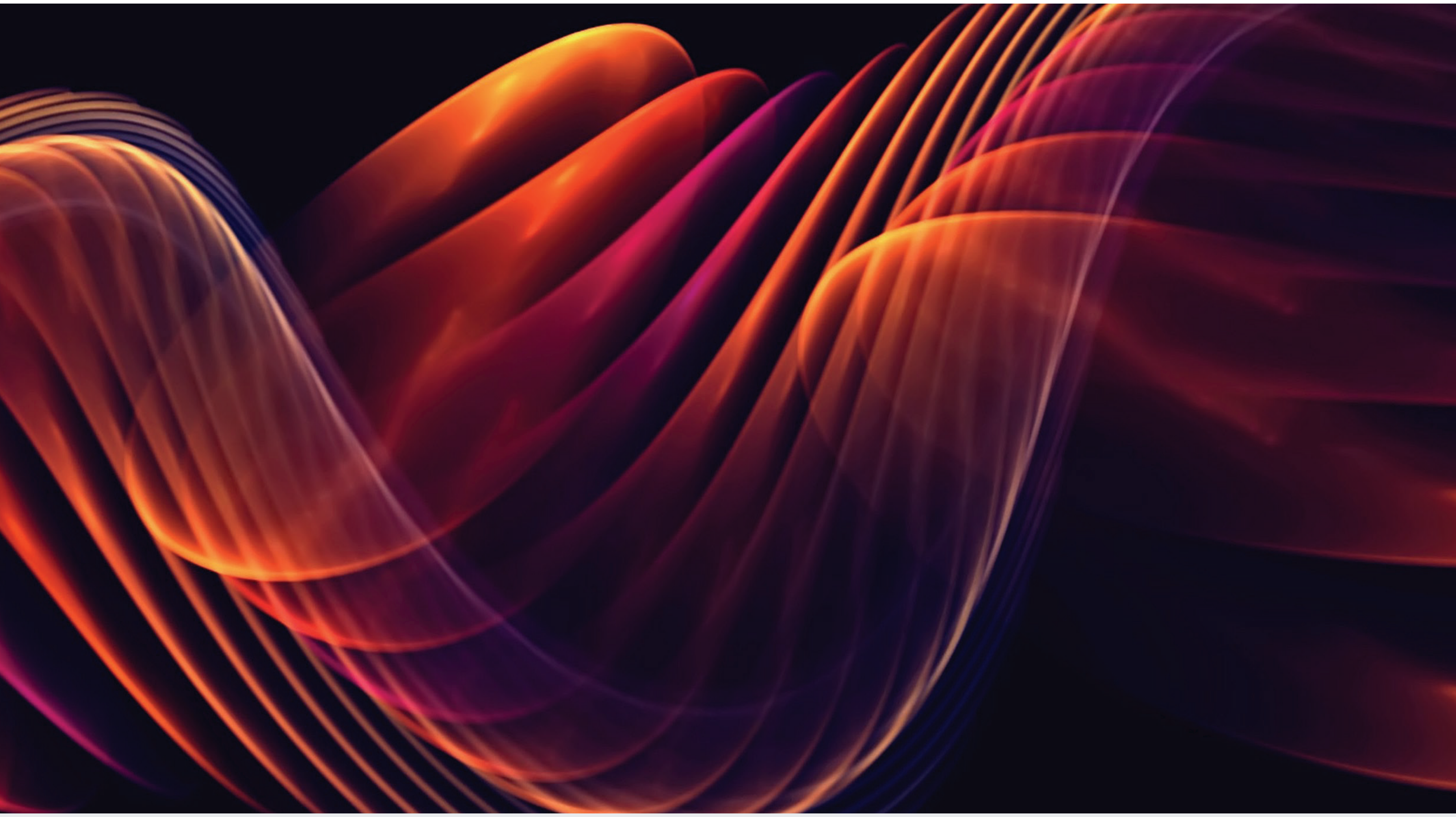
AMD



WHITE PAPER

TECHNICAL UPDATE REGARDING SPECULATIVE RETURN STACK OVERFLOW

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1. INTRODUCTION

This document describes new architectural features and CPUID bits related to the Speculative Return Stack Overflow (SRSO) vulnerability. This information is intended to assist operating system and hypervisor developers with the mitigation of this vulnerability.

2. ENUMERATION OF NEW CAPABILITIES

AMD is defining five new CPUID bits to assist with the enumeration of capabilities related to SRSO:

CPUID Fn8000_0021_EAX[31] (SRSO_MSR_FIX)
If this bit is 1, it indicates that software may use MSR BP_CFG[BpSpecReduce] to mitigate SRSO.

CPUID Fn8000_0021_EAX[30] (SRSO_USER_KERNEL_NO) -- If this bit is 1, it indicates the CPU is not subject to the SRSO vulnerability across user/kernel boundaries.

CPUID Fn8000_0021_EAX[29] (SRSO_NO) – If this bit is 1, it indicates the CPU is not subject to the SRSO vulnerability.

CPUID Fn8000_0021_EAX[28] (IBPB_BRTYPE) – If this bit is 1, it indicates that MSR 49h (PRED_CMD) bit 0 (IBPB) flushes all branch type predictions from the CPU branch predictor.

CPUID Fn8000_0021_EAX[27] (SBPB) – If this bit is 1, it indicates support for the Selective Branch Predictor Barrier, discussed later.

3. SUSCEPTIBILITY AND MITIGATION

Processors which set SRSO_NO=1 are not vulnerable to any forms of SRSO and do not require any software mitigations for SRSO. Processors which do not set SRSO_NO but set SRSO_USER_KERNEL_NO=1 are not vulnerable to SRSO across the user/kernel boundary specifically, meaning that code executed at CPL3 cannot influence the branch type used to predict branches in CPL0. These processors may be vulnerable to SRSO across other boundaries, such as across the guest/host boundary.

Processors which set SRSO_MSR_FIX=1 support an MSR bit which mitigates SRSO across guest/host boundaries. Software may enable this by setting bit 4 (BpSpecReduce) of MSR C001_102E. This bit can be set once during boot and should be set identically across all processors in the system.

Mitigation of SRSO across user/user or VM/VM boundaries requires the use of IBPB unless SRSO_NO is 1.

4. BRANCH PREDICTOR BARRIER CHANGES

When IBPB_BRTYPE is supported, PRED_CMD bit 0 (IBPB) may be used to flush all older branch type predictions from the CPU branch predictor in addition to all older indirect branch predictions. On processors subject to the SRSO vulnerability, this may be used when transitioning between address spaces and/or privilege domains to mitigate SRSO by flushing any attacker-controlled branch type information. In some implementations, IBPB only flushes branch prediction information related to the current thread.

When SBPB is supported, software may write PRED_CMD bit 7 to 1 to initiate a Selective Branch Predictor Barrier (SBPB). This is a write-only bit. Setting this bit to 1 prevents the processor from using older indirect branch target predictions to influence future indirect branch predictions. This applies to JMP indirect, CALL indirect, and RET (return) instructions. SBPB is not guaranteed to flush older branch type predictions from the CPU branch predictor. In some implementations, SBPB only flushes indirect prediction information related to the current thread. If SRSO mitigation is not required or is disabled, software may use SBPB on context/virtual machine switch to help protect against vulnerabilities like Spectre v2.

If software writes PRED_CMD with both bits 0 and 7 set to 1, the processor performs an IBPB operation.

5. ENUMERATION ON EXISTING AMD CPUS

On AMD “Zen” and “Zen2” microarchitecture-based CPUs, the IBPB operation flushes branch type predictions from the branch predictor but does not set the IBPB_BRTYPE bit. Bare-metal software that detects a “Zen” or “Zen2” microarchitecture-based CPU should assume IBPB_BRTYPE=1 behavior exists. Hypervisor software should synthesize the value of IBPB_BRTYPE on these platforms so guest software can use CPUID to determine IBPB capabilities.

When the appropriate microcode patch is loaded on “Zen3” and “Zen4” microarchitecture-based CPUs, the IBPB operation flushes branch type predictions and the SBPB operation is supported but neither CPUID bit is set by hardware. Bare-metal software that detects a microcode patch version equal or greater than the version listed in AMD-SB-7005, the “Return Address Predictor Security Bulletin” *, should assume IBPB_BRTYPE=1 behavior and the existence of the SBPB feature. Hypervisor software should synthesize the value of both the IBPB_BRTYPE and SBPB CPUID bits on these platforms for use by guest software.

> All other SRSO CPUID bits return 0 on existing AMD processors through "Zen4" but may be set on future AMD processors.

*See **https://www.amd.com/en/resources/product-security/bulletin/amd-sb-7005.html** for more information.

“Zen” microarchitecture-based CPUs include Family 17h Models 00-2Fh and Models 50-5Fh. “Zen2” microarchitecture-based CPUs include Family 17h Models 30-4Fh, Models 60-7Fh, and Models A0-AFh.
https://www.amd.com/en/resources/product-security/bulletin/amd-sb-7005.html

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