Intel® Itanium® Architecture Software Developer's Manual Specification Update

December 2002

Notice: Intel® Itanium® architecture processors may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in processor specification updates.

Document Number: 248699-007

Contents

Revision History

Date	Version Number	Description
December 2002	007	Added clarifications on PSR.dt serialization (Table 3-2 and Section 8.3, Volume 2). Clarified PSR requirements for `br.ia`/`rfi` instructions during PSR.is transition (pp. 3-18, 3-22, 3-204, 3-205, and 3-233 in Volume 3). Added Illegal Operation Fault to `fnma` instruction page (p. 3-81, Volume 3). Revised figures and tables for CPUID Register 4 (Table 3-8 and Figure 3-12, Volume 1).
June 2002	001-006	Changes from previous Software Developer's Manual Specification Updates were incorporated into version 2.1 of the Software Developer's Manual published October 2002.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications, and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document #
Intel® Itanium® Architecture Software Developer's Manual, Volume 1: Application Architecture	245317-004
Intel® Itanium® Architecture Software Developer's Manual, Volume 2: System Architecture	245318-004
Intel® Itanium® Architecture Software Developer's Manual, Volume 3: Instruction Set Reference	245319-004

Nomenclature

Specification Changes are modifications to the current published specifications for Intel® Itanium® architecture processors. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further explain a specification's interpretation. These clarifications will be incorporated in the next release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the *Intel® Itanium® Architecture Software Developer's Manual*.

Summary Table of Changes

The following tables indicate the specification changes, specification clarifications, or documentation changes that apply to the *Intel® Itanium® Architecture Software Developer's Manual*.

Specification Changes

No.	Page	SPECIFICATION CHANGES
1	8	Volume 1: ao bit added to CPUID Register 4

Specification Clarifications

No.	Page	SPECIFICATION CLARIFICATIONS
1	9	Volume 2: PSR.dt serialization clarification
3	9	Volume 3: Clarification on PSR requirements for br.ia/rfi instructions during PSR.is transition
4	10	Volume 3: Added Illegal Operation fault to fnma I-page

Documentation Changes

No.	Page	DOCUMENTATION CHANGES
		None for this revision of this specification update

Specification Changes

1. Volume 1: ao bit added to CPUID Register 4

1. New Figure 3-12 (page 1:30) - added a new bit for ao:

2. Table 3-8 (page 1:30) has a new entry for ao:

Field	Bits	Description
lb	0	Processor implements the long branch (brl) instructions.
sd	1	Processor implements spontaneous deferral (see Section 5.5.5, “Deferral of Speculative Load Faults” on page 2:88).
ao	2	Processor implements 16-byte atomic operations (see “ld — Load”, “st — Store” and “cmpxchg — Compare and Exchange” instructions in Volume 3).
rv	63:3	Reserved.

Specification Clarifications

1. Volume 2: PSR.dt serialization clarification

1. Volume 2, Part I, Section 3.3.2, Table 3-2:

   On page 2:20, change the Serialization Required column for PSR.dt from:

   "data"

   to:

   "inst/data"

   and add a cross-reference to footnote c.

2. Volume 2: Unaligned debug fault clarification

1. Volume 2, Part I, Section 8.3, Debug vector page:
   On page 2:175, add the following paragraph to the end of the Notes section:

   If unaligned accesses are being performed with debug faults enabled, this fault may be taken even though there is not a match for the address programmed in the breakpoint register. See Volume 2, Section 7.1.2, "Debug Address Breakpoint Match Conditions."

3. Volume 3: Clarification on PSR requirements for `br.ia`/`rfi` instructions during PSR.is transition

1. `br.ia` instruction page (Volume 3, p. 3:18):

   a. Under "ia" bullet, add the following paragraph after the 3rd paragraph:

   Software must set PSR properly before branching to the IA-32 instruction set; otherwise processor operation is undefined. See Volume 2, Table 3-2, "Processor Status Register Fields" on page 2:19 for details.

   b. In the "Operation" section on page 3:22 under "case 'ia'," add below "`tmp_taken = 1;`":

```
if (PSR.ic==0 || PSR.dt==0 || PSR.mc==1 || PSR.it==0)
undefined_behavior();
```

2. `rfi` instruction page (Volume 3, p. 3:204):

   a. In the "Description" section, before the paragraph beginning "Software must issue a `mf` instruction...," add the following paragraph:

   If IPSR.is is 1, software must set other IPSR fields properly for IA-32 instruction set execution; otherwise processor operation is undefined. See Volume 2, Table 3-2, "Processor Status Register Fields" on page 2:19 for details.

   b. In the "Operation" section:

   Add the following below, "`if (CR[IPSR].is == 1) {`":

```
if (PSR.ic==0 || PSR.dt==0 || PSR.mc==1 || PSR.it==0)
undefined_behavior();
```

3. Table 3-1, Volume 3: Pseudo-Code Functions chapter:

   a. On page 3:253, replace the bullet list of faults in the Operation column of the tlb_translate() row of the Pseudo-Code Functions table with this new bullet list:

   - Unimplemented Data Address fault
   - Data Nested TLB fault

- Alternate Data TLB fault
- VHPT Data fault
- Data TLB fault
- Data Page Not Present fault
- Data NaT Page Consumption fault
- Data Key Miss fault
- Data Key Permission fault
- Data Access Rights fault
- Data Dirty Bit fault
- Data Access Bit fault
- Data Debug fault
- Unaligned Data Reference fault
- Unsupported Data Reference fault

b. Replace the bullet list of faults in the Operation column of the tlb_translate_nonaccess() row of the Pseudo-Code Functions table with this new bullet list:

- Unimplemented Data Address fault
- Data Nested TLB fault
- Alternate Data TLB fault
- VHPT Data fault
- Data TLB fault
- Data Page Not Present fault
- Data NaT Page Consumption fault
- Data Access Rights fault (`fc` only)

4. Volume 3: Added Illegal Operation fault to `fnma` I-page

1. Volume 3, `fnma` instruction page:

   On page 3:81, add “Illegal Operation fault” to the list of interruptions in the Interruptions section.

Documentation Changes

None for this revision of this specification update.