C

Alphabetical list of IA MMX™ Instruction Set Mnemonics

APPENDIX C
ALPHABETICAL LIST OF IA MMX™ INSTRUCTION SET MNEMONICS

The following table lists the mnemonics of the IA MMX™ instructions in alphabetical order. For each mnemonic, it summarizes the type of source data, the encoding of the first and second bytes in hexadecimal, and the format used.

Table C-1. IA MMX™ Instruction Set Mnemonics

MNEMONIC	OPERAND TYPES	Byte 1	Byte 2	Byte 3, [4]
EMMS	None	0F	77	mod-rm, [sib]
MOVD	register, memory/iregister	0F	6E	mod-rm, [sib]
MOVD	memory/iregister, register	0F	7E	mod-rm, [sib]
MOVQ	register, memory/register	0F	6F	mod-rm, [sib]
MOVQ	memory/register, register	0F	7F	mod-rm, [sib]
PACKSSDW	register, memory/register	0F	6B	mod-rm, [sib]
PACKSSWB	register, memory/register	0F	63	mod-rm, [sib]
PACKUSWB	register, memory/register	0F	67	mod-rm, [sib]
PADDB	register, memory/register	0F	FC	mod-rm, [sib]
PADDD	register, memory/register	0F	FE	mod-rm, [sib]
PADDSB	register, memory/register	0F	EC	mod-rm, [sib]
PADDSW	register, memory/register	0F	ED	mod-rm, [sib]
PADDUSB	register, memory/register	0F	DC	mod-rm, [sib]
PADDUSW	register, memory/register	0F	DD	mod-rm, [sib]
PADDW	register, memory/register	0F	FD	mod-rm, [sib]
PAND	register, memory/register	0F	DB	mod-rm, [sib]
PANDN	register, memory/register	0F	DF	mod-rm, [sib]
PCMPEQB	register, memory/register	0F	74	mod-rm, [sib]
PCMPEQD	register, memory/register	0F	76	mod-rm, [sib]

Table C-1. IA MMX™ Instruction Set Mnemonics (Contd.)

MNEMONIC	OPERAND TYPES	Byte 1	Byte 2	Byte 3, [4]
PCMPEQW	register, memory/register	0F	75	mod-rm, [sib]
PCMPGTB	register, memory/register	0F	64	mod-rm, [sib]
PCMPGTD	register, memory/register	0F	66	mod-rm, [sib]
PCMPGTW	register, memory/register	0F	65	mod-rm, [sib]
PMADDWD	register, memory/register	0F	F5	mod-rm, [sib]
PMULHW	register, memory/register	0F	E5	mod-rm, [sib]
PMULLW	register, memory/register	0F	D5	mod-rm, [sib]
POR	register, memory/register	0F	EB	mod-rm, [sib]
PSHIMD*	register, immediate	0F	72	mod-rm, imm
PSHIMQ*	register, immediate	0F	73	mod-rm, imm
PSHIMW*	register, immediate	0F	71	mod-rm, imm
PSLLD	register, memory/register	0F	F2	mod-rm, [sib]
PSLLQ	register, memory/register	0F	F3	mod-rm, [sib]
PSLLW	register, memory/register	0F	F1	mod-rm, [sib]
PSRAD	register, memory/register	0F	E2	mod-rm, [sib]
PSRAW	register, memory/register	0F	E1	mod-rm, [sib]
PSRLD	register, memory/register	0F	D2	mod-rm, [sib]
PSRLQ	register, memory/register	0F	D3	mod-rm, [sib]
PSRLW	register, memory/register	0F	D1	mod-rm, [sib]
PSUBB	register, memory/register	0F	F8	mod-rm, [sib]

Table C-1. IA MMX™ Instruction Set Mnemonics (Contd.)

MNEMONIC	OPERAND TYPES	Byte 1	Byte 2	Byte 3, [4]
PSUBD	register, memory/register	0F	FA	mod-rm, [sib]
PSUBSB	register, memory/register	0F	E8	mod-rm, [sib]
PSUBSW	register, memory/register	0F	E9	mod-rm, [sib]
PSUBUSB	register, memory/register	0F	D8	mod-rm, [sib]
PSUBUSW	register, memory/register	0F	D9	mod-rm, [sib]
PSUBW	register, memory/register	0F	F9	mod-rm, [sib]
PUNPCKHBW	register, memory/register	0F	68	mod-rm, [sib]
PUNPCKHDQ	register, memory/register	0F	6A	mod-rm, [sib]
PUNPCKHWD	register, memory/register	0F	69	mod-rm, [sib]
PUNPCKLBW	register, memory/register	0F	60	mod-rm, [sib]
PUNPCKLDQ	register, memory/register	0F	62	mod-rm, [sib]
PUNPCKLWD	register, memory/register	0F	61	mod-rm, [sib]
PXOR	register, memory/register	0F	EF	mod-rm, [sib]

Notes:

* These are not the actual mnemonics:

PSHIMD represents the PSLLD, PSRAD and PSRLD instructions when shifting by immediate shift counts.

PSHIMW represents the PSLLW, PSRAW and PSRLW instructions when shifting by immediate shift counts.

PSHIMQ represents the PSLLQ and PSRLQ instructions when shifting by immediate shift counts.

The instructions that shift by immediate counts are differentiated by the ModR/M bytes (See Appendix B).