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Introduction to the Intel Architecture MMX™ Technology

CHAPTER 1
INTRODUCTION TO THE INTEL ARCHITECTURE MMX™ TECHNOLOGY

1.1. ABOUT THE INTEL ARCHITECTURE MMX™ TECHNOLOGY

The media extensions for the Intel Architecture (IA) were designed to enhance performance of advanced media and communication applications. The MMX™ technology provides a new level of performance to computer platforms by adding new instructions and defining new 64-bit data types, while preserving compatibility with software and operating systems developed for the Intel Architecture.

The MMX technology introduces new general-purpose instructions. These instructions operate in parallel on multiple data elements packed into 64-bit quantities. They perform arithmetic and logical operations on the different data types. These instructions accelerate the performance of applications with compute-intensive algorithms that perform localized, recurring operations on small native data. This includes applications such as motion video, combined graphics with video, image processing, audio synthesis, speech synthesis and compression, telephony, video conferencing, 2D graphics, and 3D graphics

The IA MMX instruction set has a simple and flexible software model with no new mode or operating-system visible state. The MMX instruction set is fully compatible with all Intel Architecture microprocessors. All existing software continues to run correctly, without modification, on microprocessors that incorporate the MMX technology, as well as in the presence of existing and new applications that incorporate this technology.

1.1.1. Single Instruction, Multiple Data (SIMD) Technique

The MMX technology uses the Single Instruction, Multiple Data (SIMD) technique. This technique speeds up software performance by processing multiple data elements in parallel, using a single instruction. The MMX technology supports parallel operations on byte, word, and doubleword data elements, and the new quadword (64-bit) integer data type.

1.1.2. Performance Improvement

Modern media, communications, and graphics applications now include sophisticated algorithms that perform recurring operations on small data types. The MMX technology directly addresses the need of these applications. For example, most audio data is represented in 16-bit (word) quantities. The MMX instructions can operate on four of these words simultaneously with one instruction. Video and graphics information is commonly represented as palletized 8-bit (byte) quantities; one MMX instruction can operate on eight of these bytes simultaneously.

1.2. ABOUT THIS MANUAL

It is assumed that the reader is familiar with the Intel Architecture software model and Assembly language programming.

This manual describes the IA MMX instruction set and introduces the architectural features, instruction set, data types, data formats, application programming model, and system programming model of the MMX technology. It also explains how to use the new instructions to significantly increase the performance of applications.

In this context, architecture refers to the conceptual structure and functional behavior of MMX technology as seen by a programmer, but not the logical organization or performance aspects of the actual implementation.

This manual is organized into five chapters, including this chapter (Chapter 1), and four appendices:

Chapter 1—Introduction to the Intel Architecture MMX™ Technology

Chapter 2—Intel Architecture MMX™ Technology Features: This chapter provides an overview of the IA MMX technology and its new features.

Chapter 3—Application Programming Model: This chapter describes the software conventions and architecture of the IA MMX technology. It defines the steps for writing MMX code.

Chapter 4—System Programming Model: This chapter discusses interfacing with the operating system and compatibility with Intel Architecture.

Chapter 5—Intel Architecture MMX™ Instruction Set: This chapter details the instructions, mnemonics, and instruction notations. A full description including graphical representations of the new instructions is presented.

Appendix A—IA MMX™ Instruction Set Summary: This appendix summarizes the instructions by functional groups.

Appendix B—IA MMX™ Instruction Formats and Encodings: This appendix lists the instruction formats and encodings. It also lists a detailed break-down of the instruction operations and the supported data types.

Appendix C—Alphabetical list of IA MMX™ Instruction Set Mnemonics: This appendix summarizes operand types, encodings in hexadecimal, and the formats used.

Appendix D—IA MMX™ Instruction Set Opcode Map: This appendix provides a detailed encoding table of opcode mappings.

1.3. RELATED DOCUMENTATION

Refer to the following documentation for more information related to Intel Architecture:

Pentium® Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual. Intel Corporation, Order Number 240897.

Pentium® Pro Processor Developer's Manual, Volumes 2 and 3. Intel Corporation, Order Numbers 242691 and 242692.

Intel Architecture MMX™ Technology Developers' Manual - Intel Corporation, Order Number 243010.

Refer to Intel's corporate website for the latest information on related documentation:

http://www.intel.com