

# Architecture Specification: Intel® Trust Domain Extensions (Intel® TDX) Module

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# SECTION 1: INTRODUCTION AND OVERVIEW

## 1. About this Document

### 1.1. Scope of this Document

This document describes the architecture and the external Application Binary Interface (ABI) of the Intel® Trust Domain Extensions (Intel® TDX) module, implemented using the Intel TDX Instruction Set Architecture (ISA) extensions, for confidential execution of Trust Domains in an untrusted hosted cloud environment.

This document is a work in progress and is subject to change based on customer feedback and internal analysis. This document does not imply any product commitment from Intel to anything in terms of features and/or behaviors.

**Note:** The contents of this document are accurate to the best of Intel's knowledge as of the date of publication, though Intel does not represent that such information will remain as described indefinitely in light of future research and design implementations. Intel does not commit to update this document in real time when such changes occur.

### 1.2. Document Organization

The document has the following main sections:

- Section 1 contains an introduction to the document and an overview of the Intel TDX module.
- Section 2 contains the Intel TDX module architecture specification.
- Section 3 is an Application Binary Interface (ABI) function reference for the Intel TDX module.

### 1.3. Glossary

Table 1.1: Intel TDX Glossary

Acronym	Full Name	New for TDX	Description
ABI	Application Binary Interface	No	A programming interface defined at the binary level (i.e., instruction opcode and CPU registers). The Intel TDX module interface is specified as an ABI.
ACM	Authenticated Code Module	No	A code module that is designed to be loaded, verified and executed by the CPU in on-chip memory (CRAM).
N/A	Accessible (Memory)	No	Memory whose content is readable and/or writeable (e.g., TD private memory is accessible to the guest TD).
N/A	Addressable (Memory)	No	Memory that can be referred to by its address. The content of addressable memory might not necessarily be accessible (e.g., TDCS is not accessible to the host VMM).
CMR	Convertible Memory Range	Yes	A range of physical memory configured by BIOS and verified by MCHECK. MCHECK verification is intended to help ensure that a CMR may be used to hold TDX memory pages encrypted with a private HKID.
N/A	Enlightened OS	No	A TD OS is considered enlightened if it is aware that it is running as a TD (see Paravirtualization).
EPxE	Extended Paging Structures Cache	No	The CPU's cache of EPT intermediate translations (as opposed to TLB, which caches full LA or GPA to HPA translations).
GPA	Guest Physical Address	No	An address viewed as a physical address, from a guest VM's point of view. A GPA is subject to further translation (by EPT) to produce an HPA.

Acronym	Full Name	New for TDX	Description
N/A	Hidden	No	A resource or a data structure that is not directly addressable by software (except the Intel TDX module).
HKID	Host Key ID	Yes	When MKTME is activated, HKID is a key identifier for an encryption key used by one or more memory controllers on the platform.
N/A	Host VMM	Yes	The VMM that serves as a host to guest TDs. The term “host” is used to differentiate between the “host VMM” and future VMMs that may be nested within TDs.
HPA	Host Physical Address	No	A physical address at the host VMM level. This is the actual physical address used by the hardware (e.g., caches). See also PA.
KET	Key Encryption Table	Yes	A table held by each MKTME encryption engine, intended for holding encryption key information, indexed by HKID.
KOT	Key Ownership Table	Yes	An internal, hidden table held by the Intel TDX module, intended for controlling the assignment of HKIDs to TDs.
MBZ	Must Be Zero	No	Normally used to indicate that reserved fields must contain 0.
MKTME	Multi-Key TME	No	This SoC capability adds support to the TME to allow software to use one or more separate keys for encryption of volatile or persistent memory encryption. When used with TDX, it can provide confidentiality via separate keys for memory used by TDs. MKTME can be used with and without TDX extensions. <sup>1</sup>
MRTD	Measurement of Trust Domain	Yes	The SHA-384 measurement of a TD accumulated during TD build.
PA	Physical Address	No	The physical address used by the hardware (e.g., caches). See also HPA.
PAMT	Physical Address Metadata Table	Yes	An internal, hidden data structure used by the Intel TDX module, which is intended to hold the metadata of physical pages.
PV	Para-Virtualization	No	A virtualization technique where the VM can be aware it is being virtualized (as opposed to running directly on hardware).
RTMR	Run-Time Measurement Register	Yes	A SHA-384 measurement register that can be updated during TD run-time.
SEAM	Secure Arbitration Mode	Yes	See TDX ISA.
SEAMLDR	SEAM Loader	Yes	An ACM intended to load the Intel TDX module.
SEAMRR	SEAM Range Register	Yes	A range register used by the BIOS to help configure the SEAM memory range, where the Intel TDX module is loaded and executed.

<sup>1</sup> In this document, the term “MK-TME” is used to mean both the feature and the encryption engine itself.

Acronym	Full Name	New for TDX	Description
SEPT	Secure EPT	Yes	An Extended Page Table for GPA-to-HPA translation of TD private HPA. A Secure EPT is designed to be encrypted with the TD's ephemeral private key. SEPT pages are allocated by the host VMM via Intel TDX functions, but their content is intended to be hidden and is not architectural.
Intel® SGX	Intel® Software Guard Extensions	No	An Intel CPU mode and ISA extensions that support operation and management of Intel® SGX enclaves.
SoC	System on Chip	No	A whole system, including cores, uncore, interconnects etc., packaged as a single device.
SPA	System Physical Address	No	The physical address used by the hardware (e.g., caches). See also HPA.
TD	Trust Domain	Yes	Trust Domains (TDs) are designed to be hardware isolated Virtual Machines (VMs) deployed using Intel® Trust Domain Extensions (Intel® TDX).
TD OS	Trust Domain Operating System	Yes	The guest operating system that runs in a TD.
N/A	TD Private Memory (Access)	Yes	TD Private Memory is designed to hold TD private content, encrypted by the CPU using the TD ephemeral key.
N/A	TD Shared Memory (Access)	Yes	TD Shared memory is designed to hold content accessible to the TD and the host software (and/or other TDs). TD shared memory may be encrypted using MKTME keys managed by the VMM.
TDCS	Trust Domain Control Structure	Yes	Multi-page control structure for a TD. TDCS pages are allocated by the host VMM via Intel TDX functions, but their content is intended to be non-architectural and not directly accessible to software.
TDCX	Trust Domain Control Extension	Yes	4KB physical pages that are intended to hold parts of a TDCS.
TDR	Trust Domain Root	Yes	The root control structure for a TD. The TDR page is allocated by the host VMM via Intel TDX functions, but its content is intended to be non-architectural and not directly accessible to software.
TDMR	Trust Domain Memory Range	Yes	A range of memory, configured by the host VMM, that is covered by PAMT and is intended to hold TD private memory and TD control structures.
TDVPS	Trust Domain Virtual Processor State	Yes	A multi-page structure for holding a TD Virtual CPU (VCPU) state. TDVPS pages are allocated by the host VMM via Intel TDX functions, but their content is intended to be non-architectural and not directly accessible to software.
TDVPR	Trust Domain Virtual Processor Root	Yes	A 4KB physical page that is intended to be the root (first) page of a TDVPS.

Acronym	Full Name	New for TDX	Description
TDVPM	Trust Domain Virtual Processor Module	Yes	4KB physical pages that are intended to be the non-root pages of a TDVPS.
Intel® TDX	Intel® Trust Domain Extensions	Yes	An architecture, based on the TDX Instruction Set Architecture (ISA) extensions and the Intel TDX module, which supports operation and management of Trust Domains.
TDX ISA	Intel® TDX Instruction Set Architecture	Yes	Intel CPU Instruction Set Architecture (ISA) extensions that support the Intel TDX module: an isolated software module that facilitates the operation and management of Trust Domains.
TME	Intel® Total Memory Encryption	No	A memory encryption/decryption engine using an ephemeral platform key designed to encrypt memory contents exposed externally from the SoC.
XFAM	Extended Features Allowed Mask	Yes	A mask of CPU extended features (in XCR0 format) that the TD is allowed to use.

## 1.4. Notation

This section describes the notation used in this document.

### 1.4.1. Requirement and Definition Commitment Levels

When specifying requirements or definitions, the level of commitment is specified following the convention of [RFC 2119: Key words for use in RFCs to indicate Requirement Levels](#), as described in the following table:

**Table 1.2: Requirement and Definition Commitment Levels**

Keyword	Description
<b>Must</b>	" <b>Must</b> ", " <b>Required</b> " or " <b>Shall</b> " means that the definition is an absolute requirement of the specification.
<b>Must Not</b>	" <b>Must Not</b> " or " <b>Shall Not</b> " means that the definition is an absolute prohibition of the specification.
<b>Should</b>	" <b>Should</b> ", or the adjective " <b>Recommended</b> ", means that there may exist valid reasons in particular circumstances to ignore a particular item, but the full implications must be understood and carefully weighed before choosing a different course.
<b>Should Not</b>	" <b>Should Not</b> ", or the phrase " <b>Not Recommended</b> " means that there may exist valid reasons in particular circumstances when the particular behavior is acceptable or even useful, but the full implications should be understood, and the case must be carefully weighed before implementing any behavior described with this label.
<b>May</b>	" <b>May</b> ", or the adjective " <b>Optional</b> ", means that an item is discretionary. An implementation may choose to include the item, while another may omit the same item, because of various reasons.

## 1.5. References

### 1.5.1. Intel Public Documents

**Table 1.3: Intel Public Documents**

Reference	Document	Version & Date
Intel SDM	<a href="#">Intel® 64 and IA-32 Architectures Software Developer's Manual</a>	325462-072US, May 2020
ISA Extensions	<a href="#">Intel® Architecture Instruction Set Extensions and Future Features Programming Reference</a>	319433-040, June 2020

### 5 1.5.2. Intel TDX Public Documents

**Table 1.4: Intel TDX Public Documents**

Reference	Document	Version & Date
TDX Whitepaper	Intel Trust Domain Extensions Whitepaper	August 2020
Intel TDX Spec	Intel® Architecture Trust Domain Extensions (TDX) Specification	Rev. 1.0, August 2020
MKTMEi Spec	Intel® Architecture Memory Integrity Specification	Rev. 1.0, March 2020



## 2. Overview of Intel® Trust Domain Extensions

**Intel® Trust Domain Extensions (Intel® TDX)** refers to an Intel technology that extends Virtual Machines Extensions (VMX) and Multi-Key Total Memory Encryption (MKTME) with a new kind of virtual machine guest called a **Trust Domain (TD)**. A TD runs in a CPU mode that is designed to protect the confidentiality of its memory contents and its CPU state from any other software, including the hosting Virtual Machine Monitor (VMM), unless explicitly shared by the TD itself.

The TDX solution is built using a combination of Intel® Virtual Machine Extensions (VMX) and Multi-Key Total Memory Encryption (MK-TME), as extended by the **Intel® Trust Domain Extensions Instruction Set Architecture (Intel TDX ISA)**. An attested software module called the **Intel TDX module** is designed to implement the TDX architecture.

The platform is managed by a TDX-aware **host VMM**. As shown in Figure 2.1 below, a host VMM can launch and manage both guest TDs and legacy guest VMs. The host VMM maintains all legacy functionality from the legacy VMs' perspective; it is restricted only with regard to the TDs it manages.

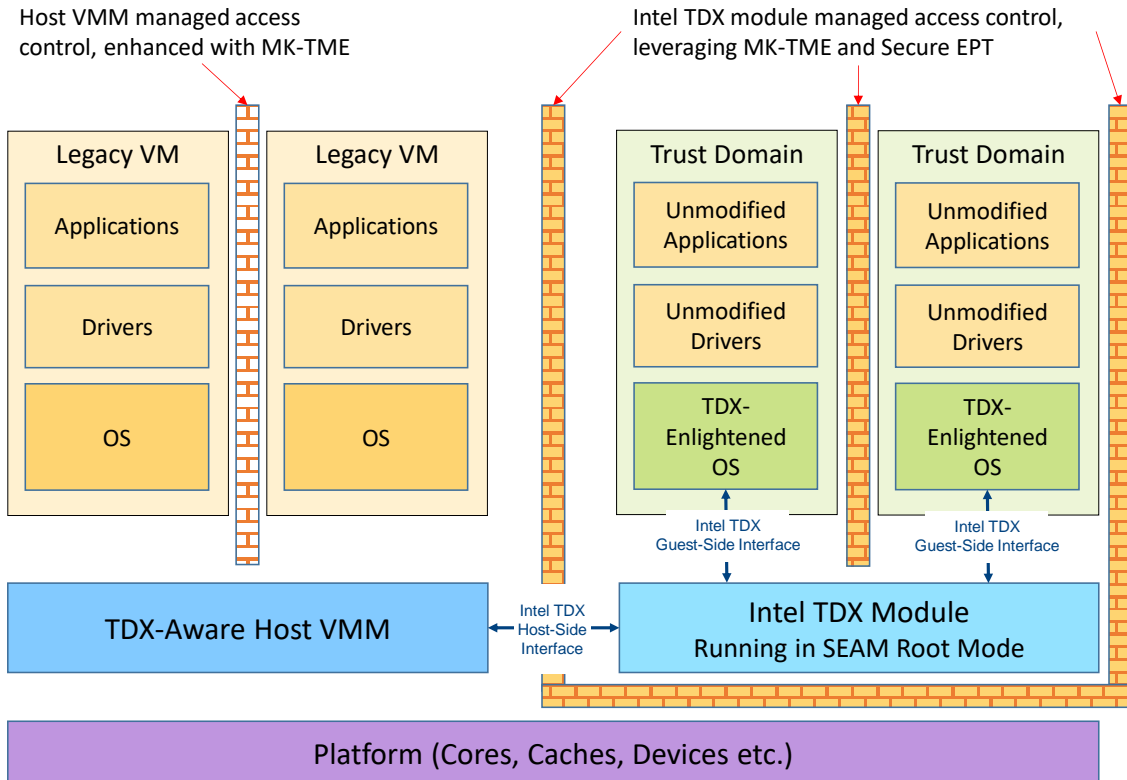


Figure 2.1: Intel® Trust Domain Extension Components Overview

### 2.1. Intel TDX Module Lifecycle

#### 2.1.1. Boot-Time Configuration and Intel TDX Module Loading

1. BIOS should configure the SEAMRR registers and prepares a table of **Convertible Memory Regions (CMRs)** – memory regions that can hold TD-private memory pages.
2. BIOS should then initiate MCHECK (as part of a µCode patch load) by WRMSR(0x79). MCHECK is designed to check the correct configuration of SEAMRR and CMRs and store the information in a well-known location in SEAMRR.
3. The host VMM can then load the Intel TDX module using the SEAMLDR ACM.

#### 2.1.2. Intel TDX Module Initialization, Enumeration and Configuration

1. After loading the Intel TDX module, the host VMM should call the TDH.SYS.INIT function to globally initialize the module.
2. The host VMM should then call the TDH.SYS.LP.INIT function on each logical processor. TDH.SYS.LP.INIT is intended to initialize the module within the scope of the Logical Processor (LP).
3. The host VMM should then call the TDH.SYS.INFO function to enumerate the Intel TDX module functionality and parameters, and retrieve the trusted platform topology and CMR information as previously checked by MCHECK.

4. Based on the above, the host VMM should then decide on a set of **Trust Domain Memory Regions (TDMRs)**. TDMR is a region of convertible memory that may contain some reserved sub-regions.
  5. The host VMM should then call the TDH.SYS.CONFIG function and pass TDMR information with other configuration information. TDH.SYS.CONFIG is intended to check the configuration information vs. the Intel TDX module's trusted internal data.
  6. The host VMM should then call the TDH.SYS.KEY.CONFIG function per package. TDH.SYS.KEY.CONFIG is intended to configure a CPU-generated random key that is used as the Intel TDX module's global private key.
  7. The host VMM should then use the TDH.SYS.TDMR.INIT function to initialize the TDMRs and their associated control structures.
- 10 The Intel TDX module lifecycle is detailed in Chapter 12.

## 2.2. Guest TD Life Cycle Overview

### 2.2.1. Guest TD Build

The host VMM can create a new guest TD by allocating and initializing a TD Root (TDR) control structure using the TDH.MNG.CREATE function. As an input to TDH.MNG.CREATE, the host VMM assigns the TD with a memory protection key identifier, also known as a Host Key ID (HKID). The HKID can be used by the CPU to tag memory accesses done by the TD and by the multi-key total memory encryption engines (MKTMEs) to select the encryption/decryption keys – the keys themselves are designed to not be exposed to the host VMM. The VMM should then program the HKID and encryption key into the MKTME encryption engines using the TDH.MNG.KEY.CONFIG function on each package.

Once the TD is assigned a key, the host VMM can build the TD Control Structure (TDCS) by adding control structure pages, using the TDH.MNG.ADDCX function, and initialize using the TDH.MNG.INIT function. It can then build the Secure EPT tree using the TDH.MEM.SEPT.ADD function and add the initial set of TD-private pages using the TDH.MEM.PAGE.ADD function. These pages typically contain Virtual BIOS code and data along with some clear pages for stacks and heap. Most of the guest TD code and data is dynamically loaded at a later stage. The guest TD can extend run-time measurement registers, designed to be securely maintained by the Intel TDX module, for the added contents using the TDH.MR.EXTEND function.

The host VMM can then create and initialize TD Virtual CPUs (VCPUs). After creating each VCPU using the TDH.VP.CREATE function, the VMM allocates a set of pages to hold the VCPU state (in a structure called TDVPS) using the TDH.VP.ADDCX function. The host VMM can then initialize the VCPU using the TDH.VP.INIT function.

After the initial set of pages is added and extended, the VMM can finalize the TD measurement using the TDH.MR.FINALIZE function.

### 2.2.2. Guest TD Execution

The host VMM may enter the TD (launch the TD for the first time, or resume a previously intercepted TD execution) using the TDH.VP.ENTER function. The Intel TDX module is designed to load CPU state from the TDVPS structure and perform VM entry to go into TDX non-root mode.

When TD exit is triggered, the Intel TDX module is designed to save CPU state into the TDVPS structure, load the CPU state saved on TD entry, and switch back to TDX root mode (SEAMRET) at the instruction following SEAMCALL. The VMM can then inspect the TD exit information in General Purpose Registers (GPRs).

### 2.2.3. Guest TD Management during its Run-Time

During TD lifetime, the VMM might need to dynamically control the TD and manage the resources assigned to it. The Intel TDX module provides the VMM with functions to support scenarios such as:

- Adding and removing TD pages.
- Changing page mapping sizes.
- Reclaiming the HKIDs from a TD, and assigning them to another TD.
- Destroying an existing TD.

### 2.3. Intel TDX Operation Modes and Transitions

The Intel TDX module is designed to provide two main new **logical** modes of operation built upon the new SEAM root and non-root CPU modes added to the Intel VMX architecture: TDX Root Mode, and TDX Non-Root Mode. Figure 2.2 below shows the Intel TDX logical modes and transitions (in red) on top of the CPU architectural modes.

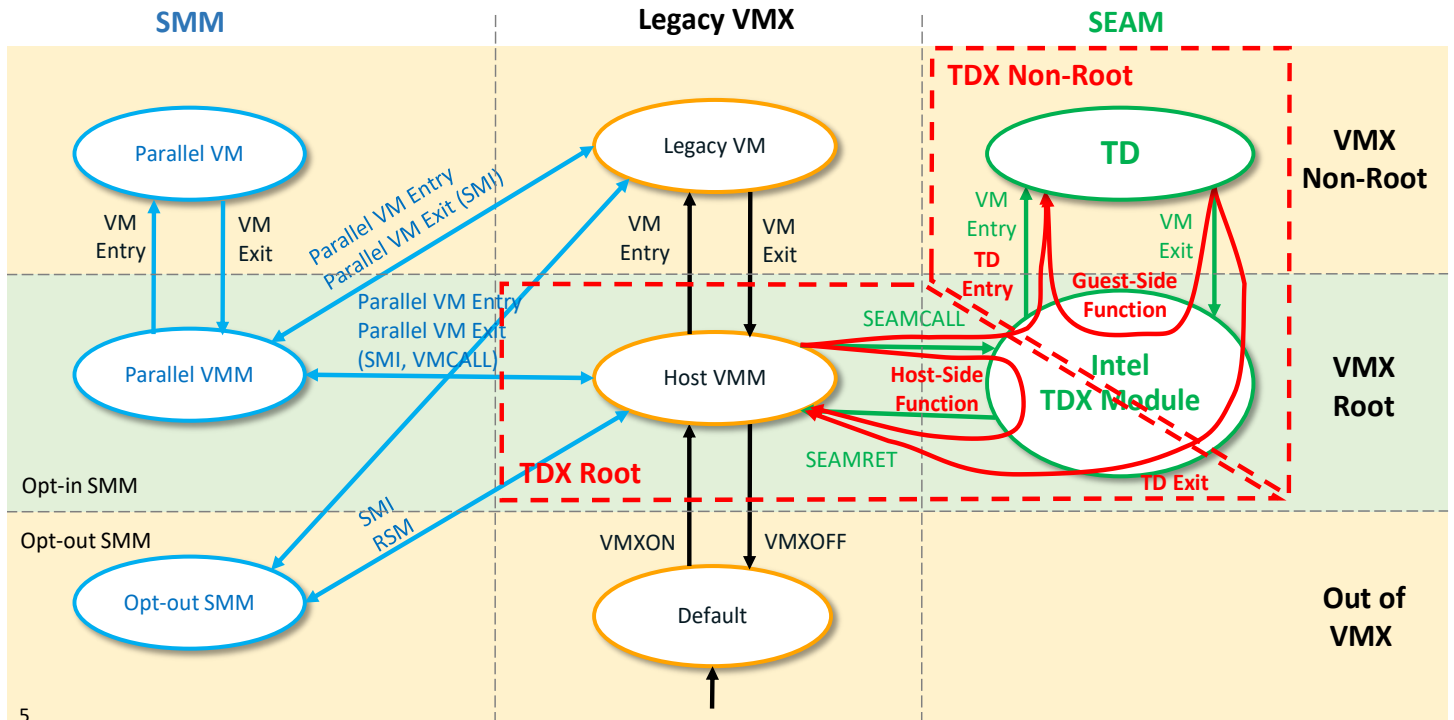


Figure 2.2: Overview of Intel TDX Modes & Transitions based on VMX and SEAM Modes and Transitions

The following table adds more details.

Table 2.1: Overview of Intel TDX Modes

Intel TDX Logical Mode	Intel VMX Mode	SEAM Mode	Description
<b>TDX Root</b>	VMX Root	Non-SEAM (mostly), SEAM (during host-side Intel TDX functions execution)	TDX root mode is mostly identical to the legacy VMX root operation mode. It is generally used for host VMM operation. Host-side Intel TDX functions, triggered by SEAMCALL, are provided by the Intel TDX module. Logically, host-side functions run in TDX root mode, though the CPU's SEAM mode is on.

Intel TDX Logical Mode	Intel VMX Mode	SEAM Mode	Description
<b>TDX Non-Root</b>	VMX Non-Root (mostly), VMX Root (during guest-side Intel TDX flows execution)	SEAM	<p>TDX non-root mode is used for TD guest operation. TDX non-root operation is similar to legacy VMX non-root operation, with changes and restrictions to better assure that no other software or hardware has direct visibility of the TD memory and state.</p> <p>The changes in TDX non-root mode vs. legacy VMX non-root operation are implemented by:</p> <ul style="list-style-type: none"> <li>The CPU running in SEAM non-root mode. This modifies the address translation to support Secure EPT and usage of private HKIDs, and it also modifies the VMX operation (entry, exit, etc.).</li> <li>The Intel TDX module, acting as the root VMM for the guest TD, using VMX and SEAM to virtualize the CPU behavior and emulate the required TDX non-root behavior.</li> </ul> <p>Guest-side Intel TDX flows, triggered by a VM Exit, are provided by the Intel TDX module. Logically, guest-side functions run in TDX non-root mode, though the CPU runs VMX root mode.</p> <p>TDX non-root operation is described in Chapter 9.</p>

**Intel TDX transitions** between TDX root operation and TDX non-root operation include **TD Entries**, from TDX root to TDX non-root mode, and **TD Exits** from TDX non-root to TDX root mode. A TD Exit might be **asynchronous**, triggered by some external event (e.g., external interrupt or SMI) or an exception, or it might be **synchronous**, triggered by a TDCALL(TDG.VP.VMCALL) function.

## 2.4. Guest TD Private Memory Protection

### 2.4.1. Memory Encryption

The Intel TDX module helps protect guest TD private memory using memory encryption and integrity protection as enabled by the CPU's MKTME and TDX ISA features. The Intel TDX module adds **key management functionality** to help enforce its security objectives.

Memory encryption is designed to be performed by encryption engines that reside at each memory controller. An encryption engine holds a table of encryption keys, known as the Key Encryption Table (KET). An encryption key is selected for each memory transaction based on a **Host Key Identifier (HKID)** that should be provided with the transaction.

In the first generation of MKTME, HKID is "stolen" from the physical address by allocating a configurable number of bits from the top of the physical address. TDX ISA is designed to further partition the HKID space into **shared HKIDs** for legacy MKTME accesses and **private HKIDs** for SEAM-mode-only accesses. Future generations might choose to express HKID differently.

During TDX non-root operation, memory accesses can be qualified as either shared or private, based on the value of a new SHARED bit in the Guest Physical Address (GPA). Shared accesses are intended to behave as legacy memory accesses and use the upper bits of the host physical address as an HKID, which must be from the range allocated to legacy MKTME. Private accesses use the guest TD's private HKID.

The host-side Intel TDX functions help provide the means for the host VMM to manage HKID assignment to guest TDs, configure the memory encryption engines, etc., while better assuring proper operation to help maintain the TDX's security objectives. By design, the host VMM does not have access to the encryption keys.

Encryption-based memory protection is described in the [MKTME PAS] and [SEAM PAS]. Key management is described in Chapter 4.

### 2.4.2. Address Translation

Guest Physical Address (GPA) space is divided into private and shared sub-spaces, determined by the SHARED bit of GPA.

As designed, the CPU translates shared GPAs using the Shared EPT, which resides in host VMM memory. The Shared EPT is directly managed by the host VMM – the same as with legacy VMX.

As designed, the CPU translates private GPAs using a separate Secure EPT. The Secure EPT pages are encrypted and integrity-protected with the TD’s ephemeral private key. The Secure EPT is not intended to be directly accessible by any software other than the Intel TDX module, nor by any devices. Secure EPT can be managed indirectly by the host VMM, using Intel TDX functions. The Intel TDX module helps ensure that the Secure EPT security properties are kept. At the end of translation, the CPU sets the HKID bits in the HPA to the TD’s assigned HKID.

5

TD private memory management is described in Chapter 7.

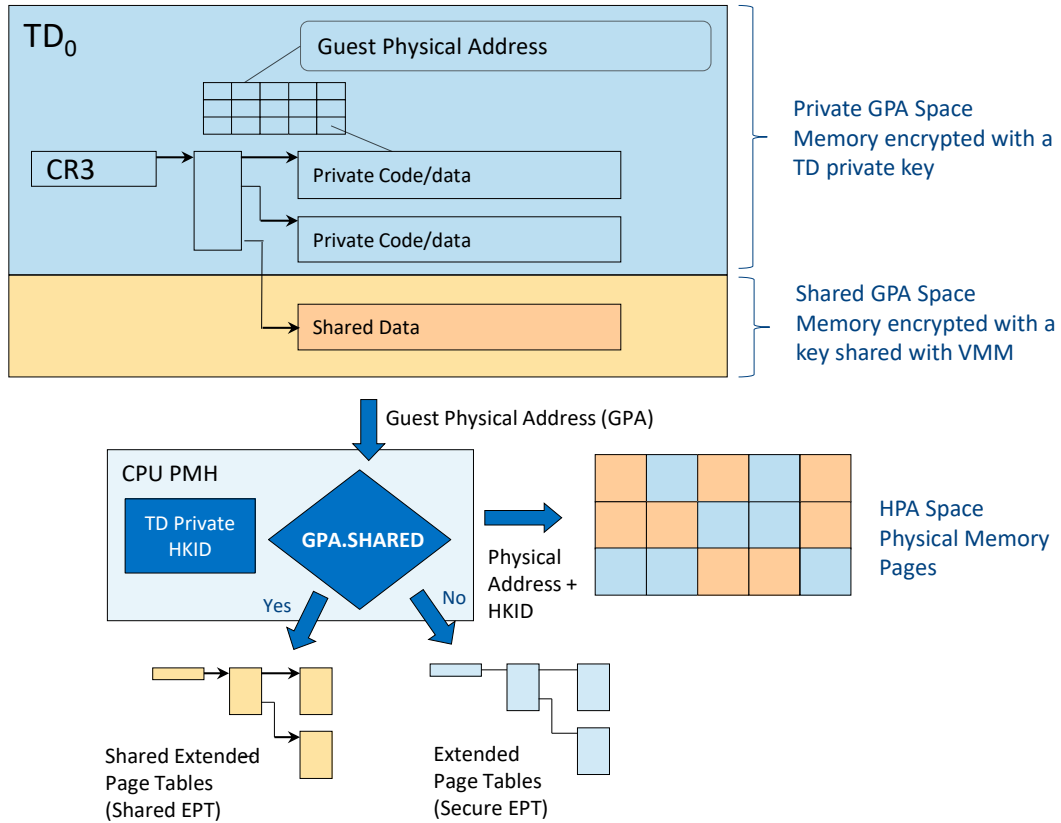


Figure 2.3: Secure EPT Concept

### 2.5. Guest TD State Protection

10 Intel TDX helps protect the confidentiality and integrity of a guest TD and the state of its Virtual CPUs (VCPUs) with the following mechanisms:

**Protected Control Structures** TD-scope and TD VCPU-scope control structures, which hold guest TD metadata and TD VCPU state, are not directly accessible to any software (besides the Intel TDX module) or devices. As designed, the control structures are encrypted and integrity-protected with a private key, and managed by Intel TDX functions. TD control structures are described in Chapter 5.

**VCPU State on TD Transitions** On asynchronous TD exits, which happen due to exceptions or external events, the CPU state is saved to the VCPU control structures, and a synthetic state is loaded into the CPU registers. On the following TD Entry, the CPU state is restored from the protected control structures.

On synchronous TD-initiated exit, using the TDCALL(TDG.VP.VMCALL) function, selected GPR and XMM state can be passed as-is to the host VMM. On the following TD entry, that state can be passed back as-is to the guest TD.

### 2.6. Intel TDX I/O Model

The TD guest can use the following I/O models:

- Paravirtualized devices
- Paravirtualized devices with MMIO emulation
- Direct assignment of devices to a TD

15

The Intel TDX architecture does not provide specific mechanisms for trusted I/O. Any integrity or confidentiality protection of data submitted to or received from physical or emulated devices must be done by the guest software using cryptography.

Intel TDX I/O is detailed in Chapter 11.

5 **2.7. Measurement and Attestation**

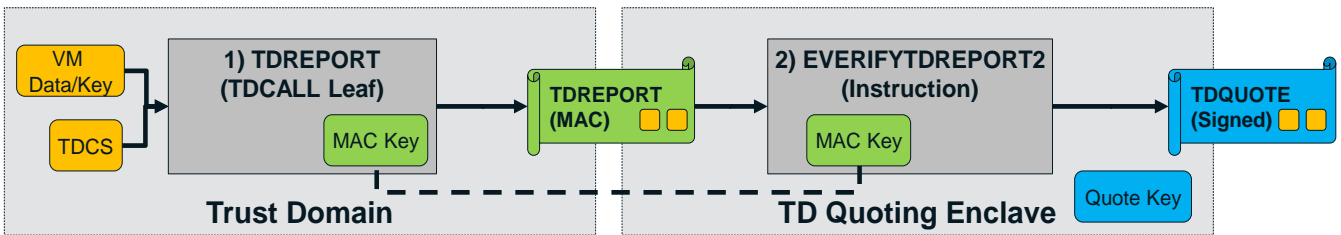
As designed, during TD launch, the initial contents and configuration of the TD are recorded by the Intel TDX module. In addition, run-time measurement registers can be used by the guest TD software, e.g., to measure a boot process. At run-time, the Intel TDX module reuses the Intel® Software Guard Extensions (Intel® SGX) attestation infrastructure to provide support for attesting to these measurements as described below.

10 Intel TDX attestation is intended to be used in two phases:

1. Software within the guest TD can use the TDCALL(TDG.MR.REPORT) function to request the Intel TDX module to generate an integrity-protected TDREPORT structure. The Intel TDX ISA provides support for enabling the Intel TDX module to create this structure that includes the TD’s measurements, the Intel TDX module’s measurements, and a value provided by the guest TD software. This will typically be an asymmetric key that the attestation verifier can use to establish a secure channel or protect sensitive data to be sent to the TD software.
2. An Intel SGX Quoting Enclave, written specifically to support quoting Intel TDX TDs, uses a new ENCLU instruction leaf, EVERIFYTDREPORT2, to help check the integrity of the TDG.MR.REPORT. If it passes, the Quoting Enclave can use a certified quote signing key to sign a quote containing the guest TD’s measurements and the additional data being quoted.

20 The Quoting Enclave can run anywhere on the platform where Intel SGX is supported.

**Note:** Running Intel SGX enclaves within a guest TD is not supported.



**Figure 2.4: TD Attestation**

TD measurement and attestation is described in Chapter 10.

25 **2.8. Intel TDX Managed Control Structures**

As designed, the Intel TDX module holds and manages a set of control structures that are not directly accessible to software (except the Intel TDX module itself). The controls structures are encrypted with private keys and HKIDs, and their content is only accessible in SEAM mode. Most control structures are addressable by the host VMM, which is responsible for allocating the memory to hold them.

30 The Intel TDX module uses control structures to help manage TD-private memory, transitions into and out of TDX non-root operation (TD entries and TD exits), as well as processor behavior in TDX non-root operation.

**Table 2.2: TDX-Managed Control Structures Overview**

Scope	Name	Meaning	Description
Platform	KOT	Key Ownership Table	Designed to control private HKID assignment. KOT is internal to the Intel TDX module, intended not to be directly accessible to any other software.
	PAMT	Physical Address Metadata Table	The PAMT is designed to hold metadata of each page in a Trust Domain Memory Range (TDMR). It controls assignment of physical pages to guest TDs, etc. The PAMT is intended not to be directly accessible to software. It resides in memory allocated by the host VMM on TDX initialization.

Scope	Name	Meaning	Description
Guest TD	TDR	Trust Domain Root	The TDR is intended to be the root control structure of a guest TD. It controls the key management and build/teardown process. The TDR is not intended to be directly accessible to software. It resides in memory allocated by the host VMM, via Intel TDX interface functions.
	TDCS	Trust Domain Control Structure	The TDCS is intended to control the operation of a guest TD as a whole. The TDCS is not intended to be directly accessible to software. It resides in memory allocated by the host VMM, via Intel TDX interface functions.
	SEPT	Secure EPT	The TDX-managed Extended Page Table (EPT) tree, used to help securely manage address translation for the TD private pages. The SEPT is not intended to be directly accessible to software. SEPT pages reside in memory allocated by the host VMM via Intel TDX interface functions.
Guest TD VCPU	TDVPS	Trust Domain Virtual Processor State	The TDVPS helps control the operation and hold the state of a guest TD virtual processor. It holds the TD VMCS and its auxiliary structures as well as other non-VMX control and state fields. The TDVPS is not intended to be directly accessible to software. It resides in memory allocated by the host VMM, via Intel TDX interface functions.

Intel TDX control structures are described in Chapter 5.

## 2.9. Intel TDX Interface Functions

The Intel TDX module implements functions that are triggered by executing two TDX instructions:

- 5 **SEAMCALL** The instruction used by the host VMM to invoke **host-side TDX interface functions**. The desired interface function is selected by an input operand (**leaf number**, in RAX). Host-side interface function names start with TDH (Trust Domain Host).
- 10 **TDCALL** The instruction used by the guest TD software (in TDX non-root mode) to invoke **guest-side TDX functions**. The desired interface function is selected by an input operand (**leaf number**, in RAX). Guest-side interface function names start with TDG (Trust Domain Guest).

### 2.9.1. Host-Side (SEAMCALL Leaf) Interface Functions

**Table 2.3: Host-Side (SEAMCALL Leaf) Interface Functions for Intel TDX Module Management**

Interface Function Name	Leaf Number	Description
TDH.SYS.CONFIG	45	Globally configure the Intel TDX module
TDH.SYS.INFO	32	Get Intel TDX module information
TDH.SYS.INIT	33	Globally initialize the Intel TDX module
TDH.SYS.KEY.CONFIG	31	Configure the Intel TDX global private key on the current package
TDH.SYS.LP.INIT	35	Initialize the Intel TDX module per logical processor
TDH.SYS.LP.SHUTDOWN	44	Shutdown the Intel TDX module on the current LP
TDH.SYS.TDMR.INIT	36	Partially initialize a Trust Domain Memory Region (TDMR)

**Table 2.4: Host-Side (SEAMCALL Leaf) Interface Functions for TD Management**

Interface Function Name	Leaf Number	Description
TDH.MNG.ADDCX	1	Add a control structure page to a TD
TDH.MNG.CREATE	9	Create a guest TD and its TDR root page
TDH.MNG.INIT	21	Initialize per-TD control structures
TDH.MNG.KEY.CONFIG	8	Configure the TD private key on a single package
TDH.MNG.KEY.FREEID	20	Mark the guest TD's HKID as free
TDH.MNG.KEY.RECLAIMID	27	Reclaim the HKID assigned to a guest TD
TDH.MNG.RD	11	Read a TD-scope control structure field of a debuggable TD
TDH.MNG.VPFLUSHDONE	19	Check all of a guest TD's VCPUs have been flushed by TDH.VP.FLUSH
TDH.MNG.WR	13	Write a TD-scope control structure field of a debuggable TD

**Table 2.5: VCPU-Scope Host-Side (SEAMCALL Leaf) Interface Functions**

Interface Function Name	Leaf Number	Description
TDH.VP.ADDCX	4	Add a control structure page to a TD VCPU
TDH.VP.CREATE	10	Create a guest TD VCPU and its TDVPR root page
TDH.VP.ENTER	0	Enter TDX non-root operation
TDH.VP.FLUSH	18	Flush the address translation caches and cached TD VMCS associated with a TD VCPU
TDH.VP.INIT	22	Initialize the per-VCPU control structures
TDH.VP.RD	26	Read a TDVPS field
TDH.VP.WR	43	Write a TDVPS field

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**Table 2.6: Host-Side (SEAMCALL Leaf) Interface Functions for Physical Memory Management**

Interface Function Name	Leaf Number	Description
TDH.PHYMEM.CACHE.WB	40	Write back the contents of the cache on a package
TDH.PHYMEM.PAGE.RD	12	Read a debuggable guest TD private memory
TDH.PHYMEM.PAGE.RDMD	24	Read the metadata of a page in a TDMR
TDH.PHYMEM.PAGE.RECLAIM	28	Reclaim a physical memory page owned by a TD (i.e., TD private page, Secure EPT page or a control structure page)
TDH.PHYMEM.PAGE.WBINVD	41	Write back and invalidate all cache lines associated with the specified memory page and HKID
TDH.PHYMEM.PAGE.WR	14	Write a debuggable guest TD private memory

**Table 2.7: Host-Side (SEAMCALL Leaf) Interface Functions for TD Private Memory Management**

Interface Function Name	Leaf Number	Description
TDH.MEM.PAGE.ADD	2	Add a 4KB private page to a TD during TD build time



Interface Function Name	Leaf Number	Description
TDH.MEM.PAGE.AUG	6	Dynamically add a 4KB private page to an initialized TD
TDH.MEM.PAGE.DEMOTE	15	Split a 2MB or a 1GB private TD page mapping into 512 4KB or 2MB page mappings respectively
TDH.MEM.PAGE.PROMOTE	23	Merge 512 consecutive 4KB or 2MB private TD page mappings into one 2MB or 1GB page mapping respectively
TDH.MEM.PAGE.REMOVE	29	Remove a private page from a guest TD
TDH.MEM.RANGE.BLOCK	7	Block a TD private GPA range
TDH.MEM.RANGE.UNBLOCK	39	Remove the blocking of a TD private GPA range
TDH.MEM.SEPT.ADD	3	Add and map a 4KB Secure EPT page to a TD
TDH.MEM.SEPT.RD	25	Read a Secure EPT entry
TDH.MEM.SEPT.REMOVE	30	Remove a Secure EPT page from a TD
TDH.MEM.SEPT.WR	42	Write a Secure EPT entry
TDH.MEM.TRACK	38	Increment the TD's TLB tracking counter

**Table 2.8: Host-Side (SEAMCALL Leaf) Interface Functions for TD Measurement and Attestation**

Interface Function Name	Leaf Number	Description
TDH.MR.EXTEND	16	Extend the guest TD measurement register during TD build
TDH.MR.FINALIZE	17	Finalize the guest TD measurement register

### 2.9.2. Guest-Side (TDCALL Leaf) Interface Functions

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**Table 2.9: Guest-Side (TDCALL Leaf) Interface Functions**

Interface Function Name	Leaf Number	Description
TDG.MEM.PAGE.ACCEPT	6	Accept a pending private page into the TD
TDG.MR.REPORT	4	Creates a cryptographic report of the TD
TDG.MR.RTMR.EXTEND	2	Extend a TD run-time measurement register.
TDG.VP.CPUIDVE.SET	5	Control delivery of #VE on CPUID instruction execution
TDG.VP.INFO	1	Get TD execution environment information
TDG.VP.VEINFO.GET	3	Get Virtualization Exception Information for the recent #VE exception
TDG.VP.VMCALL	0	Call a host VM service

Intel TDX interface function details are described in Chapter 20.

### 3. Software Use Cases

This chapter summarizes the software use cases (also known as software flows) used with the Intel TDX module.

#### 3.1. Intel TDX Module Lifecycle

##### 3.1.1. Intel TDX Module Platform-Scope Initialization

- 5 This sequence is intended to be used by the host VMM to initialize the Intel TDX module at the platform scope.

**Table 3.1: Typical Intel TDX Module Platform-Scope Initialization Sequence**

Phase		Intel TDX Function	Scope	Execute On	Description
<b>Boot</b>	1	N/A	Platform	Each core	BIOS configures Convertible Memory Regions (CMRs); MCHECK checks them and securely stores the information.
<b>Intel TDX Module Loading</b>	2	N/A	Platform	Any one LP	OS/VMM launches the SEAMLDR ACM, which loads the Intel TDX module.
<b>Intel TDX Module Initialization</b>	3	TDH.SYS.INIT	Platform	Any one LP	Perform global initialization of the Intel TDX module.
	4	TDH.SYS.LP.INIT	LP	Each LP	Perform LP-scope, core-scope and package-scope initialization, checking and configuration of the platform and the Intel TDX module.
<b>Enumeration and Configuration</b>	5	TDH.SYS.INFO	Platform	Any LP	Retrieve Intel TDX module information and convertible memory (CMR) information.
	6	TDH.SYS.CONFIG	Platform	Any one LP	Configure the Intel TDX module with TDMR and PAMT setup.
	7	N/A	Package	Each Package	If any MODIFIED cache lines may exist for the PAMT ranges, flush them to memory using, e.g., WBINVD.
	8	TDH.SYS.KEY.CONFIG	Package	Each Package	Configure the Intel TDX global private key used for encrypting PAMT and TDR on the hardware (other TD-scope control structures are encrypted with their respective TD's ephemeral private keys).
At this point any Intel TDX function may be executed on any LP.					
<b>Memory Initialization</b>	9	TDH.SYS.TDMR.INIT (multiple)	Platform	One or more LPs	Called multiple times to gradually initialize the PAMT structure for each TDMR.
	Once each 1GB block of TDMR has been initialized by TDH.SYS.TDMR.INIT, it can be used to hold TD-private pages.				

##### 3.1.2. Intel TDX Module Shutdown and Update

- 10 This sequence is intended to be used by the host VMM to gracefully shut down the Intel TDX module and then load a new module. All guest TDs' context and memory are lost.

**Table 3.2: Typical Intel TDX Module Shutdown and Update Sequence**

Phase		Intel TDX Function	Scope	Execute On	Description
<b>Shutdown</b>	1	TDH.SYS.LP.SHUTDOWN	LP	Each LP	Mark the current LP as being shut down and prevent further SEAMCALLS.

Phase		Intel TDX Function	Scope	Execute On	Description
Update	2	N/A	LP	Selected LP	OS/VMM executes VMXOFF and sends INIT signal to all other LPs.
	3	N/A	LP	Other LPs	LP enters INIT state.
	4	N/A	LP	Selected LP	OS/VMM launches the SEAMLDR ACM in UPDATE scenario. SEAMLDR checks shutdown on all LPs and loads a new Intel TDX module.
	At this point, the initialization sequence continues in the same way as described in 3.1.1 above.				

### 3.2. TD Build

The following sequence is intended to be used by the host VMM to build a TD.

**Table 3.3: Typical TD Build Sequence**

	Step	Description	SEAMCALL Leaf Functions	
A	<b>TD Creation and Key Resource Assignment</b>	1	The host VMM finds/allocates a free HKID for the new TD.	TDH.MNG.CREATE TDH.MNG.KEY.CONFIG
		2	The host VMM allocates a 4K page for the TDR in TDMR. If any MODIFIED cache lines may exist for this page, the host VMM flushes them to memory using, e.g., CLFLUSHOPT or TDH.PHYMEM.PAGE.WBINVD.	
		3	The host VMM creates the new TD by calling the TDH.MNG.CREATE function (passing HPA of the TDR page). This initializes the target TDR page.	
		4	The TD host VMM configures the MKTME hardware with the TD's private key by calling the TDH.MNG.KEY.CONFIG function on each package.	
		5	At this point, the TD private memory is accessible. The VMM can use Intel TDX interface functions to create control structures and TD private pages as described below.	
B	<b>TDCS Memory Allocation and TD Initialization</b>	1	The host VMM allocates multiple 4KB TDCX pages for TDCS. The number of required TDCX pages is enumerated by TDH.SYS.INFO. If any MODIFIED cache lines may exist for these pages, the host VMM flushes them to memory using, e.g., CLFLUSHOPT or TDH.PHYMEM.PAGE.WBINVD.	TDH.MNG.ADDCX TDH.MNG.INIT
		2	For each TDCX page, the host VMM calls the TDH.MNG.ADDCX function (passing HPA of TDCX) to add the page to the TD.	
		3	The host VMM builds a TD_PARAMS structure. For example, the TD configuration parameters can be obtained from a TD manifest supplied by the TD owner.	
		4	The host VMM calls the TDH.MNG.INIT function (passing the TD_PARAMS structure) to initialize the TD.	
C		1	The host VMM allocates target pages for the VCPU's TDVPR and TDVPX pages in TDMR in the context of a TD. The number of required TDVPX pages is enumerated by TDH.SYS.INFO. If any MODIFIED cache lines may exist for these pages, the host VMM flushes them to memory using, e.g., CLFLUSHOPT or TDH.PHYMEM.PAGE.WBINVD.	TDH.VP.CREATE TDH.VP.ADDCX TDH.VP.INIT TDH.VP.WR

	Step	Description	SEAMCALL Leaf Functions
	<b>Virtual Processor Creation and Configuration (Executed per each VCPU)</b>	2 The host VMM creates a new TD virtual CPU by calling the TDH.VP.CREATE function (passing the HPA of the new TDVPR page and its owner TDR page).	
		3 For each TDVPX page, the TDRM calls the TDH.VP.ADDCX function (passing the HPA of the new TDVPX page and its parent TDVPR page).	
		4 The host VMM initializes the TD VCPU by calling the TDH.VP.INIT function (passing the HPA of its TDVPR page). It also passes a single 64b parameter that is later passed to the VBIOS in the initial value of RCX. This parameter can be used as a pointer to a configuration structure in shared memory.	
		5 The host VMM allocates Shared EPT for each VP.	
		6 The host VMM uses the TDH.VP.WR function to write to the TD VMCS Shared EPTP field.	
		7 The host VMM may modify a few TD VMCS execution control fields using TDH.VP.WR.	
D		<b>TD Boot Memory Setup</b>	
	2 The host VMM builds the TD Secure EPT by allocating physical pages and calling the TDH.MEM.SEPT.ADD function multiple times. If any MODIFIED cache lines may exist for these pages, the host VMM flushes them to memory using, e.g., CLFLUSHOPT or TDH.PHYMEM.PAGE.WBINVD.		
	3 The host VMM allocates the initial set of physical pages for the TD boot image and maps them into host address space. If any MODIFIED cache lines may exist for these pages, the host VMM flushes them to memory using, e.g., CLFLUSHOPT or TDH.PHYMEM.PAGE.WBINVD.		
	4 For each TD page: <ol style="list-style-type: none"> <li>1. The host VMM specifies a TDR as a parameter and calls the TDH.MEM.PAGE.ADD function. It copies the contents from the TD image page into the target TD page which is encrypted with the TD ephemeral key. TDH.MEM.PAGE.ADD also extends the TD measurement with the page GPA.</li> <li>2. The host VMM extends the TD measurement with the contents of the new page by calling the TDH.MR.EXTEND function on each 256-byte chunk of the new TD page.</li> </ol>		
E	<b>TD Measurement Finalization</b>	1 The host VMM calls the TDH.MR.FINALIZE function, which finalizes the TD measurement.	TDH.MR.FINALIZE
		2 At this point, the TD is finalized. <ul style="list-style-type: none"> <li>• Its measurement cannot be modified anymore (except the run-time measurement registers).</li> <li>• TD VCPUs can be entered using SEAMCALL(TDH.VP.ENTER).</li> </ul>	

### 3.3. TD Run Time

#### 3.3.1. Private Memory Management

##### 3.3.1.1. Dynamic Page Addition (Shared to Private Conversion)

The following sequence is intended to be used by the host VMM to dynamically add a page to a guest TD.

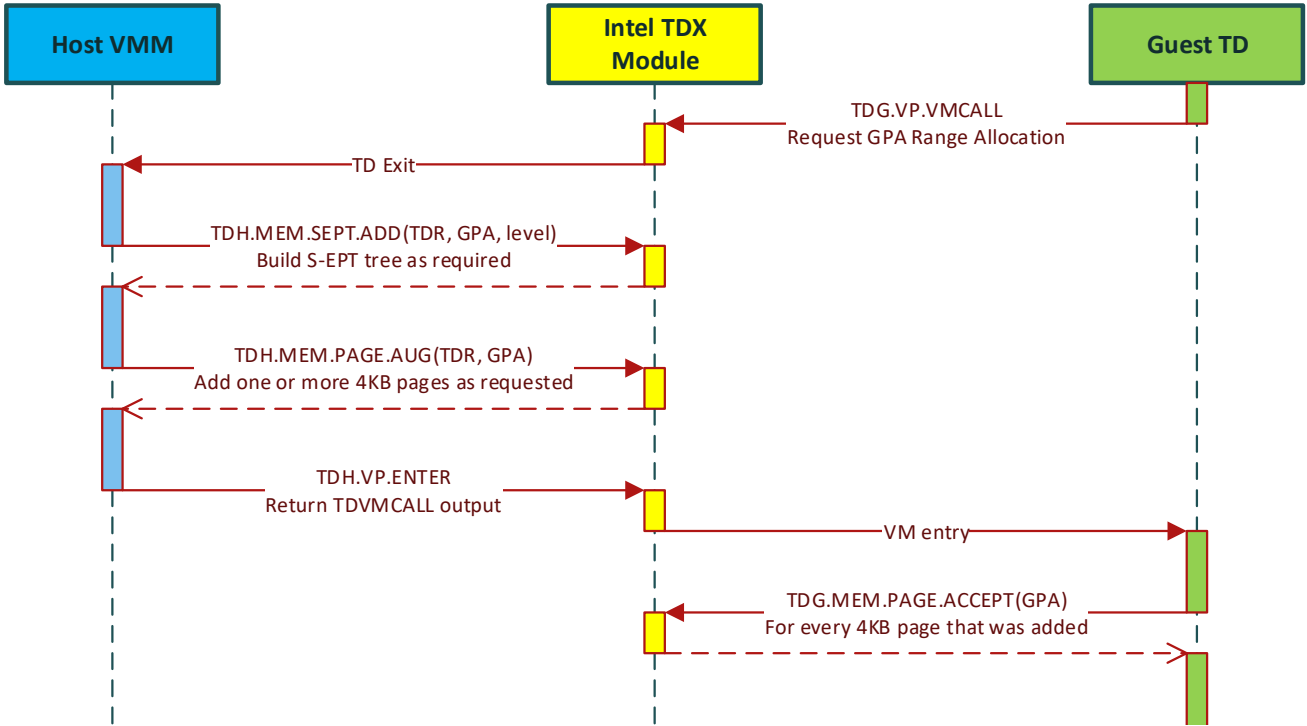


Figure 3.1: Typical Dynamic Page Addition Sequence

Table 3.4: Typical Dynamic Page Addition (Shared to Private Conversion) Sequence

Phase		Side	Intel TDX Function	Scope	Execute On	Description
Allocation Request	1	TD	TDG.VP.VMCALL	TD	Any LP	Optional software protocol: Request GPA range allocation.
Page Addition	2	VMM	TDH.MEM.SEPT.ADD	TD	Any LP	If required, update the Secure EPT.
	3	VMM	TDH.MEM.PAGE.AUG (multiple)	TD	Any LP	Add one or more new 4KB private pages.
	At this point, the new page is pending acceptance by the guest TD and cannot be accessed by it yet.					
	4	VMM	TDH.VP.ENTER	TD	Any LP	Optional software protocol: Return TDG.VP.VMCALL result.
Page Acceptance	5	TD	TDG.MEM.PAGE.ACCEPT (multiple)	TD	Any LP	Accept the new pending page(s). Content of each page is zeroed out.
	At this point, the new page can be accessed by the guest TD.					

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3.3.1.2. *Dynamic Page Removal (Private to Shared Conversion)*

The following sequence is intended to be used by the host VMM to dynamically remove a page from a guest TD. Dynamic page removal is detailed in 7.12.

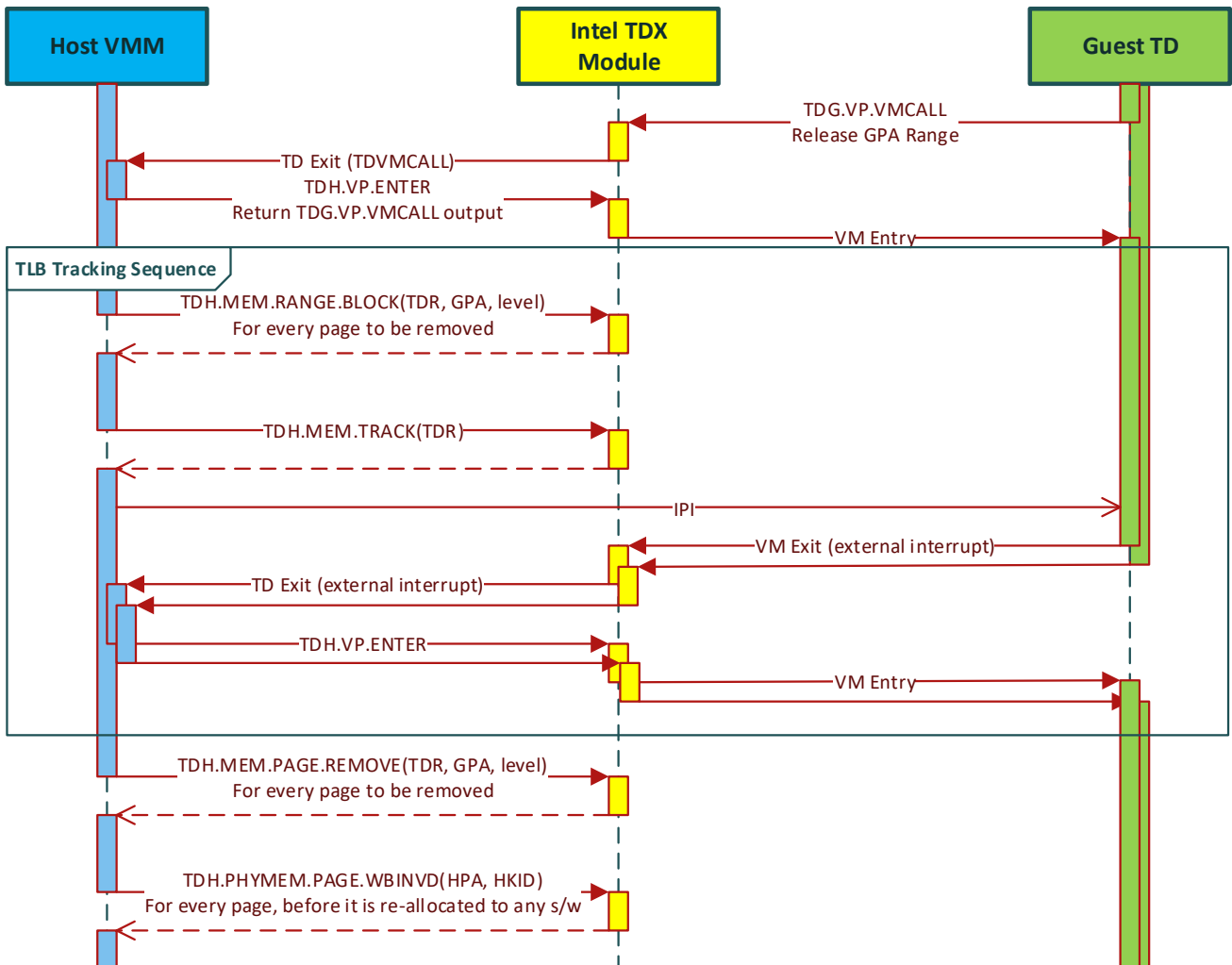


Figure 3.2: Typical Dynamic Page Removal Sequence

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Table 3.5: Typical Dynamic Page Removal (Private to Shared Conversion) Sequence

Phase		Side	Intel TDX Function	Scope	Execute On	Description
Ballooning Notification	1	TD	TDG.VP.VMCALL	TD	Any LP	Optional software protocol: Release GPA range.
	2	VMM	TDH.VP.ENTER	TD	Any LP	Optional software protocol: Return TDG.VP.VMCALL result.
TLB Tracking Sequence	3	VMM	TDH.MEM.RANGE.BLOCK (multiple)	TD	Any LP	Block private pages from further address translation.
	4	VMM	TDH.MEM.TRACK	TD	Any one LP	Increment the TD's TLB epoch.
	5	VMM	N/A	TD	Multiple LPs	Send an IPI, causing TD exit on any remote LP associated with a VCPU. Subsequent TDH.VP.ENTER will flush TLB.

Phase		Side	Intel TDX Function	Scope	Execute On	Description
Page Removal	6	VMM	TDH.MEM.PAGE.REMOVE (multiple)	TD	Any LP	Clear Secure EPT entry, and mark the physical page as free.
Cache Flushing	Before re-allocating any of the removed pages to any use, the host VMM must assure none of the cache lines of the removed pages are in the MODIFIED state to avoid corruption due to cache line aliasing. This is done using one of the following methods:					
	7a	VMM	TDH.PHYMEM.PAGE.WBINVD (multiple)	TD	Any one LP	Flush the cache lines of the removed page(s).
	7b	VMM	WBNOINVD	Platform	One LP per package <sup>2</sup>	Globally write back all caches.
	7c	VMM	WBINVD	Platform	One LP per package <sup>3</sup>	Globally write back and invalidate all caches.

**3.3.1.3. Page Promotion (Mapping Merge)**

Page size promotion is intended to be used by the host VMM to merge 512 pages mapped as 4KB or 2MB into a single page mapped as 2MB or 1GB, respectively. It is detailed in 7.10.

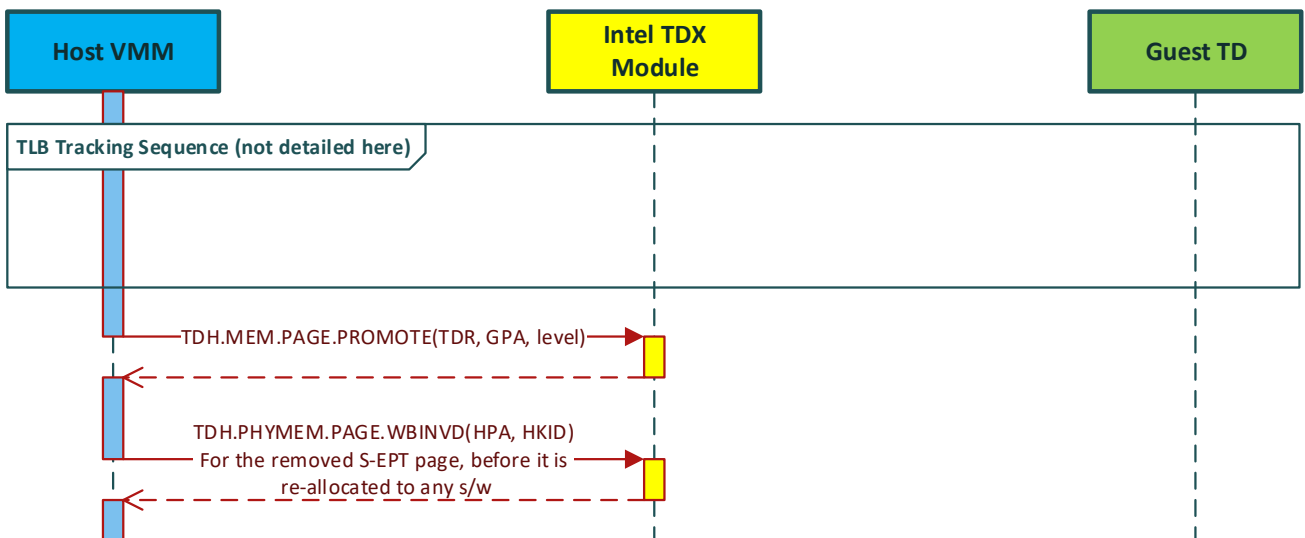


Figure 3.3: Typical Page Promotion Sequence

<sup>2</sup> Some CPUs may require running WBNOINVD per core.

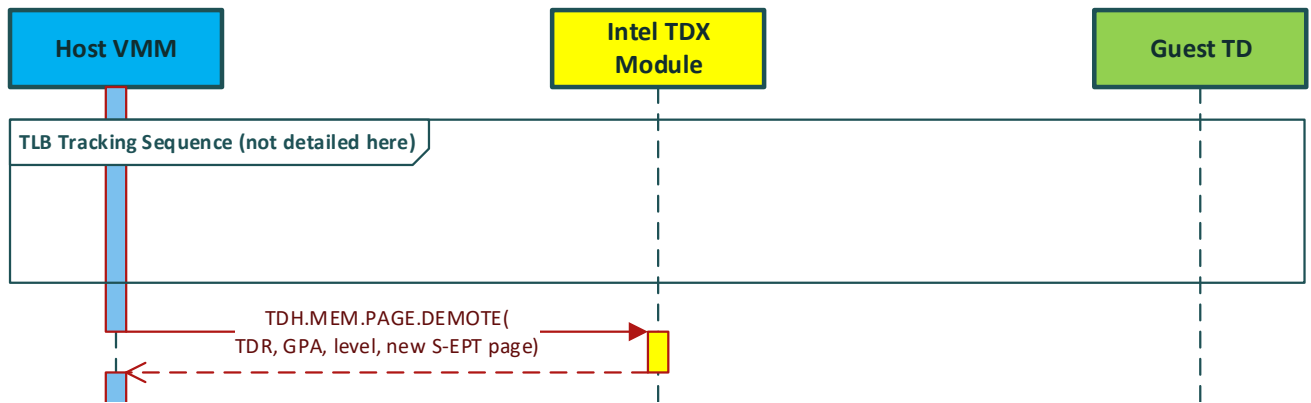
<sup>3</sup> Some CPUs may require running WBINVD per core.

**Table 3.6: Typical Page Promotion (Mapping Merge) Sequence**

Phase		Intel TDX Function	Scope	Execute On	Description
TLB Tracking Sequence	1	TDH.MEM.RANGE.BLOCK	TD	Any LP	Block the GPA range to be merged from further address translation.
	2	TDH.MEM.TRACK	TD	Any one LP	Increment the TD's TLB epoch.
	3	N/A	TD	Multiple LPs	Send an IPI, causing TD exit on any remote LP associated with a VCPU. Subsequent TDH.VP.ENTER will flush TLB.
Promotion	4	TDH.MEM.PAGE.PROMOTE	TD	Any LP	Merge small pages in the GPA range into a large page.
Cache Flushing	5	TDH.PHYMEM.PAGE.WBINVD	TD	Any LP	Flush the removed Secure EPT page's cache lines.

**3.3.1.4. Page Demotion (Mapping Split)**

Page size demotion is intended to be used by the host VMM to split a page mapped as 1GB or 2MB into 512 pages mapped as 2MB or 4KB, respectively. It is detailed in 7.11.



**Figure 3.4: Typical Page Demotion Sequence**

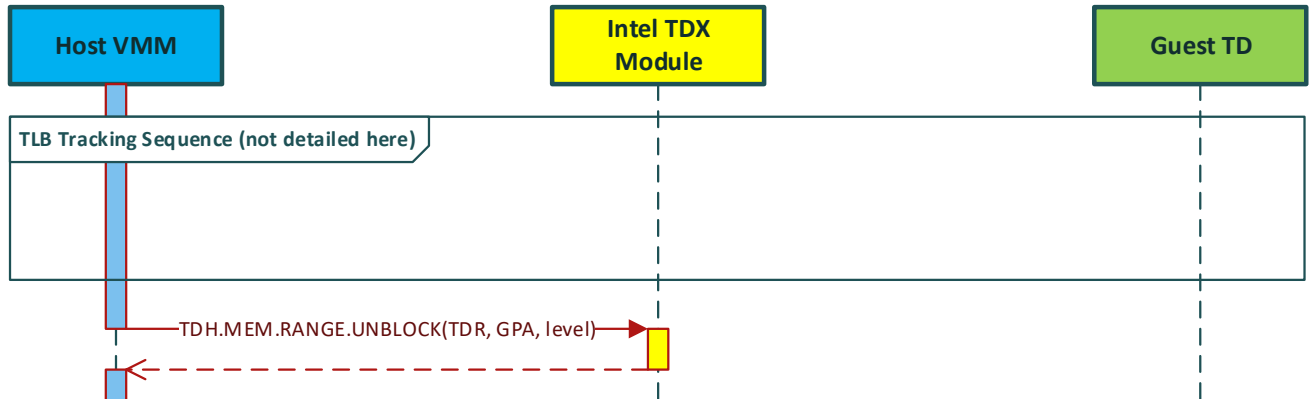
**Table 3.7: Typical Page Demotion (Mapping Split) Sequence**

Phase		Intel TDX Function	Scope	Execute On	Description
TLB Tracking Sequence	1	TDH.MEM.RANGE.BLOCK	TD	Any LP	Block private large page from further address translation.
	2	TDH.MEM.TRACK	TD	Any one LP	Increment the TD's TLB epoch.
	3	N/A	TD	Multiple LPs	Send an IPI, causing TD exit on any remote LP associated with a VCPU. Subsequent TDH.VP.ENTER will flush TLB.
Demotion	4	TDH.MEM.PAGE.DEMOTE	TD	Any LP	Split the large page into multiple small pages.



3.3.1.5. GPA Range Unblock

GPA range unblock is intended to be used when a range has been blocked, for example, for page removal, but the host VMM decides to cancel the operation. Unblock is detailed in 7.14.



5 **Figure 3.5: Typical GPA Range Unblock Sequence**

**Table 3.8: Typical GPA Range Unblock Sequence**

Phase		Intel TDX Function	Scope	Execute On	Description
TLB Tracking Sequence	1	TDH.MEM.RANGE.BLOCK (multiple)	TD	Any LP	Block private GPA range from further address translation.
	2	TDH.MEM.TRACK	TD	Any one LP	Increment the TD’s TLB epoch.
	3	N/A	TD	Multiple LPs	Send an IPI, causing TD exit on any remote LP associated with a VCPU. Subsequent TDH.VP.ENTER will flush TLB.
Unblocking	4	TDH.MEM.RANGE.UNBLOCK	TD	Any LP	Remove the private GPA range blocking.

3.3.2. Guest TD Execution

10 3.3.2.1. TD VCPU First-Time Invocation

**Table 3.9: Typical TD VCPU First-Time Invocation Sequence**

Phase		Side	Intel TDX Function	Scope	Execute On	Description
Entering TD VCPU (First Time)	1	VMM	N/A	LP	LP x	Save VMM LP state not preserved across TD Entry to TD exit.
	2	VMM	TDH.VP.ENTER	VCPU/LP	LP x	Restore initial LP state, as set by TDH.VP.INIT, from TDVPS and enter TDX non-root mode.
TD VCPU Initial Execution	TD software (VBIOS) starts execution in 32-bit protected mode with no paging.					
	3	TD	N/A	VCPU/LP	LP x	TD software parses initial information in GPR, builds page tables and switches to 64-bit mode.
	TD software (VBIOS) now executes in 64-bit mode.					
Enumeration	4	TD	TDG.VP.INFO	VCPU/LP	LP x	TD software retrieves basic TD and execution environment information.

Phase		Side	Intel TDX Function	Scope	Execute On	Description
	5	TD	TDG.MR.REPORT	VCPU/LP	LP x	TD software retrieves additional TD information.
TD continues execution in TDX non-root mode.						

### 3.3.2.2. TD VCPU Entry, Exit on TDG.VP.VMCALL and Re-Entry

Table 3.10: Typical TD Entry, Exit on TDG.VP.VMCALL and Re-Entry Sequence

Phase		Side	Intel TDX Function	Scope	Execute On	Description
TD Entry	1	VMM	N/A	LP	LP x	Save VMM LP state not preserved across TD Entry to TD exit.
	2	VMM	TDH.VP.ENTER	VCPU/LP	LP x	Restore LP state from TDVPS and enter TDX non-root mode.
	TD executes in TDX non-root mode.					
Software Protocol over TDG.VP.VMCALL	3	TD	TDG.VP.VMCALL	VCPU/LP	LP x	Exit TDX non-root mode, save LP state to TDVPS, and set synthetic state (except most GPRs and all XMMs).
	4	VMM	N/A	LP	LP x	Optionally: Restore VMM LP state saved before TDH.VP.ENTER.
	5	VMM	N/A	LP	LP x	Perform TDG.VP.VMCALL function, as determined by the TD-VMM software contract (out of the scope for this document).
	6	VMM	N/A	LP	LP x	Save VMM LP state not preserved across TD Entry to TD exit.
	7	VMM	TDH.VP.ENTER	VCPU/LP	LP x	Restore LP state from TDVPS (except most GPRs and all XMMs), and enter TDX non-root mode.
	8	TD	N/A	VCPU/LP	LP x	Parse TDG.VP.VMCALL output operands as determined by TD – VMM software contract.
TD Execution	TD continues execution in TDX non-root mode.					

### 5 3.3.2.3. TD VCPU Entry, Exit on Asynchronous Event and Re-Entry

Table 3.11: Typical TD Entry, Exit on Asynchronous Event and Re-Entry Sequence

Phase		Side	Intel TDX Function	Scope	Execute On	Description
TD Entry	1	VMM	N/A	LP	LP x	Save LP state not preserved across TD Entry to TD exit.
	2	VMM	TDH.VP.ENTER	VCPU/LP	LP x	Restore LP state from TDVPS, and enter TDX non-root mode.
	TD executes in TDX non-root mode.					

Phase		Side	Intel TDX Function	Scope	Execute On	Description
<b>Async. TD Exit and Re-Entry</b>	3	TD	N/A	VCPU/LP	LP x	Asynchronous event (interrupt, exception, EPT violation, etc.) causes TD exit. Save LP state to TDVPS, and set synthetic state.
	4	VMM	N/A	LP	LP x	Restore any required LP state saved by the VMM before TDH.VP.ENTER.
	5	VMM	N/A	LP	LP x	Handle the asynchronous event.
	6	VMM	N/A	LP	LP x	Save VMM LP state not preserved across TD Entry to TD exit.
	7	VMM	TDH.VP.ENTER	VCPU/LP	LP x	Restore LP state from TDVPS and enter TDX non-root mode.
<b>TD Execution</b>	TD continues execution in TDX non-root mode.					

3.3.2.4. Guest-Side Functions

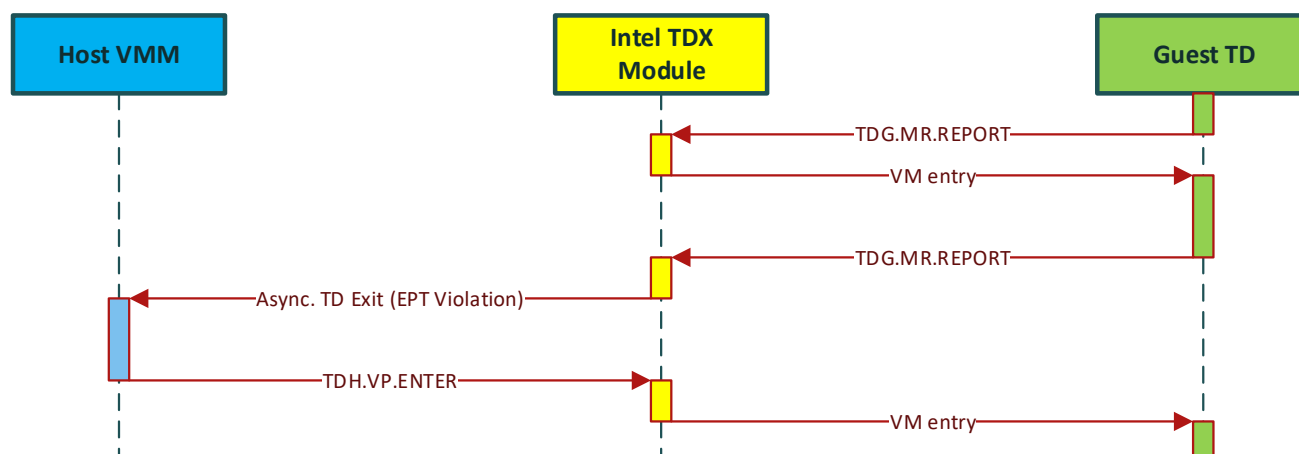


Figure 3.6: Typical Guest-Side Function Sequences

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Table 3.12: Typical Guest-Side Functions Sequences

Case		Side	Intel TDX Function	Scope	Execute On	Description
<b>Guest-Side Function Returns to Guest TD</b>	TD executes in TDX non-root mode					
	1	TD	TDG.MR.REPORT	VCPU/LP	LP x	The guest TD VM exits to the Intel TDX module, which handles the guest-side function and re-enters the TD.
	TD continues execution in TDX non-root mode					
<b>Guest-Side Function Causes Async. TD Exit</b>	2	TD	TDG.MR.REPORT	VCPU/LP	LP x	The guest TD exits to the Intel TDX module, which handles the guest-side function, but an asynchronous event (e.g., EPT violation, etc.) causes TD exit.
	3	VMM	N/A	LP	LP x	Optional: The host VMM restores the VMM LP state saved before TDH.VP.ENTER.
	4	VMM	N/A	LP	LP x	The host VMM handles the asynchronous event.

Case		Side	Intel TDX Function	Scope	Execute On	Description
	5	VMM	N/A	LP	LP x	The host VMM saves any VMM LP state not preserved across TD Entry to TD exit.
	6	VMM	TDH.VP.ENTER	VCPU/LP	LP x	The Intel TDX module restores LP state from TDVPS and enters TDX non-root mode.
TD continues execution in TDX non-root mode.						

### 3.3.2.5. TD VCPU Rescheduling (Migration to Another LP)

The Intel TDX module is designed to allow a TD VCPU to be associated with at most one LP at any time. The host VMM must explicitly break this association in order to migrate the VCPU to another LP.

5

**Table 3.13: Typical VCPU Migration to Another LP Sequence**

Phase		Intel TDX Function	Scope	Execute On	Description
<b>Old VCPU → LP Association</b>	1	Any VCPU-specific SEAMCALL leaf	VCPU	Old LP	Any VCPU-specific SEAMCALL leaf (e.g., TDH.VP.INIT, TDH.VP.ENTER, TDH.VP.RD, etc.) creates an association between the current LP and the VCPU.
<b>Breaking Old VCPU → LP Association</b>	2	TDH.VP.FLUSH	VCPU	Old LP	Break the VCPU-LP association: flush the VCPU's TD VMCS to TDVPS memory and flush the VCPU's TLB ASID.
At this point the VCPU is not associated with any LP.					
<b>New VCPU → LP Association</b>	3	Any VCPU-specific SEAMCALL leaf	VCPU	New LP	Create a new VCPU-LP association.

### 3.4. TD Destruction

The following sequence is intended to be used by the host VMM to destroy a TD and reclaim all its resources.

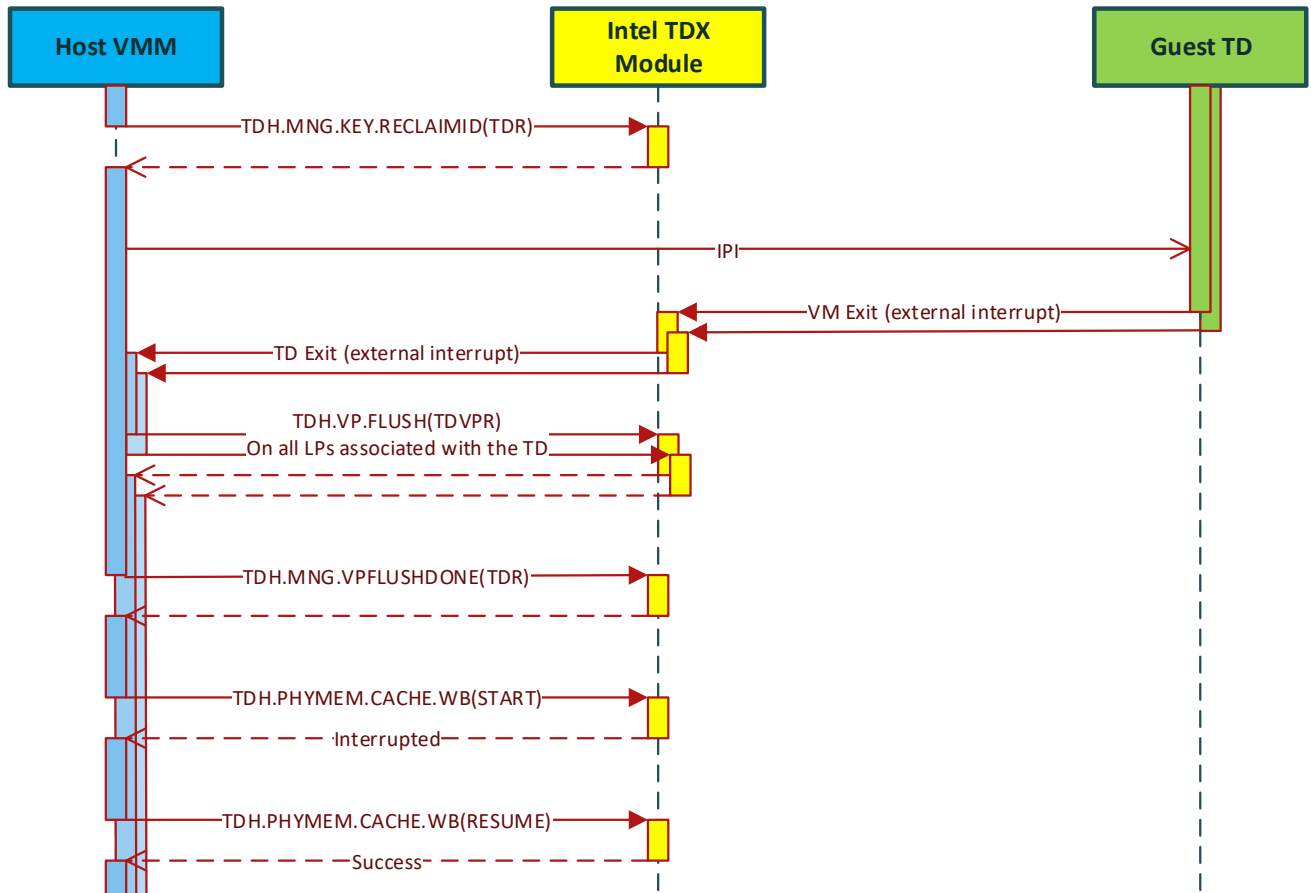


Figure 3.7: Typical TD Destruction Sequence Step A: Stopping and Flushing Out

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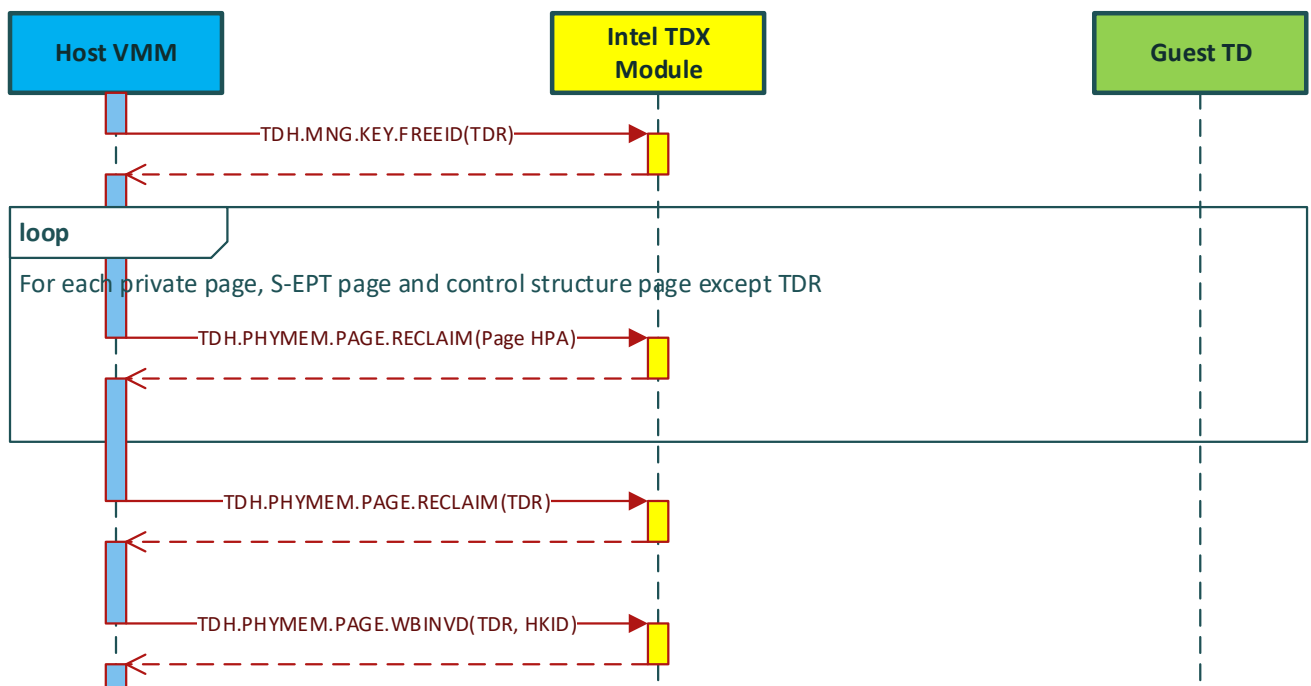


Figure 3.8: Typical TD Destruction Sequence Step B: Resource Reclamation

Table 3.14: Typical TD Destruction Sequence

	Step	Description	SEAMCALL Leaf Functions	
A	<b>TD Stopping and Flushing Out</b>	1	The host VMM selects a TD to destroy. It sends a virtual interrupt to the TD to shut down gracefully.	TDH.MNG.KEY.RECLAIMID TDH.VP.FLUSH TDH.MNG.VPFLUSHDONE TDH.PHYMEM.CACHE.WB
		2	The host VMM reclaims the TD's HKID by calling the TDH.MNG.KEY.RECLAIMID function.	
		3	The host VMM broadcasts inter-processor interrupts (IPIs) and must ensure TD exit on all logical processors.	
		4	The host VMM calls the TDH.VP.FLUSH function on all LPs associated with a TD VCPU to flush the TLBs and cached TD VMCS associated with a TD VCPU on those LPs.	
		5	The host VMM calls the TDH.MNG.VPFLUSHDONE function. It checks that above step executed for all the TD's VCPUs are associated with an LP.	
		6	The host VMM calls the TDH.PHYMEM.CACHE.WB function on each package to write back to memory the TD contents from all caches.  TDH.PHYMEM.CACHE.WB is interruptible by external events. The host VMM should restart it if it indicates it was interrupted, until successfully completed.	
		7	At this point, no address translations or cache lines may exist for this TD except for the TDR page.	
B	<b>Resource Reclamation</b>	1	The host VMM calls the TDH.MNG.KEY.FREEID function. It marks the HKID used by the TD as available for other TDs.	TDH.MNG.KEY.FREEID TDH.PHYMEM.PAGE.RECLAIM TDH.PHYMEM.PAGE.WBINVD
		2	For each physical page in TDMR allocated to the TD (TD private pages, Secure EPT pages, and control structures except TDR), the host VMM calls the TDH.PHYMEM.PAGE.RECLAIM function to mark the page as free.	
		3	The host VMM calls the TDH.PHYMEM.PAGE.RECLAIM function to mark the TDR page as free. The function checks that all other TD physical pages have been reclaimed before.	
		4	Before allocating the reclaimed TDR physical page to any use, the host VMM calls TDH.PHYMEM.PAGE.WBINVD to flush its cache lines.	

# SECTION 2: INTEL TDX MODULE ARCHITECTURE SPECIFICATION

## 4. Key Management

### 4.1. Objectives

The main goal of Intel TDX key management is to enable the VMM to perform the following:

- Manage HKID space as a limited platform resource, assigning HKIDs to TDs and reclaiming them as required.
- Enable the Intel TDX module to use a global ephemeral key for encrypting its data (e.g., PAMT).
- Enable each TD to use its own ephemeral key.

The Intel TDX interface functions are designed to provide the required building blocks and help assure that software cannot perform operations that are not compliant with TDX security objectives, as follows:

1. Help assure that only HKID values that have been configured for TDX private memory encryption keys can be assigned to TDs, and that those HKID values cannot be used by non-TD software or devices.
2. Prevent assignment of the same HKID to more than one TD.
3. At the time an HKID is assigned to a TD, there must be no modified cache lines – at any level, for any core, on any package – for that HKID. All such cache lines that may have held modified data have been written to memory (if required). Note that this requirement applies only to TDX private HKID and not to legacy MKTME HKIDs.
4. TD memory may be accessed, and the TD may run, only when the following conditions are met:
  - 4.1. An HKID has been assigned for the TD's ephemeral key.
  - 4.2. The encryption key has been configured for all the TD's ephemeral HKID, on all crypto engines, on all packages.

### 4.2. Background: HKID Space Partitioning

Since the same MKTME encryption engines and the same set of encryption keys are used for legacy MKTME operation and for TDX operation, TDX ISA enables the enumeration and partitioning of the activated HKID space between the two technologies. As designed, the encryption keys and their associated HKIDs are divided into three ranges, as shown in Table 4.1 below.

- A single key with HKID value 0 is the legacy TME key. It is used as a platform shared memory encryption key.
- A range of keys with HKID values 1 to MAX\_ACTIVATED\_MKTME\_HKIDS - 1 are used as legacy MKTME keys.
- A range of keys with HKID values MAX\_ACTIVATED\_MKTME\_HKIDS to MAX\_ACTIVATED\_HKIDS are used as TDX keys. These HKIDs are known as **private HKIDs**.

Private HKIDs and private keys are designed to be fully controlled by the Intel TDX module and are the subject of this chapter.

**Table 4.1: HKID Space Partitioning**

	HKID	Key
Shared HKIDs	0	Legacy TME key, shared
	1	Legacy MKTME key #1
	2	Legacy MKTME key #2
	...	...
	MAX_ACTIVATED_MKTME_HKIDS - 1	Last legacy MKTME key
Private HKIDs	MAX_ACTIVATED_MKTME_HKIDS	Private key of a specific TD
	MAX_ACTIVATED_MKTME_HKIDS + 1	Private key of a specific TD
	MAX_ACTIVATED_MKTME_HKIDS + 2	Private key of a specific TD
	...	...
	MAX_ACTIVATED_HKIDS - 1	Private key of a specific TD



### 4.3. Key Management Tables

The CPU and the Intel TDX module maintain several tables for key management. No table is intended to be directly accessible by software; the tables are used by the Intel TDX functions. The tables help the Intel TDX module track the proper operation of the software and help achieve the Intel TDX security objectives.

5 **Table 4.2: Key Management Tables**

Table	Scope	Description	Reference
<b>Key Encryption Table (KET)</b>	Package	<p>KET is an abstraction of the CPU micro-architectural hardware table for configuring the memory encryption engines. The KET is indexed by HKID. All crypto engines on a package are configured the same way.</p> <p>KET is part of the legacy MKTME architecture. Intel TDX ISA partitions KET to shared and private ranges, as described in 4.2 above.</p> <ul style="list-style-type: none"> <li>• A KET entry in private HKIDs range is configured per package by the host VMM using the SEAMCALL(TDH.MNG.KEY.CONFIG) function.</li> <li>• A KET entry in the shared HKID range is configured by software per package directly, using the PCONFIG instruction.</li> </ul>	
<b>KeyID Ownership Table (KOT)</b>	Platform	<p>KOT is an Intel TDX module hidden table for managing the TDX HKIDs inventory. It is used for assigning HKIDs to TDs, revoking HKIDs from TDs and controlling cache flush.</p> <p>KOT is indexed by HKID.</p>	
<b>TD Key Management Fields</b>	TD	<p>TD-scope key management fields are held in TDR. They include the key state, ephemeral private HKID and key information, and a bitmap for tracking key configuration.</p>	19.1.2

Figure 4.1 below provides an abstract, high-level picture of how the tables are related. Detailed discussion is provided in the following sections.

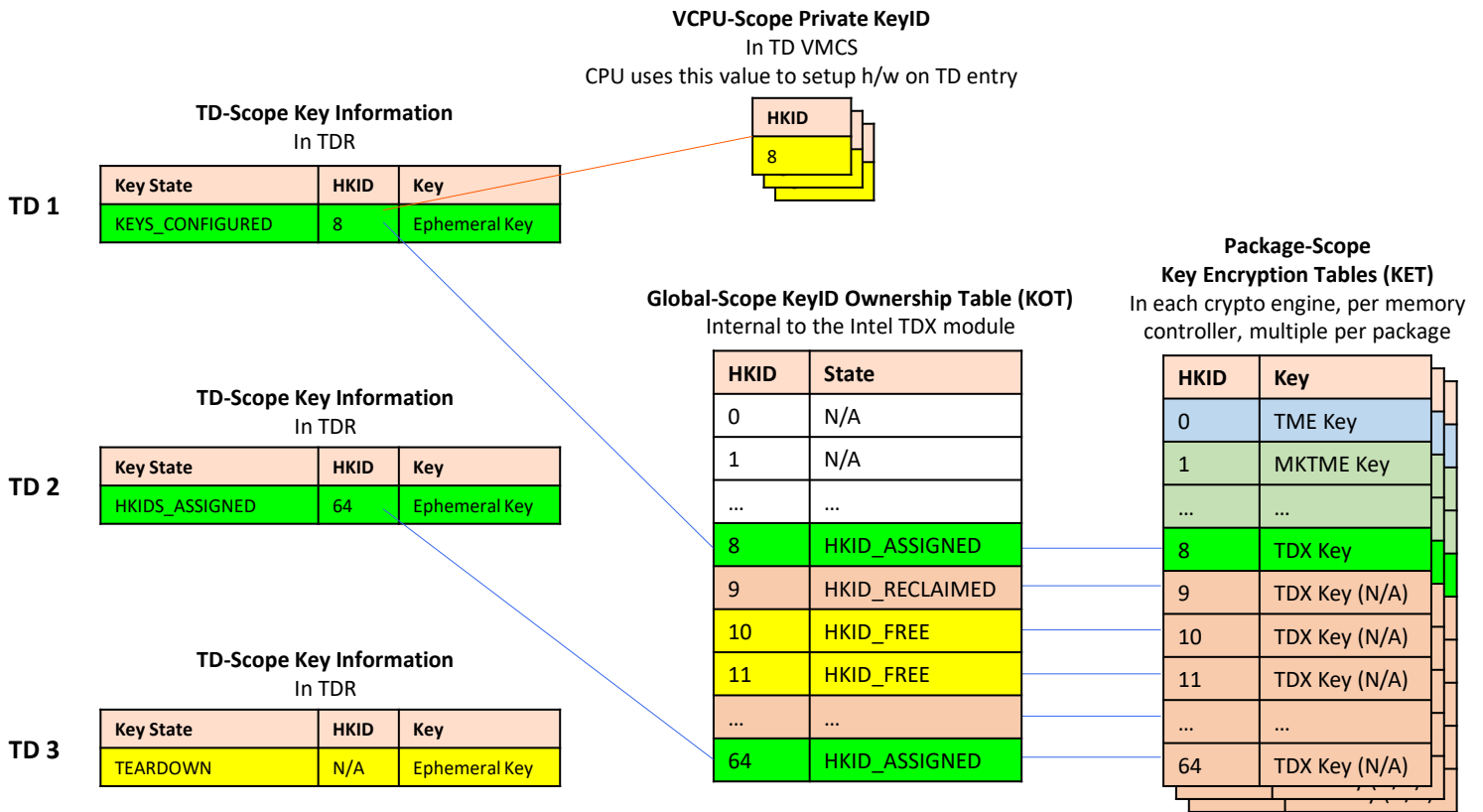


Figure 4.1: Overview of the Key Management State at TD-Scope, LP-Scope, Package-Scope and Global-Scope

#### 4.4. Combined Key Management State

Key management state is composed of two state variables:

- **Per-HKID state**, which is also the state of a JOT entry, is designed to control how the inventory of private HKIDs is managed using the KOT.
- **Per-TD state** is designed to control how TD keys are configured on the hardware and the process of shutting down a TD.

The combined key management state is intended to affect whether the TD private memory is accessible, whether its contents may be cached, whether private GPA-to-HPA address translations are allowed and whether such translations may be cached.

Table 4.3 below lists the designed combined key management state values and their meaning. Figure 4.2 below shows a simplified diagram of the combined key state. Refer also to the key management sequences described in 4.5.

Table 4.3: Combined TD Key Management States

TD Key Management State	KOT Entry (HKID) State	Private Memory Access		S-EPT Translations		Comments
		New	Cached	New	Cached	
N/A	HKID_FREE	No	No	No	No	HKID not assigned to TD
TD_HKID_ASSIGNED	HKID_ASSIGNED	No	No	No	No	TD private key not configured
TD_KEYS_CONFIGURED		TD	TD	TD	TD	TD build and execution <sup>4</sup>
TD_BLOCKED	HKID_RECLAIMED	TD	TD	No	TD	TD private memory access is blocked <sup>5</sup> , TD may not run
	HKID_FLUSHED	No	TD	No	No	TD private memory access is blocked, TD may not run
TD_TEARDOWN	N/A (HKID_FREE)	No	No	No	No	TD has no HKID
N/A	HKID_RESERVED	Global	Global	N/A	N/A	HKID for Intel TDX global data

<sup>4</sup> Sub-states of TD\_KEYS\_CONFIGURED are described in 5.4.

<sup>5</sup> TDH.VP.FLUSH may write to TD VMCS

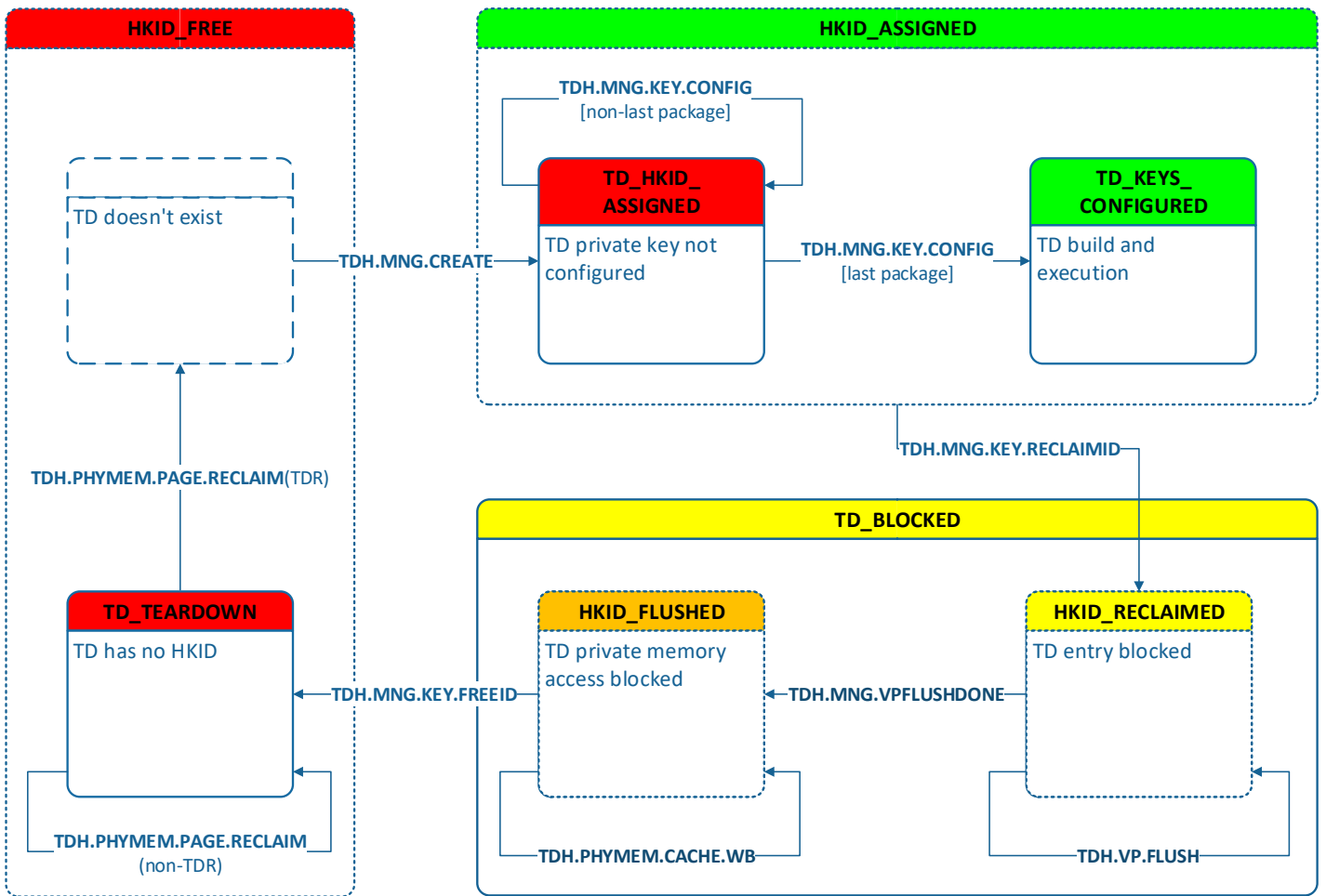


Figure 4.2: Simplified Combined TD Key Management State Diagram

See also 5.4, which zooms-in into the TD\_KEYS\_CONFIGURED state, detailing its TD build and execution sub-states.

### 4.5. Key Management Sequences

#### 5 4.5.1. Intel TDX Module Initialization: Setting an Ephemeral Key and Reserving an HKID for Intel TDX Data

This sequence is described as part of the Intel TDX module initialization sequence in 12.1.1.

#### 4.5.2. TD Creation, Keys Assignment and Configuration

This sequence is intended to be used by the host VMM to create a new TD, select HKIDs from the global pool in KOT and assign them to the TD, and configure the TD keys on the hardware.

10 Refer also to the software flow discussion in 3.2.

Table 4.4: Typical TD Creation, Keys Assignment and Configuration (TD-Scope and KOT-Scope) Sequence

	Intel TDX Function	Scope	Execute On	Description
1	TDH.MNG.CREATE	TD	One LP	Assign the TD's private HKID.
2	TDH.MNG.KEY.CONFIG	TD	Each package and each TD key	Configure the TD's random ephemeral key on the package.

### 4.5.3. TD Keys Reclamation, TLB and Cache Flush

This sequence is intended to be used by the host VMM to reclaim the HKIDs assigned to a TD and return them to the global pool in KOT. At the end of this sequence, the HKIDs should be free to be assigned to another TD.

5 The cache flush operation is long. Since it is designed to run at global scope and is decoupled from any TD, the host VMM may choose to implement it in a lazy fashion, i.e., wait until a certain number of HKIDs in the KOT pool become RECLAIMED. This is especially important since TDH.PHYMEM.CACHE.WB operates on all cache lines regardless of HKID.

To avoid long latencies, TDH.PHYMEM.CACHE.WB is designed to be interruptible. The host VMM is expected to repeat the execution of this instruction until it returns a success indication.

Refer also to the software flow discussion in 3.4.

10 **Table 4.5: Typical TD Keys Reclamation, TLB and Cache Flush (TD-Scope and KOT-Scope) Sequence**

	Intel TDX Function	Scope	Execute On	Description
As a preparation, the host VMM avoids any VCPU-specific SEAMCALL function (i.e., TDH.VP.ENTER, TDH.VP.INIT, TDH.VP.RD and TDH.VP.WR) and waits until no VCPU is running.				
1	TDH.MNG.KEY.RECLAIMID	TD, KOT	One LP	Reclaim the TD's HKIDs, and mark the as RECLAIMED in the KOT.
2	TDH.VP.FLUSH	TD VCPU	One each LP associated with a TD VCPU	Flush the VCPU's TD VMCS to TDVPS memory, and flush the VCPU's TLB ASID.
3	TDH.MNG.VPFLUSHDONE	TD, KOT	One LP	Check all the VCPUs have been flushed.
4	TDH.PHYMEM.CACHE.WB	KOT	Each package or core <sup>6</sup>	Write back cache hierarchy, at least for the HKIDs marked as TLB_FLUSHED. The instruction execution time is long; it is interruptible by external events and may be restarted until completed.
5	TDH.MNG.KEY.FREEID	TD, KOT	One LP	Mark all the TD's RECLAIMED HKIDs as FREE.

<sup>6</sup> Enumerated by CPU during Intel TDX module initialization, see 12.1.3.3.

## 5. Guest TD Control Structures & Life Cycle

This chapter discusses the guest TD control structures and how they are intended to be used during the TD life cycle.

### 5.1. Overview

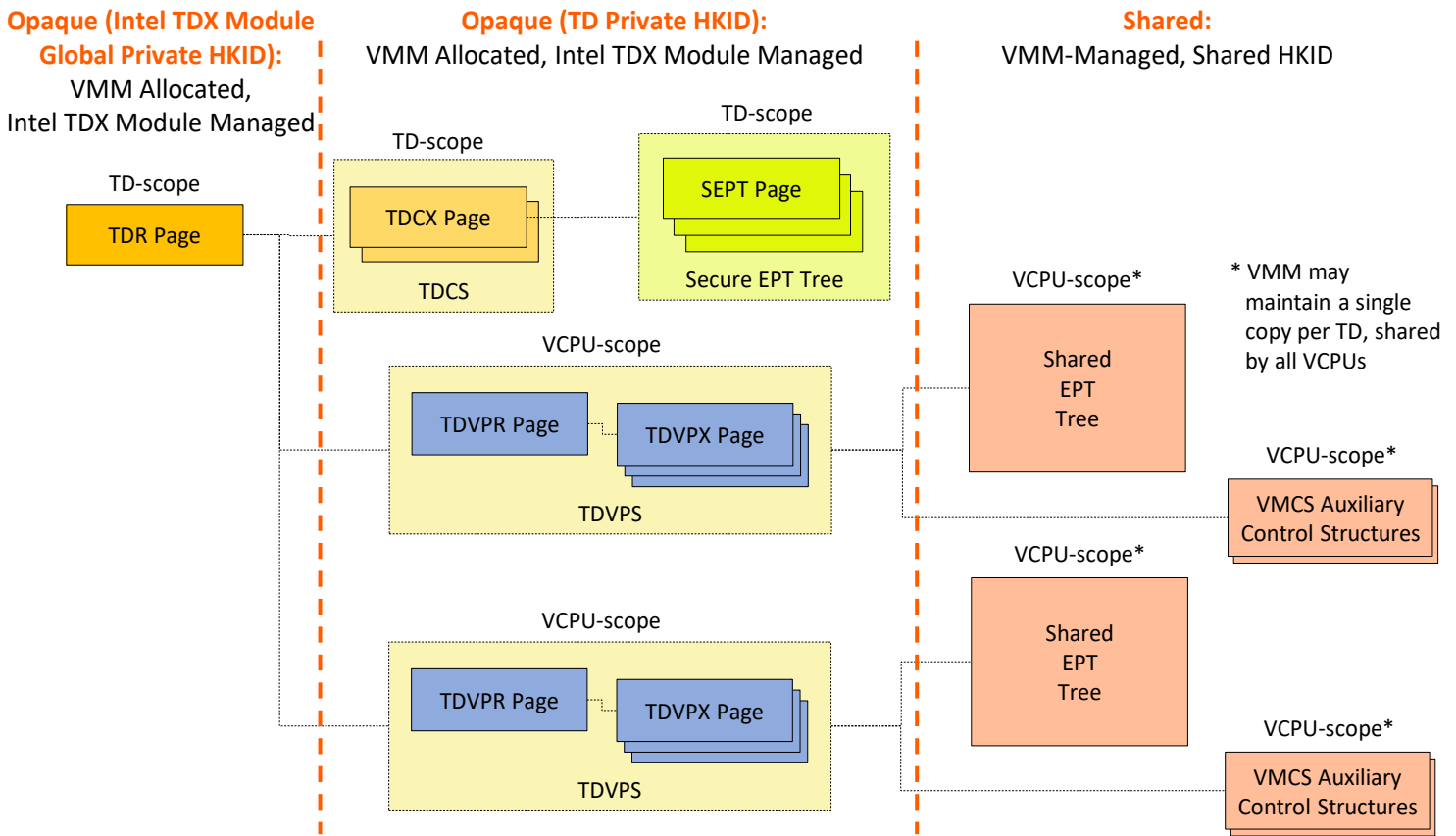


Figure 5.1: Guest TD Control Structures Overview

All guest TD control structures reside in memory pages that are allocated by the host VMM from the pre-configured TDMRs. Guest TD control structure pages are addressable by the host VMM.

#### 5.1.1. Opaque vs. Shared Control Structures

Control structures are divided to two classes:

- **Shared control structures** are intended to be directly managed by the host VMM and are encrypted with a shared HKID. The Intel TDX module architecture only describes the shared control structures that might directly impact its operation. The host VMM may hold additional control structures.
- **Opaque control structures** are not intended to be directly accessible to any software (except the Intel TDX module) or DMA. They are intended to be managed via Intel TDX module functions. Generally speaking, the host VMM is not aware of the exact format of opaque control structures. Opaque control structures' memory pages are intended to be encrypted with a private HKID.

#### 5.1.2. Scope of Control Structures

Guest TD control structures have two possible scopes:

- **TD-scope control structures** are intended to apply for a guest TD as a whole.
- **TD VCPU-scope control structures** are intended to apply for a single virtual CPU of a guest TD.

### 5.2. TD-Scope Control Structures and Management Functions

TD-scope control structures include TDR and TDCS, discussed below, and Secure EPT, discussed in Chapter 7.

### 5.2.1. TDR (Trust Domain Root)

TDR is the root control structure of a guest TD. As designed, TDR is encrypted using the Intel TDX global private HKID. It holds a minimal set of state variables that enable guest TD control even during times when the TD's private HKID is not known, or when the TD's key management state does not permit access to memory encrypted using the TD's private key.

- 5 TDR occupies a single 4KB naturally aligned page of memory. It is designed to be the first TD page to be allocated and the last to be removed. Its physical address serves as a unique identifier of the TD, as long as any TD page or control structure resides in memory.

At a high level, TDR holds the following information:

- Fields designed to control guest TD build and teardown process.
- 10 • Fields designed to manage memory encryption keys.

### 5.2.2. TDCS (Trust Domain Control Structure)

TDCS is the main control structure of a guest TD. As designed, TDCS is encrypted using the guest TD's ephemeral private key. TDCS is a multi-page logical structure composed of multiple TDCX physical pages.

At a high level, TDCS holds the following information:

- 15 • Fields designed to control the TD operation as a whole (e.g., a counter of the number of VCPUs currently running).
- Fields designed to control the TD's execution control (debuggability, CPU features available to the TD, etc.).
- Fields related to TD measurement.
- EPTP: as designed, a pointer (HPA) to the TD's secure EPT root page and EPT attributes.
- MSR bitmaps, designed to be used by all the TD's VCPUs.
- 20 • As designed, the secure EPT root page.
- A page filled with zeros, designed to be used in cases where the Intel TDX module needs a read-only constant-0 page encrypted with the TD's private key.

## 5.3. TD VCPU-Scope Control Structures and Management Functions

### 5.3.1. Trust Domain Virtual Processor State (TDVPS)

- 25 Trust Domain Virtual Processor State (TDVPS) is the root control structure of a TD VCPU. It helps the Intel TDX module control the operation of the VCPU, and holds the VCPU state while the VCPU is not running. TDVPS is a single logical control structure composed of multiple physical 4KB pages.

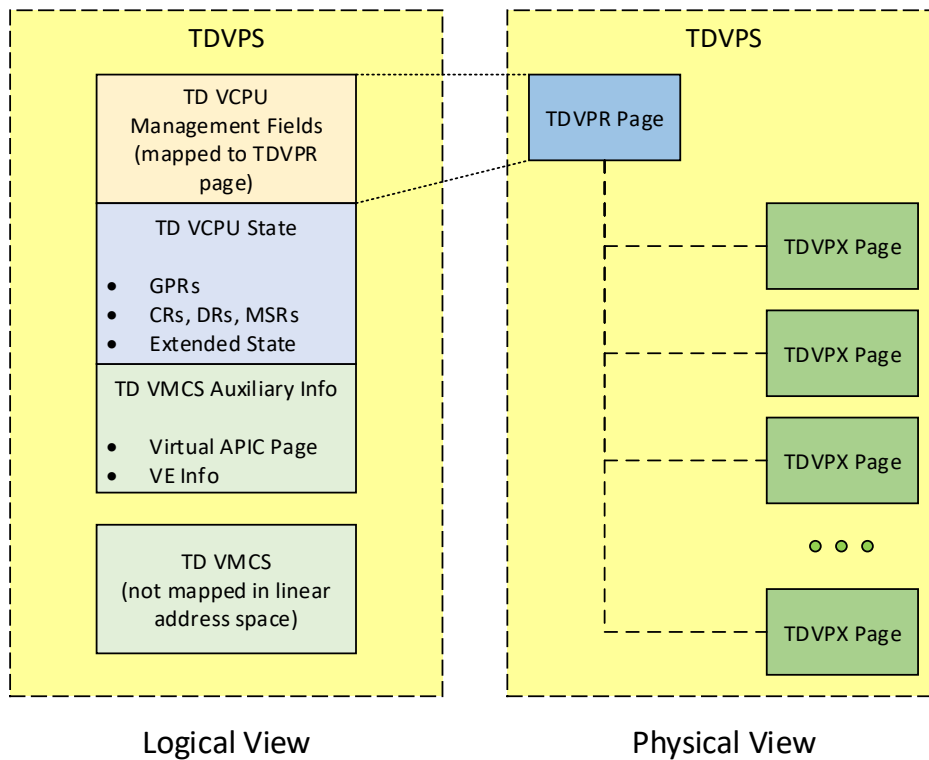


Figure 5.2: High Level Logical and Physical View of TDVPS

5.3.1.1. Physical View of TDVPS: TDVPR/TDVPX

TDVPS is designed to be opaque to software and DMA access, accessible only by using the Intel TDX module functions. From the VMM perspective, TDVPS is composed of multiple 4KB pages, where each page may reside in arbitrary locations in convertible memory.

**Trust Domain Virtual Processor Root (TDVPR)** is the 4KB root page of TDVPS. Its physical address serves as a unique identifier of the VCPU (as long as it resides in memory).

**Trust Domain Virtual Processor eXtension (TDVPX)** 4KB pages extend TDVPR to help provide enough physical space for the logical TDVPS structure.

The TDVPR and TDVPX pages are designed to be encrypted with the TD’s ephemeral private key. They are addressable by the host VMM, which is responsible for allocating memory to hold them.

The required number of 4KB TDVPR/TDVPX pages in TDVPS is enumerated to the VMM by the TDH.SYS.INFO function (see 12.2.3).

5.3.1.2. Logical View of TDVPS

Logically, TDVPS is organized as a single large data structure. At a high level, it is composed of the following parts:

**VMX (with TDX ISA Extensions) Standard Control Structures**

- TD VMCS
- TD VMCS auxiliary structures, such as virtual APIC page, virtualization exception information, etc. Note that MSR bitmaps are held as part of TDCS because they are meant to have the same value for all VCPUs of the same TD.

The TDX design does not require some of the VMX control structures (notably, the Shared EPT) to be protected. They are described below.

**Proprietary Fields**

- TD VCPU Management fields designed to manage the operation of the VCPU
- TD VCPU State fields designed to hold most of the VPCU state (except state that is saved to the TD VMCS) when the VCPU is not running

TDVPS organization and format are detailed in 19.2.



5.3.2. Non-Protected Control Structures: Shared EPT and VMCS Auxiliary Control Structures

Several VMX control structures are directly managed and accessed by the host VMM. These control structures are pointed to by fields in the TD VMCS. The Intel TDX module checks that the pointers conform to the shared-access HPA semantics (see 15.2.1.1).

5 Non-protected control structures include:

- Shared EPT tree
- Posted interrupt descriptor

5.3.3. VMM Access to TDVPS Fields

10 The **TDH.VP.RD** and **TDH.VP.WR** functions enable host VMM access to selected TDVPS fields. The Intel TDX module is designed to control which field can be read or written (down to the bit level, if required), depending on whether it is a production TD or a debug TD.

TDH.VP.RD and TDH.VP.WR are detailed in 20.2.43 and 20.2.44, respectively. Field codes are defined in 18.7.3.

5.4. TD Life Cycle

15 Figure 5.3 below shows a state diagram of the TD life cycle. Note that this diagram is a zoom-in on the relevant part of the key management state diagram in Figure 4.2.

TD build and destruction use cases are discussed in 3.2 and 3.4, respectively.

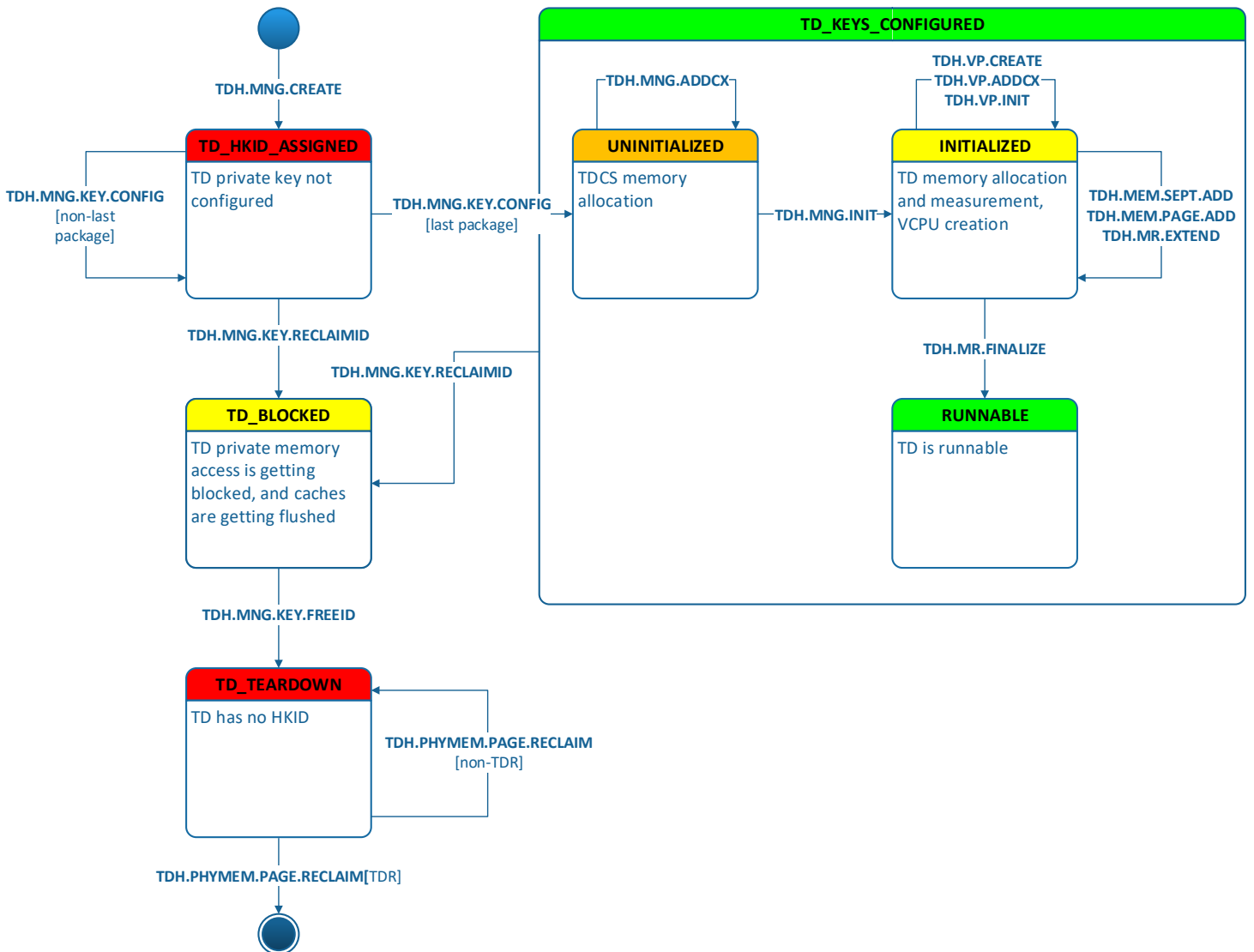


Figure 5.3: High-Level TD Life Cycle State Diagram

### 5.4.1. TD Creation Sequence

The following sequence is intended to be used by the host VMM to create a new TD. Note that only the general aspects of TD creation are described here. Other aspects, such as key management, are described in other chapters.

Refer also to the software flow discussion in 3.2.

5 **Table 5.1: Typical TD Creation Sequence**

	Intel TDX Function	Inputs	Description
1	N/A	N/A	If any MODIFIED cache lines may exist for the physical pages to be written below (TDR, TDCS, Secure EPT root page), flush them to memory using, e.g., CLFLUSH (possibly on multiple LPs). This is required to avoid corruption due to cache line aliasing.
2	TDH.MNG.CREATE	TDR page PA	Create the TDR and generate the TD's random ephemeral key.
3	Multiple	See 4.5.2	Assign an HKID, and configure the TD's random ephemeral key on all packages, as described in 4.5.2.
4	TDH.MNG.ADDCX (multiple)	<ul style="list-style-type: none"> <li>Owner TDR PA</li> <li>TDCX page PA</li> </ul>	Run multiple times to add the required number of TDCX pages.
5	TDH.MNG.INIT	<ul style="list-style-type: none"> <li>Owner TDR PA</li> <li>TD initialization parameters</li> </ul>	Initialize the TD state in TDR and TDCS.

At this point the TD is initialized. Private memory pages can be added as described in Chapter 7. VCPUs can be created and initialized as described below.

### 5.4.2. VCPU Creation and Initialization Sequence

VCPU creation and initialization is only allowed during TD build time.

The following sequence is intended to be used by the host VMM to create a new TD VCPU. After this sequence is done, the TD VCPU may be entered on an LP (assuming other conditions are met).

Refer also to the software flow discussion in 3.2.

10 **Table 5.2: Typical TD VCPU Creation and Initialization Sequence**

	Intel TDX Function	Inputs	Description
1	N/A	N/A	If any MODIFIED cache lines may exist for the physical pages to be written below (TDVPR, TDVPX), flush them to memory (e.g., using CLFLUSH – possibly on multiple LPs). This is required to avoid corruption from cache line aliasing.
2	TDH.VP.CREATE	<ul style="list-style-type: none"> <li>TDVPR page PA</li> <li>Owner TDR PA</li> </ul>	Create the VCPU and its TDVPR page.
3	TDH.VP.ADDCX (multiple)	<ul style="list-style-type: none"> <li>TDVPX page PA</li> <li>Parent TDVPR PA</li> </ul>	Run multiple times to add the required number of TDVPX pages as an extension to a parent TDVPR.
4	TDH.VP.INIT	<ul style="list-style-type: none"> <li>TDVPR PA</li> <li>VMM-provided identifier</li> </ul>	Initialize the VCPU state.

	Intel TDX Function	Inputs	Description
5	TDH.VP.WR	<ul style="list-style-type: none"> <li>• TDVPR page PA</li> <li>• Field code</li> <li>• New field value</li> <li>• Write mask</li> </ul>	<p>The host VMM typically writes one or more of the following TD VCPU's VMCS controls:</p> <ul style="list-style-type: none"> <li>• Shared EPTP</li> <li>• Posted-interrupts descriptor address, posted-interrupts notification vector and process posted interrupt</li> <li>• bus-lock detection</li> <li>• notification exiting and notify window</li> </ul> <p>For details, see 19.2.4.</p>

### 5.4.3. TD Teardown Sequence

The following sequence is intended to be used by the host VMM to tear down a TD. Note that only the general aspects of TD teardown are described here. Other aspects, such as key management, are described in other chapters. See also the discussion of physical page reclamation in 6.5.

Refer also to the software flow discussion in 3.4.

**Table 5.3: Typical TD Teardown Sequence**

	Intel TDX Function	Inputs	Description
1	Multiple	See 4.5.3	Reclaim the HKID, and flush TLB and cache, as described in 4.5.3.
2	TDH.PHYMEM.PAGE.RECLAIM (multiple)	TD page or control structure PA	Remove all TD private pages and control structure pages, and mark them as PT_NDA in the PAMT.
3	TDH.PHYMEM.PAGE.RECLAIM	TDR PA	Remove the TDR page, and mark it as PT_NDA in the PAMT.
4	TDH.PHYMEM.PAGE.WBINVD	TDR PA	Flush MODIFIED cache lines: this is required to avoid corruption due to cache line aliasing. Note that all cache lines for all other TD pages must have been flushed before the TDR page was reclaimed.

## 5.5. Concurrency Restrictions and Enforcement

10 A general description of concurrency restriction is provided in 15.1.

Normally, exclusive or shared access is acquired, if needed, for the typically short duration of function flows. A TD VCPU execution is an exception case. Shared access to TDCS and TDVPS is acquired on TD Entry and released on TD Exit. This implies that SEAMCALL(TDH.VP.ENTER) function, all TDCALL functions, and asynchronous TD Exit have implicit shared access to TDCS and TDVPS.

15 This mechanism helps protect running VCPUs against concurrent functions that may try to change their governing control structures.

## 6. Physical Memory Management

This chapter describes how the Intel TDX module manages memory as a set of physical pages.

### 6.1. Trust Domain Memory Regions (TDMRs) and Physical Address Metadata Tables (PAMTs)

**Trust Domain Memory Region (TDMR)** is defined as a range of convertible memory pages. TDMRs are set by the host VMM, based on the CMR information previously checked by MCHECK.

Each TDMR is defined as controlled by a (logically) single **Physical Address Metadata Table (PAMT)**. The PAMT structure is discussed in 6.3 below. PAMT tables reside in VMM-allocated memory, and they are designed to be encrypted with the Intel TDX global private HKID. The required size of PAMT memory, as a function of TDMR size, is enumerated to the VMM by TDH.SYS.INFO.

Typically, after the host VMM initializes the Intel TDX module (TDH.SYS.INIT and TDH.SYS.LP.INIT), it configures the TDMRs and their respective PAMTs using TDH.SYS.CONFIG. It then would gradually initialize the TDMRs using TDH.SYS.TDMR.INIT. For a detailed description of the typical Intel TDX module initialization and configuration sequence, see Chapter 12.

### 6.2. TDMR Details

The following list includes definitions of the characteristics of a TDMR:

- TDMR configuration is "soft" – no hardware range registers are used.
- Each TDMR defines a single physical address range.
- Each TDMR has its own size which must be a multiple of 1GB. TDMR size is **not** required to be a power of two.
- A TDMR must be aligned on 1GB.
- TDMRs cannot overlap with each other.
- TDMRs may contain reserved areas. This effectively allows the host VMM to flexibly configure TDMRs based on the VMM's own consideration of system memory allocation – without being impacted by the 1GB granularity of the TDMR size.
  - A reserved area must be aligned on 4KB, and its size must be a multiple of 4KB.
  - The number of reserved areas that may be configured per TDMR is enumerated by TDH.SYS.INFO.
- TDMR memory, except for reserved areas, must be convertible as checked by MCHECK (i.e., every TDMR page must reside within a CMR).
- There is no requirement for TMDRs to cover all CMRs.
- TDMRs are configured at platform scope (no separate configuration per package).
- The maximum number of TDMRs is Intel TDX module implementation specific. It is enumerated to the host VMM using the SEAMCALL(TDH.SYS.INFO) function, as described below.

### 6.3. PAMT Details

The Physical Address Metadata Table (PAMT) is designed to track the metadata of every physical page in TDMR. A page metadata include page type, page size, assignment to a TD, and other attributes.

The PAMT is used by the Intel TDX module to help enforce the following properties:

<b>Page Attributes</b>	A physical page in TDMR has a well-defined set of attributes, such as page type and page size.
<b>Single TD Assignment</b>	A physical page in TDMR can be assigned to at most one TD.
<b>Secure EPT Consistency</b>	The page size of any private TD page, mapped in Secure EPT, matches its page size attribute in PAMT.

#### 6.3.1. PAMT Entry

**Note:** The description below is provided at a high level. Implementation details may differ.

A PAMT entry is designed to hold metadata for a single physical page. The page size may be 4KB, 2MB or 1GB depending on the PAMT level (see 6.3.2 below).

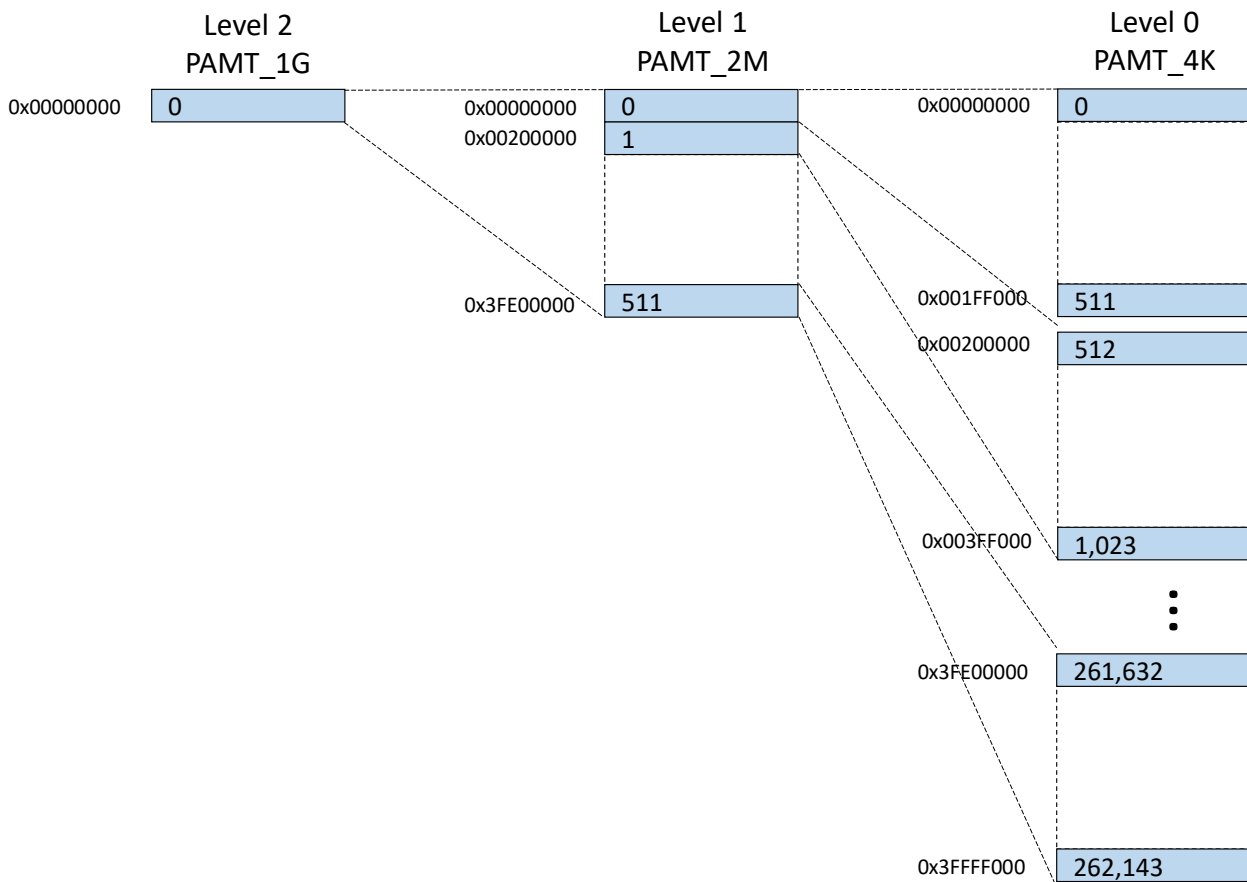
**Table 6.1: High-Level View of a PAMT Entry**

Field	Description
<b>PT</b>	PT indicates the type of page intended to be associated with this PAMT entry. See Table 6.3 below for details.
<b>OWNER</b>	OWNER is designed to contain bits 51:12 of the physical address of the TD's TDR page. This field can be applicable in all cases when a page is assigned to the Intel TDX module at this PAMT level or at a higher level. See Table 6.3 below for details.
<b>BEPOCH</b>	By design, the value of TDCS.TD_EPOCH as sampled by TDH.MEM.RANGE.BLOCK This field is intended to be applicable only if PT is PT_REG or PT_EPT. See 7.6 for a detailed discussion.

**6.3.2. PAMT Blocks and PAMT Arrays**

For each 1GB of TDMR physical memory, there is a corresponding **PAMT Block**. A PAMT Block is **logically** arranged in a three-level tree structure of **PAMT Entries**, as shown in Figure 6.1 below. Levels 0 through 2 (PAMT\_4K, PAMT\_2M and PAMT\_1G) correspond to 4KB, 2MB and 1GB physical TDMR pages, respectively.

Physically, for each TDMR the design includes three arrays of PAMT entries, one for each PAMT level. This aims to simplify VMM memory allocation. A logical PAMT Block has one entry from the PAMT\_1G array, 512 entries from the PAMT\_2M array, and 512<sup>2</sup> entries from the PAMT\_4K array.



**Figure 6.1: Typical Example of a PAMT Block Hierarchy for a 1GB TDMR Block**

10

### 6.3.3. PAMT Hierarchy and Page Types

Table 6.2 below describes the PAMT page types:

**Table 6.2: PAMT Page Types**

Page Type	PAMT Level	Associated TDX Page	Description
PT_NDA	Any	Depending on PT at higher PAMT level, if any	The physical page is <b>Not Directly Assigned</b> to the Intel TDX module at this size (4K, 2M or 1G) and PAMT level. This page may be part of a larger page that is assigned to the Intel TDX module at a higher level, or this page may contain smaller pages that are assigned to the Intel TDX module at lower levels. See Table 6.3 below for details.
PT_RSVD	PAMT_4K	None	The physical page is reserved for non-TDX usage. The Intel TDX module will not allow converting this page to any other page type. The page can be used by the host VMM for any purpose. PT_RSVD is used for implementing reserved areas within TDMRs. See 12.1.4.2.1 for details.
PT_REG	Any	TD private page	The physical page at this PAMT level (4K, 2M or 1G) holds TD private memory and is mapped in the guest TD GPA space by the Secure EPT.
PT_TDR	PAMT_4K	TDR	TDR control structure page
PT_TDCX	PAMT_4K	TDCX	One physical page of the multi-page TDCS control structure
PT_TDVPR	PAMT_4K	TDVPR	Root page of the multi-page TDVPS control structure
PT_TDVPX	PAMT_4K	TDVPX	Non-root page of the multi-page TDVPS control structure
PT_EPT	PAMT_4K	Secure EPT	Secure EPT page

- 5 Table 6.3 below shows the page type (PT) of PAMT entries at the three levels of hierarchy, depending on whether the page is assigned to the Intel TDX module manages the page, whether the page is mapped in secure EPT, and the mapping size.

**Table 6.3: PAMT Hierarchy and Page Types**

Intel TDX Module Management			PAMT Entry Page Type		
Assigned to TDX?	Physical Page Size	GPA Mapping Size (Secure EPT Level)	PAMT_1G (Level 2)	PAMT_2M (Level 1)	PAMT_4K (Level 0)
No	4KB	N/A	PT_NDA	PT_NDA	PT_RSVD
No	4KB	N/A	PT_NDA	PT_NDA	PT_NDA
Yes	4KB	None	PT_NDA	PT_NDA	PT_TDR, PT_TDCX, PT_TDVPR, PT_TDVPX, PT_EPT
Yes	4KB	4KB (Level 0)	PT_NDA	PT_NDA	PT_REG
Yes	2MB	2MB (Level 1)	PT_NDA	PT_REG	PT_NDA
Yes	1GB	1GB (Level 2)	PT_REG	PT_NDA	PT_NDA

Note the following:

- A 4KB page is considered **free** (i.e., not assigned to TDX) if its PAMT.PT at all three PAMT levels is PT\_NDA. Any function that attempts to assign an HPA to TDX (e.g., TDH.MEM.PAGE.ADD) is designed to check this.
- In all other cases, PAMT.PT is different than PT\_NDA in only one of the three PAMT levels.
- When a page is mapped by Secure EPT at 4KB, 2MB or 1GB GPA mapping size, it is managed by the Intel TDX module as a physical page of the same size. Secure EPT is described in Chapter 7.
- PT\_RSVD pages cannot be used by the Intel TDX module. They are used for implementing reserved areas within TDMRs. See 12.1.4.2.1 for details.

## 6.4. Adding Physical Pages

### 6.4.1. Preventing Cache Line Aliasing

Before adding a physical page, the host VMM is responsible for making sure no MODIFIED cache lines exist for that page. The host VMM can flush cache lines to memory – e.g., using CLFLUSH (only for pages containing data encrypted with a shared HKID – the VMM cannot directly use an HPA with a private HKID), or TDH.PHYMEM.PAGE.WBINVD (for pages containing data encrypted with any HKID, as long as the page is within a TDMR). Flushing cache lines to memory is required to avoid corruption due to cache line aliasing.

### 6.4.2. Adding Pages not Mapped to the Guest TD

By design, TD control structure pages TDR, TDCX, TDVPR and TDVPX are not mapped to the guest TD's GPA space, and they are only managed using their HPA. The functions TDH.MNG.CREATE, TDH.MNG.ADDCX, TDH.VP.CREATE and TDH.VP.ADDCX are designed to add 4KB control structure pages PT\_TDR, PT\_TDCX, PT\_TDVPR and PT\_TDVPX, respectively. The overall process is described in 5.4.1 and 5.4.2.

### 6.4.3. Adding Pages and Mapping to the Guest TD's GPA

The following page types are associated with a guest TD's GPA:

- Guest TD private pages
- Secure EPT pages are mapped to the guest TD's GPA space.

Those pages are added given their HPA and the required GPA. The functions TDH.MEM.PAGE.ADD and TDH.MEM.PAGE.AUG add a 4KB PT\_REG page, and the functions TDH.MEM.SEPT.ADD and TDH.MEM.PAGE.DEMOTE add a 4KB PT\_EPT page. TD private memory management functions are described in Chapter 7. This section describes only their physical page management aspects.

## 6.5. Reclaiming Physical Pages

### 6.5.1. Reclaiming Pages not Mapped to the Guest TD

There are two cases where pages are not considered as mapped to the guest TD:

- Control structure pages are not mapped to the guest TD.
- In TD\_TEARDOWN state, as described below, no mapping is in effect.

### 6.5.2. Reclaiming TD Pages in TD\_TEARDOWN State

As part of the TD teardown process, the VMM needs to put the TD into a TD\_TEARDOWN state, as described in 5.4.2. This is a non-recoverable state where TD keys have been reclaimed, all address translations and caches have been flushed, and the TD private memory and control structures (except TDR) are no longer accessible.

By design, in the TD\_TEARDOWN state, all TD pages are effectively unmapped. Secure EPT is not accessible, and no GPA-to-HPA mapping can be used. The host VMM must treat all the TD private pages and control structure pages as physical memory and reclaim them using the TDH.PHYMEM.PAGE.RECLAIM function in any order, as long as the TDR page is the last one to be reclaimed.

For TDR page, the intention is for the host VMM to call TDH.PHYMEM.PAGE.WBINVD after calling TDH.PHYMEM.PAGE.RECLAIM. This is required to avoid corruption due to cache line aliasing because the TDR page has still been accessed and modified, even when the TD was in TD\_TEARDOWN state.

### 6.5.3. Reclaiming Physical Pages as Part of TD Private Memory Management

Functions such as TDH.MEM.PAGE.REMOVE and TDH.MEM.PAGE.PROMOTE are designed to remove TD private pages and Secure EPT pages, respectively. By design, they first make sure the pages are no longer accessible using a GPA, then they mark the physical page as free. This is described in Chapter 7; this section only highlights the physical page reclamation.

5



## 7. TD Private Memory Management

This chapter described how the Intel TDX module helps manage TD private memory and guest-physical address (GPA) translation.

### 7.1. Overview

- 5 Intel TDX ISA introduced the concept of private GPA vs. shared GPA, depending on the GPA.SHARED bit. In SEAM non-root mode, the controlling VMCS has two EPT pointer fields:
- The legacy EPT pointer is used for translating the guest TD’s memory accesses using a private GPA (i.e., GPA.SHARED == 0).
  - A new Shared EPT pointer is used for translating the guest TD’s memory accesses using shared GPAs (i.e., GPA.SHARED == 1).
- 10

A new GPAW execution control determines the position of the SHARED bit in the GPA, and a new HKID execution control defines the HKID used for accessing TD private memory.

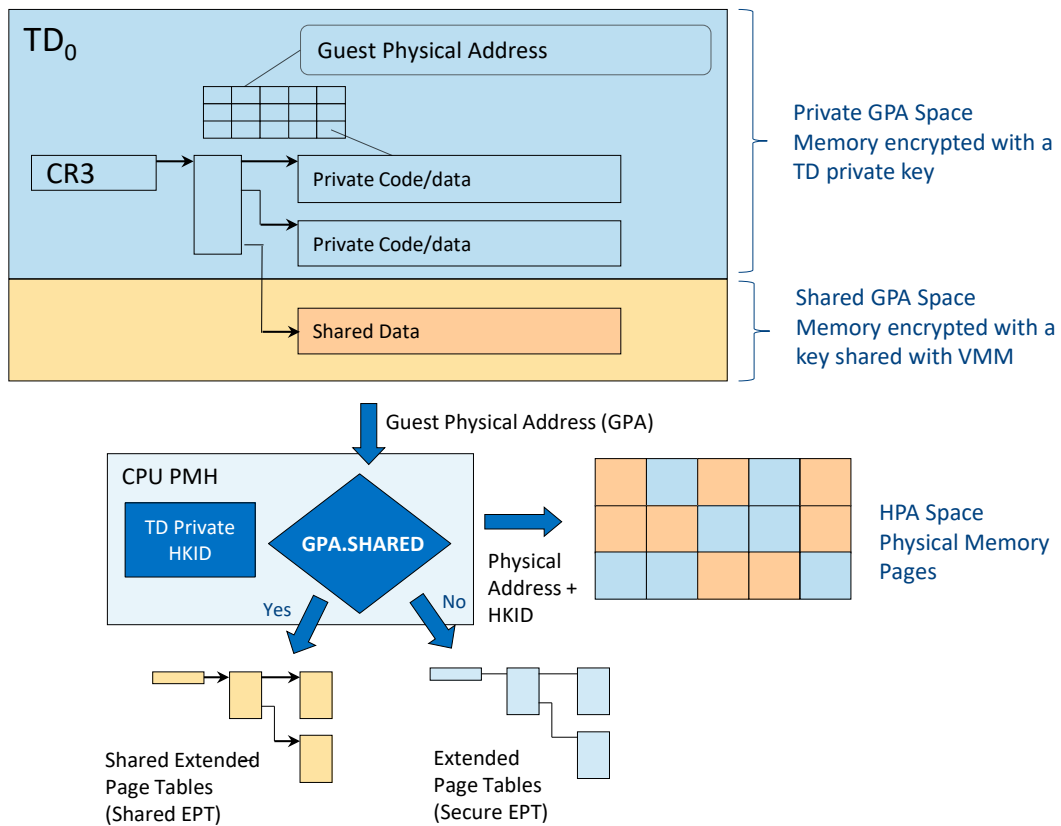


Figure 7.1: Secure EPT Concept

- 15 The Intel TDX module maintains a single Secure EPT structure per TD. Secure EPT pages are designed to be opaque; they reside in ordinary memory, and they are encrypted and integrity-protected with the TD’s ephemeral private key. The Intel TDX module does not map Secure EPT pages to the guest TD GPA space. Thus, Secure EPT is effectively not accessible by any software besides the Intel TDX module, nor by any devices. Any such access using shared HKID to Secure EPT can lead to data corruption that triggers integrity check failure leading to a machine check fault.
- 20 Secure EPT is intended to be managed indirectly by the host VMM using Intel TDX functions. The Intel TDX module helps ensure that the Secure EPT is managed correctly.

The CPU translates shared GPAs using the Shared EPT which resides in host VMM memory. The translation uses a shared HKID, and it is directly managed by the host VMM, just as with legacy VMX.

## 7.2. Secure EPT Entry

From the CPU perspective, Secure EPT has the same structure as a legacy VMX EPT. To encode additional entry state, the Intel TDX module is designed to use two of the entry bits which are defined as available to software (not used by the CPU) when the entry is non-present. For a detailed definition of the Secure EPT structure, see 18.4.

- 5 Secure EPT entry is opaque; the host VMM may not access it directly. Most of the entry bits do not contain secrets. They are readable by the host VMM using the TDH.MEM.SEPT.RD function. When the entry state is SEPT\_FREE, its address bits (51:12) are available for use as a scratchpad by the host VMM using the TDH.MEM.SEPT.WR and TDH.MEM.SEPT.RD functions.

**Table 7.1: Secure EPT Entry State High Level Description**

Secure EPT Entry State	Present (RWX != 0)	Mapped (HPA Valid)	Description
SEPT_FREE	No	No	Secure EPT entry does not map a GPA range. Most of the entry is available for use by the host VMM.
SEPT_PRESENT	Yes	Yes	Secure EPT entry maps a private GPA range which is accessible by the guest TD.
SEPT_BLOCKED	No	Yes	Secure EPT entry maps a private GPA range, but new address translations to that range are blocked.
SEPT_PENDING	No	Yes	Secure EPT entry maps a 4KB page that has been dynamically added to the guest TD using TDH.MEM.PAGE.AUG and is pending acceptance by the guest TD using TDG.MEM.PAGE.ACCEPT. This page is not yet accessible by the guest TD.
SEPT_PENDING_BLOCKED	No	Yes	Secure EPT entry is both pending and blocked.

10

## 7.3. EPT Walk

Host-side (SEAMCALL) Intel TDX functions that manage TD private memory usually accept GPA and Level parameters. They perform a Secure EPT walk which locates the target Secure EPT entry.

- 15 If the Secure EPT walk is completed successfully, the Intel TDX function may operate on the located Secure EPT entry. Otherwise, the function typically returns the last visited EPT entry and its level to the host VMM.

Guest-side (TDCALL) Intel TDX functions typically perform an EPT walk similar to the EPT walk done by the CPU. Only the GPA is provided as an input, and the function may walk the Shared EPT or the Secure EPT, depending on the specific function and the GPA's SHARED bit.

## 7.4. Secure EPT Induced TD Exits

- 20 Guest TD memory access to a non-present private GPA causes an asynchronous TD exit with an EPT Violation exit reason. As discussed in 7.2 above, a non-present GPA is any private GPA for which there is either no Secure EPT entry, or the Secure EPT entry is not in the SEPT\_PRESENT state. There is no TD exit with an EPT Misconfiguration on the Secure EPT.

On EPT violation TD exit, the content of the Secure EPT entry is provided to the host VMM to avoid the need for explicitly reading it using TDH.MEM.SEPT.RD.

- 25 Secure EPT-induced TD exits may also be triggered during a guest-side local flow, performing some function on behalf of the guest TD, and executed by the Intel TDX module.

## 7.5. Secure EPT Concurrency

Secure EPT concurrency rules are designed to support the expected usage and yet be as simple as possible.

### Host-Side (SEAMCALL) Functions:

- 30 • Functions that manage Secure EPT acquire **exclusive access** to the whole Secure EPT tree of the target TD.

- TDH.MEM.SEPT.RD and TDH.MEM.SEPT.WR acquire **shared access** to the whole Secure EPT tree of the target TD to help prevent changes to the tree while they execute.
- Other functions that only read Secure EPT for GPA-to-HPA translation (e.g., TDH.MR.EXTEND) acquire **shared access** to the whole Secure EPT tree of the target TD to help prevent changes to the tree while they execute.

## 5 Guest-Side (TDCALL) Functions

Guest-side functions emulate the CPU's top-down EPT walk operation.

- Guest-side functions have no concurrency restrictions on Secure EPT.
- Functions that need to modify Secure EPT entries (e.g., TDG.MEM.PAGE.ACCEPT) do so using atomic (locked) read-modify-write operations.

## 10 7.6. Introduction to TLB Tracking

The goal of TLB tracking is to be able to prove (when needed) that no logical processor holds any cached Secure EPT address translations to a given TD private **GPA range**. TLB tracking is required when removing a mapped TD private page (TDH.MEM.PAGE.REMOVE) or when changing the page mapping size (TDH.MEM.PAGE.PROMOTE), etc.

### GPA Range TLB Tracking Sequence

15 This sequence is intended to be used by the host VMM to help guarantee no EPT TLB entries exist to a set of GPA ranges.

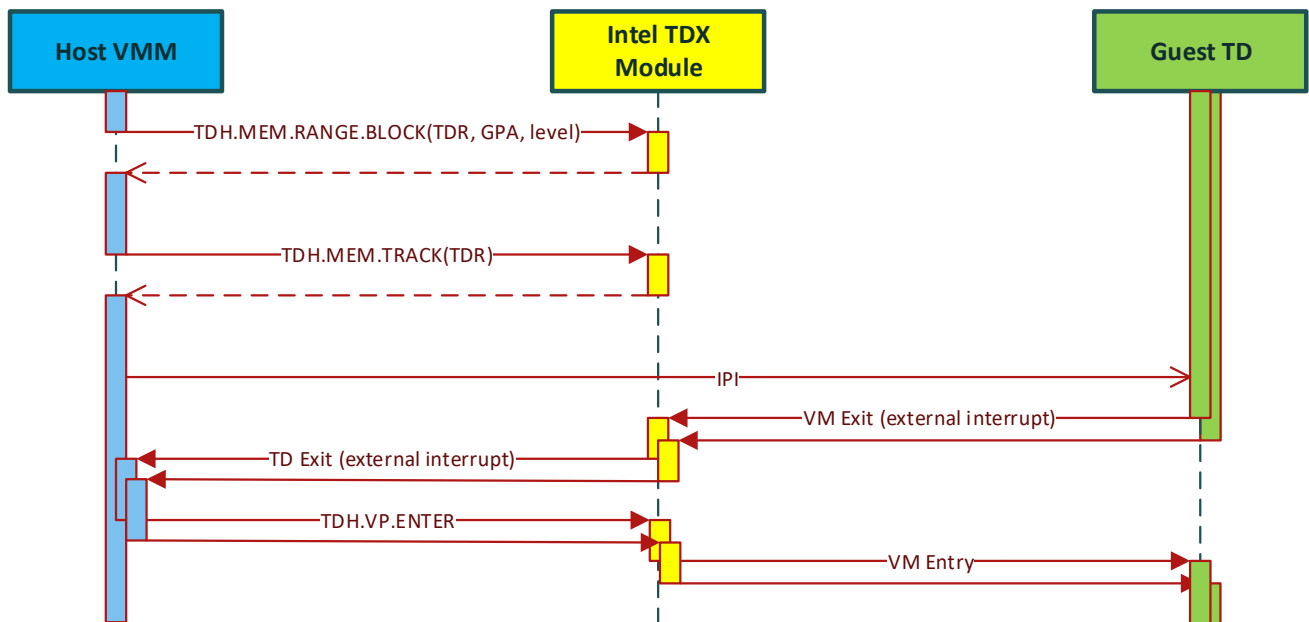


Figure 7.2: Typical TLB Tracking Sequence

The sequence typically includes five steps:

1. Execute TDH.MEM.RANGE.BLOCK on each GPA range, blocking subsequent creation of TLB translation to that range. Note that cached translations may still exist at this stage.
2. Execute TDH.MEM.TRACK, advancing the TD's epoch counter.
3. Send an Inter-Processor Interrupt (IPI) to each Remote Logical Processor (RLP) on which any of the TD's VCPUs is currently scheduled.
4. Upon receiving the IPI, each RLP will TD exit to the host VMM.
5. At this point the target GPA ranges are considered tracked. Even though some LPs may still hold TLB entries to the target GPA ranges, the following TD entry is designed to flush them.
5. Normally, the host VMM on each RLP will treat the TD exit as spurious and will immediately re-enter the TD.

## 7.7. Secure EPT Build and Update: TDH.MEM.SEPT.ADD

The host VMM can use the TDH.MEM.SEPT.ADD function to add a Secure EPT page to a guest TD. TDH.MEM.SEPT.ADD inputs are:

- Target TD, identified by its TDR HPA
- Destination physical page for the new Secure EPT table
- Mapping information: GPA and EPT level

At a high level, TDH.MEM.SEPT.ADD works as follows:

1. Check the TD keys are configured.
2. Check the destination physical page is marked as free in the PAMT.
3. Perform a Secure EPT walk to locate the Secure EPT non-leaf entry which will become the parent entry that maps the new Secure EPT page. To help prevent re-maps, TDH.MEM.SEPT.ADD checks the mapping does not already exist, else it aborts the operation.
4. Initialize the target page to zero using the target TD's private HKID and direct writes (MOVDIR64B).
5. Update the parent Secure EPT entry to map the page as SEPT\_PRESENT.
6. Update the page's PAMT entry with the PT\_EPT page type and the TDR PA as the OWNER.

The Secure EPT's root page (EPML4 or EPML5, depending on whether the host VMM uses 4-level or 5-level EPT) does not need to be explicitly added. It is created during TD initialization (TDH.MNG.INIT) and is stored as part of TDCS. On each VCPU initialization, TDH.VP.INIT copies the address of the Secure EPT root page to the VCPU's TD VMCS's EPTP field clearing the HKID bits to 0<sup>7</sup>.

The following example illustrates the build process of a 4-level Secure EPT hierarchy:

1. The host VMM calls TDH.MNG.CREATE(TDR\_PA = TDR<sub>0</sub>) to create the TD.
2. The host VMM calls TDH.MNG.ADDCX(TDR\_PA = TDR<sub>0</sub>, DST\_PA = TDCX\_PAGE\_PA) multiple times to allocate pages for TDCS. One of those pages will be used to host the Secure EPT root page D<sub>0</sub>.
3. Host VMM calls TDH.MNG.INIT(TDR\_PA = TDR<sub>0</sub>) to initialize the TD and set an EPML4 page in one of the previously added TDCX pages as the Secure EPT root page. This updates TDCS.EPTP.
4. TDH.VP.INIT of each VPCU copies TDCS.EPTP to the TD VMCS's EPTP field.
5. Host VMM calls TDH.MEM.SEPT.ADD(TDR\_PA = TDR<sub>0</sub>, DST\_PA = D<sub>1</sub>, GPA = G<sub>0</sub>, LVL= 3) to add an EPDPT page.
6. Host VMM calls TDH.MEM.SEPT.ADD(TDR\_PA = TDR<sub>0</sub>, DST\_PA = D<sub>2</sub>, GPA = G<sub>0</sub>, LVL= 2) to add an EPD page.
7. Host VMM calls TDH.MEM.SEPT.ADD(TDR\_PA = TDR<sub>0</sub>, DST\_PA = D<sub>3</sub>, GPA = G<sub>0</sub>, LVL= 1) to add an EPT page.

<sup>7</sup> The CPU adds the TD's private HKID on EPT walks. Having HKID as 0 allows the host VMM to use INVEPT, for managing the usage of shared EPT which shares the ASID with the TD's secure EPT (see [2]).

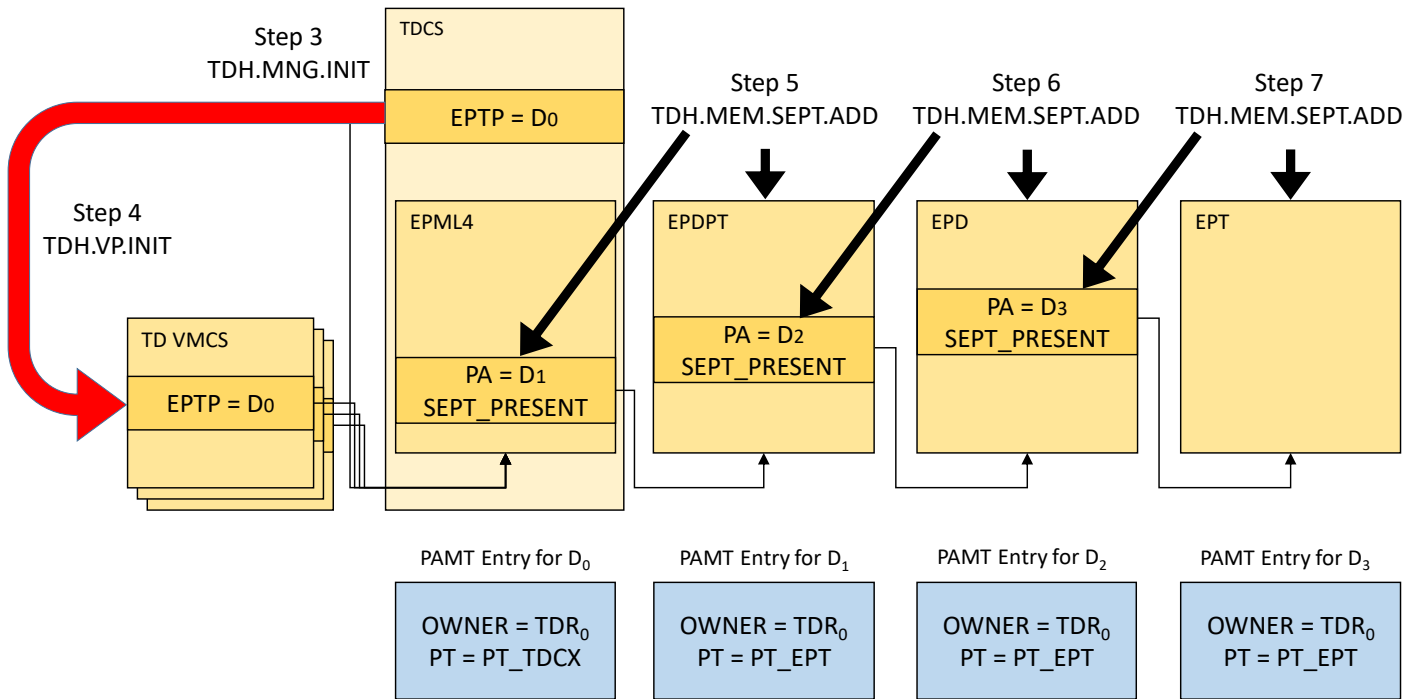


Figure 7.3: Typical Secure EPT Hierarchy Build Process

To help avoid stability issues caused by cache line aliasing, the VMM should assure that no cache lines associated with the added physical SEPT page are in a Modified state, before calling TDH.MEM.PAGE.AUG. This is typically done by calling TDH.PHYMEM.PAGE.WBINVD.

### 7.8. Adding TD Private Pages during TD Build Time: TDH.MEM.PAGE.ADD

Adding TD private pages with arbitrary content is allowed only during TD build time (before TDH.MR.FINALIZE). The host VMM adds and maps 4KB private pages to a guest TD using TDH.MEM.PAGE.ADD with the following inputs:

- Target TD, identified by its TDR physical address
- Source page physical address
- Destination page physical address
- Destination page GPA

At a high level, TDH.MEM.PAGE.ADD works as follows:

1. Check the TD has not been initialized.
2. Check the TD keys are configured.
3. Check the destination physical page is marked as free in the PAMT.
4. Perform a pseudo Secure EPT walk to locate the parent Secure EPT leaf entry that is going to map the new TD private page. To help prevent re-maps, TDH.MEM.PAGE.ADD checks the mapping does not already exist, else it aborts the operation.
5. Copy the source page to the destination page using the target TD's private HKID and direct writes (MOVDIR64B).
6. Update the previously located parent Secure EPT leaf entry to map the page as SEPT\_PRESENT.
7. Update the TD measurement with the new page GPA (as described in 10.1.1).
8. Update the PAMT entry with the PT\_REG page type and the TDR PA as the OWNER.

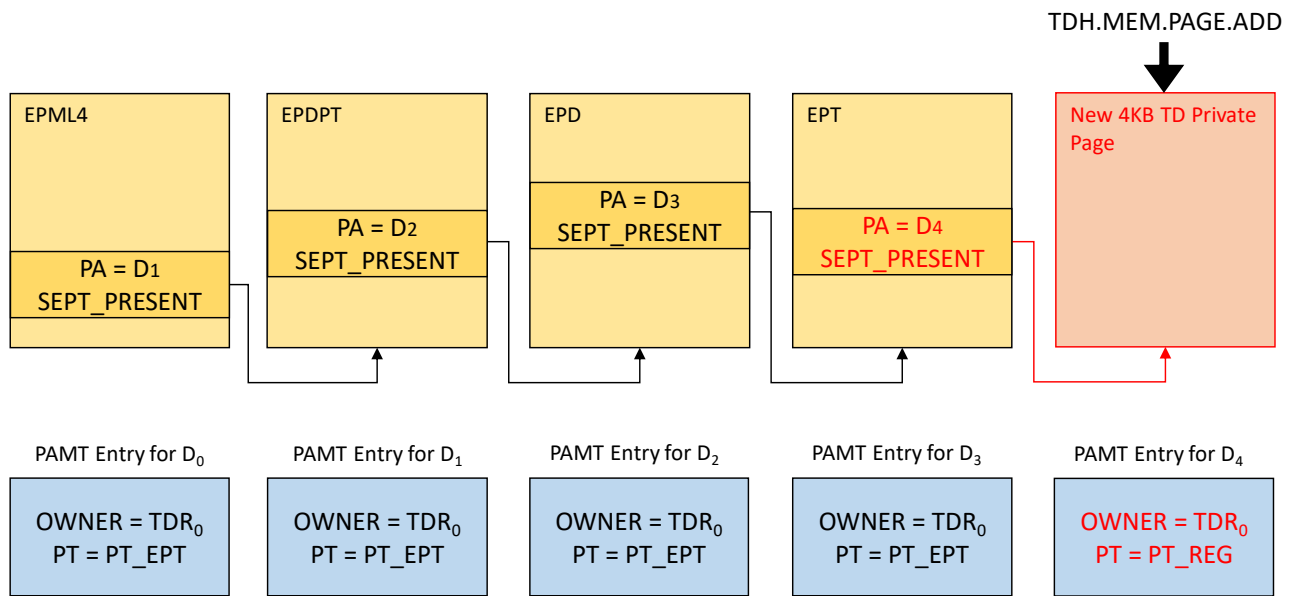


Figure 7.4: Typical Sequence for Adding a TD Private Page during TD Build Time

To help avoid stability issues caused by cache line aliasing, the VMM should assure that no cache lines associated with the added physical page are in a Modified state, before calling TDH.MEM.PAGE.AUG. This is typically done by calling TDH.PHYMEM.PAGE.WBINVD.

## 7.9. Dynamically Adding TD Private Pages during TD Run Time

### 7.9.1. Overview

Dynamically adding TD private pages after the guest TD has been initialized is typically done as a three-step process:

- The host VMM can update Secure EPT using TDH.MEM.SEPT.ADD and TDH.MEM.SEPT.REMOVE.
- The host VMM adds and maps a 4KB TD private page using TDH.MEM.PAGE.AUG. This page is not measured.
- The guest TD must accept the page before it can access it, using TDG.MEM.PAGE.ACCEPT. The page content is zeroed out.

This process is designed to help prevent attacks where the host VMM could remove arbitrary pages from the guest TD's GPA space (using TDH.MEM.PAGE.REMOVE) and replace them with zeroed-out pages.

Refer also to the software flow described in 3.3.1.1.

### 7.9.2. Page Addition by the Host VMM: TDH.MEM.PAGE.AUG

The host VMM can add and map 4KB private pages to a guest TD in a non-present and pending state using TDH.MEM.PAGE.AUG, with the following inputs:

- Target TD, identified by its TDR physical address
- Destination page physical address
- Destination page GPA

At a high level, TDH.MEM.PAGE.AUG works as follows:

1. Check the TD keys are configured.
2. Check the TD has been initialized and its build has been completed by TDH.MR.FINALIZE.
3. Check the destination physical page is marked as free in the PAMT.
4. Perform a pseudo Secure EPT walk to locate the parent Secure EPT leaf entry that is going to map the new TD private page. To help prevent re-maps, TDH.MEM.PAGE.AUG checks the mapping does not already exist, else it aborts the operation.
5. Update the previously located parent Secure EPT leaf entry to map the page as SEPT\_PENDING.
6. Update the PAMT entry with the PT\_REG page type and the TDR PA as the OWNER.

Note that TDH.MEM.PAGE.AUG does not need to access the destination page itself; the page is initialized later on by TDG.MEM.PAGE.ACCEPT.

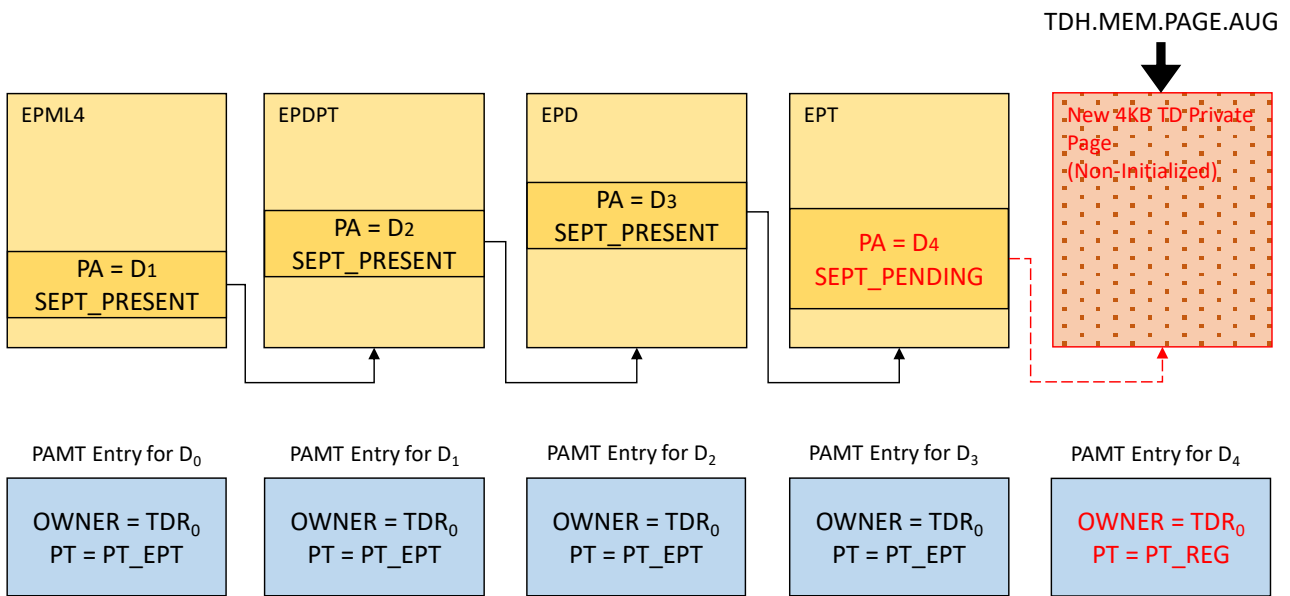


Figure 7.5: Host VMM Adding a TD Private Page during TD Run Time

To help avoid stability issues caused by cache line aliasing, the VMM should assure that no cache lines associated with the added physical page are in a Modified state, before calling TDH.MEM.PAGE.AUG. This can be done by calling TDH.PHYMEM.PAGE.WBINVD.

7.9.3. Page Acceptance by the Guest TD: TDG.MEM.PAGE.ACCEPT

The guest TD can accept a dynamically added 4KB page using TDG.MEM.PAGE.ACCEPT with the page GPA as an input.

At a high level, TDG.MEM.PAGE.ACCEPT works as follows:

1. Perform a pseudo Secure EPT walk to locate the parent Secure EPT leaf entry that maps the TD private page.
2. Check that the page is indeed mapped as SEPT\_PENDING.

If the Secure EPT entry is not found, or if its state is other than SEPT\_PENDING (even if it is SEPT\_PENDING\_BLOCKED), TDG.MEM.PAGE.ACCEPT is morphed into a TD Exit with an EPT Violation exit reason and an indication that the violation is due to TDG.MEM.PAGE.ACCEPT. For details, see the TDH.VP.ENTER definition in 20.2.31.

3. Initialize the page to zero using the target TD's private HKID and direct writes (MOVDIR64B).
4. Update the parent Secure EPT entry to set its state to SEPT\_PRESENT.

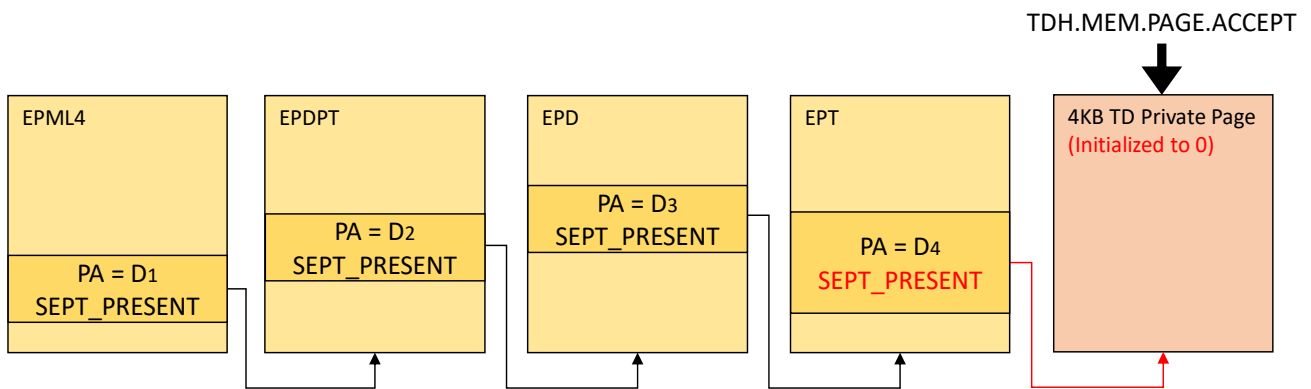


Figure 7.6: Guest TD Accepting a Pending TD Private Page

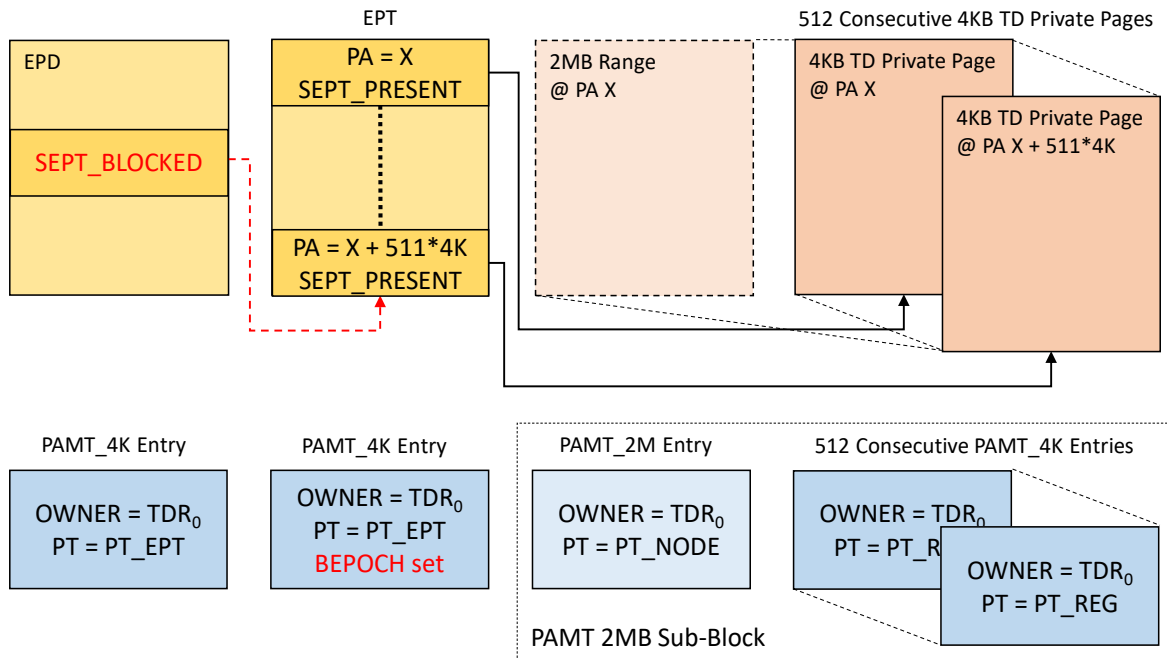
Notes on TDG.MEM.PAGE.ACCEPT Concurrency

TDG.MEM.PAGE.ACCEPT runs from a guest TD context, and it does not impose any concurrency restrictions on Secure EPT access. It is the responsibility of the guest TD to not call TDG.MEM.PAGE.ACCEPT concurrently on the same page. Failing that responsibility may result in corruption of the page contents.

**7.10. Page Merge: TDH.MEM.PAGE.PROMOTE**

The host VMM can merge the mapping of 512 consecutive 4KB or 2MB pages to a single 2MB or 1GB page, respectively. To do that, the host VMM should first perform the TLB tracking protocol on the large (2MB or 1GB) GPA range.

The host VMM should first call TDH.MEM.RANGE.BLOCK which operates on the EPT page for the large range (EPT for 2MB, EPD for 1GB). TDH.MEM.RANGE.BLOCK marks the parent EPT entry for that EPT page as **SEPT\_BLOCKED** and records the TD epoch in the PAMT entry of the EPT page. Figure 7.7 below shows the situation after TDH.MEM.RANGE.BLOCK blocked a 2MB GPA range.



**Figure 7.7: Typical State after Blocking a Range of 512 Consecutive 4KB TD Private Pages**

Typically, the host VMM then calls TDH.MEM.TRACK and performs a round of IPIs. After that, there should be no active address translation to the large (2MB or 1GB) GPA range.

The actual merge is done by TDH.MEM.PAGE.PROMOTE which has the following inputs:

- The large range GPA
- The large page level (2MB or 1GB)

At a high level, TDH.MEM.PAGE.PROMOTE works as follows:

1. Check the TLB tracking condition for the large range GPA (i.e., the EPT or EPD page for that range).
2. Check that all 512 entries of that EPT or EPD page are in the SEPT\_PRESENT state and point to leaf pages whose physical address is contiguous within the same 2MB or 1GB range.

If all checks pass, TDH.MEM.PAGE.PROMOTE does the following:

1. Mark all the PAMT\_4K or PAMT\_2M entries of the small leaf pages (4KB or 2MB, respectively) as PT\_NDA.
2. Mark the PAMT\_2M or PAMT\_1G entry of the merged large (2MB or 1GB, respectively) pages as PT\_REG.
3. Set the parent EPT entry to point to the merged large page, and mark it as present.
4. Mark the original EPT or EPD page's PAMT entry as PT\_NDA, effectively removing this for any use by the host VMM.

Once complete, the former EPT or EPD physical page should be free for use by the host VMM for any purpose. To help avoid stability issues caused by cache line aliasing, the host VMM should also assure that no cache lines associated with the page are in a Modified state. This is done by calling TDH.PHYMEM.PAGE.WBINVD.

Figure 7.8 below shows a typical 2MB merged page after TDH.MEM.PAGE.PROMOTE.



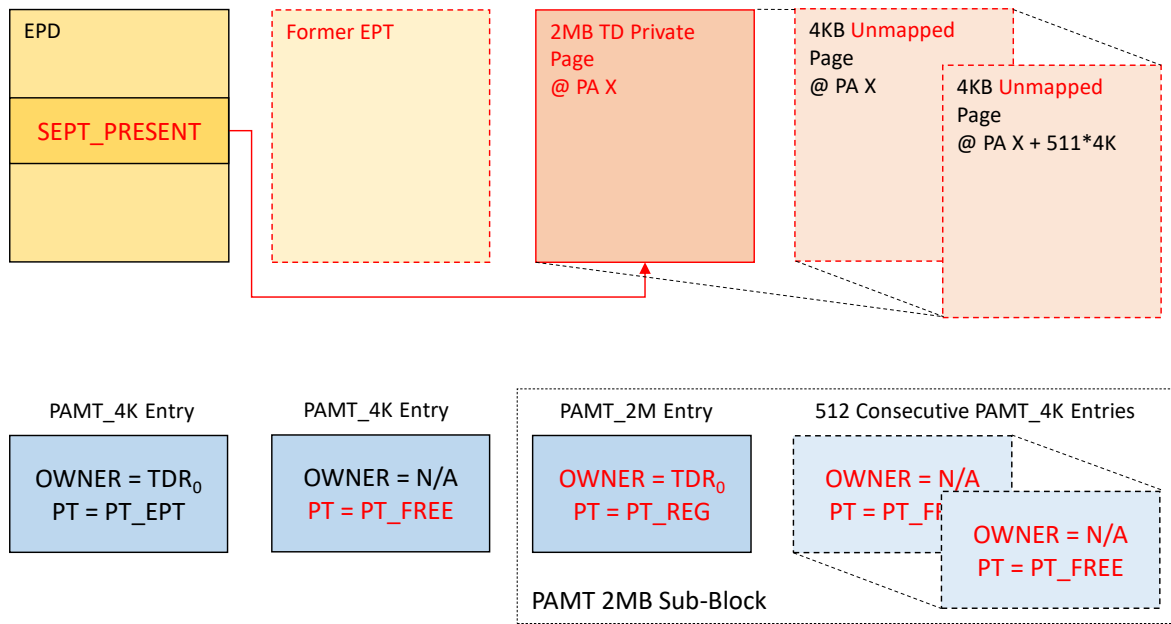


Figure 7.8: Typical State of a 2MB TD Private Page after TDH.MEM.PAGE.PROMOTE

Refer also to the software flow described in 3.3.1.3.

7.11. Page Split: TDH.MEM.PAGE.DEMOTE

- 5 The host VMM can split the mapping of a single 2MB or 1GB page to 512 consecutive 4KB or 2MB pages, respectively. To do that, the host VMM should first perform the TLB tracking protocol on the large (2MB or 1GB) page.

The host VMM should first call TDH.MEM.RANGE.BLOCK on the large page. TDH.MEM.RANGE.BLOCK marks the parent EPT entry for that page as SEPT\_BLOCKED and records the TD epoch in the PAMT entry of the page. Figure 7.9 below shows the typical situation after TDH.MEM.RANGE.BLOCK blocked a 1GB large page.

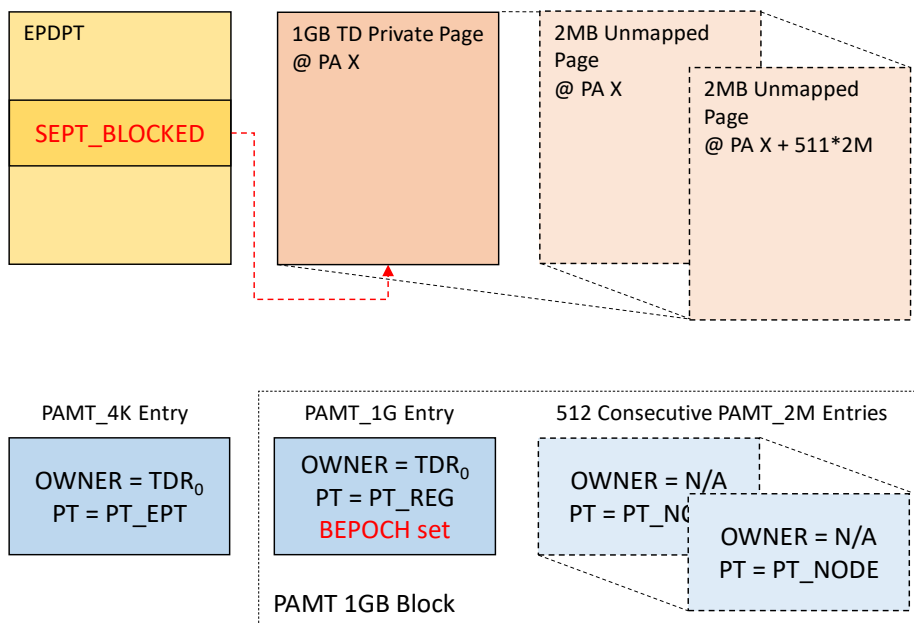


Figure 7.9: Typical State after Blocking a 1GB Page

Typically, the host VMM then calls TDH.MEM.TRACK and performs a round of IPIs. After that, there should be no active address translation to the large (2MB or 1GB) page.

The actual split is done by TDH.MEM.PAGE.DEMOTE which has the following inputs:

- 15 • The large page GPA
- The large page level (2MB or 1GB)

- The physical address of a free page that will be used for a new EPT or EPD page

At a high level, TDH.MEM.PAGE.DEMOTE works as follows:

1. Check the TLB tracking condition for the large page.
  2. Check that the physical page for the new EPT or EPD is marked as free in the PAMT.
- 5 If all checks pass, TDH.MEM.PAGE.DEMOTE does the following:
3. Mark the PAMT\_2M or PAMT\_1G entry of the large (2MB or 1GB respectively) page as PT\_NDA.
  4. Mark all the PAMT\_4K or PAMT\_2M entries of the small (4KB or 2MB respectively) consecutive leaf pages as PT\_REG.
  5. Initialize the new EPT or EPD page with 512 EPT entries pointing to the 512 consecutive leaf pages.
  6. Mark the new EPT or EPD page's PAMT entry as PT\_EPT.
- 10 7. Set the parent EPT entry to point to the new EPT or EPD page.

Figure 7.10 below shows the typical state of a 1GB GPA range after TDH.MEM.PAGE.DEMOTE.

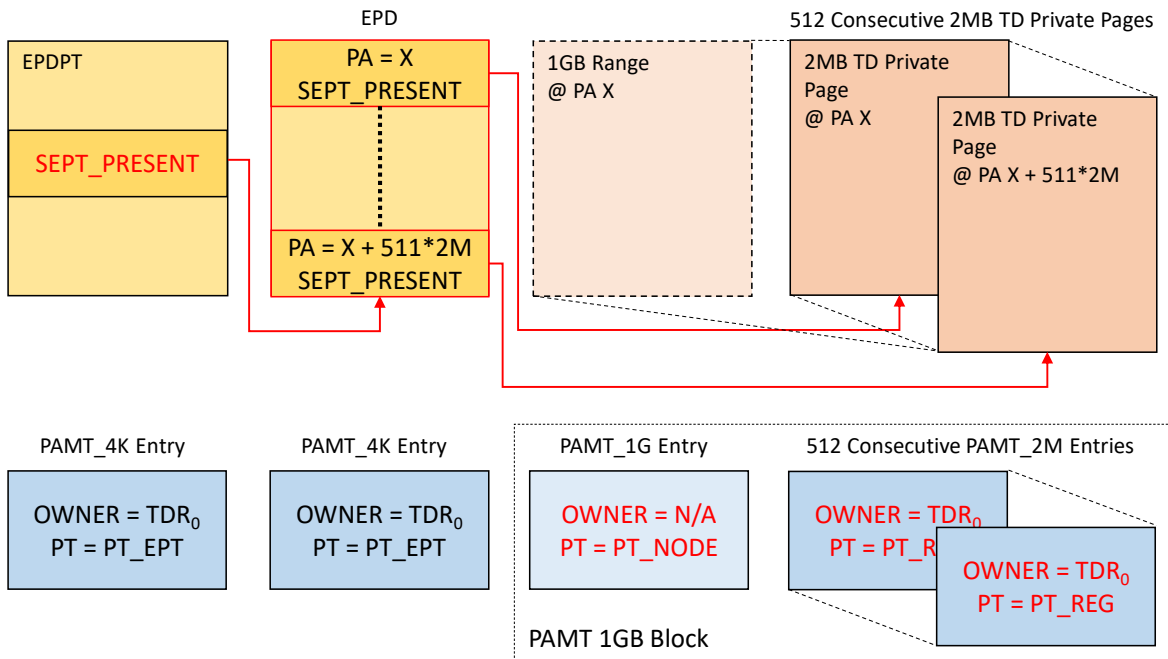


Figure 7.10: Typical State of a 1GB TD Private Range after TDH.MEM.PAGE.DEMOTE

Refer also to the software flow described in 3.3.1.4.

15 **7.12. Removing TD Private Pages: TDH.MEM.PAGE.REMOVE**

The host VMM can remove TD private pages using TDH.MEM.PAGE.REMOVE, freeing them for any use. 4KB, 2MB and 1MB pages can be removed – no demotion is required for large pages. The host VMM should first perform the TLB tracking protocol on the page.

20 The host VMM should first call TDH.MEM.RANGE.BLOCK on the target page. TDH.MEM.RANGE.BLOCK marks the parent EPT entry for that page as SEPT\_BLOCKED (if it was SEPT\_PRESENT) or SEPT\_PENDING\_BLOCKED (if it was SEPT\_PENDING) and records the TD epoch in the PAMT entry of the page.

Typically, the host VMM then calls TDH.MEM.TRACK and performs a round of IPIs. After that, there should be no active address translation to target page.

The actual removal is done by TDH.MEM.PAGE.REMOVE which has the following inputs:

- 25
- The page GPA
  - The page level (4KB, 2MB or 1GB)

At a high level, TDH.MEM.PAGE.REMOVE works as follows:

1. Check the TLB tracking condition for the page.
2. Check that the mapping size of the page fits the input parameter.

If all checks pass, TDH.MEM.PAGE.REMOVE does the following:

3. Mark the EPT entry for the target page as SEPT\_FREE.
4. Mark the PAMT entry of the page as PT\_NDA.

5 Once complete, the physical page should be free for use by the VMM for any purpose. To help avoid stability issues caused by cache line aliasing, the VMM should also assure that no cache lines associated with the removed page are in a Modified state. This is typically done by calling TDH.PHYMEM.PAGE.WBINVD.

Refer also to the software flow described in 3.3.1.2.

### 7.13. Removing a Secure EPT Page: TDH.MEM.SEPT.REMOVE

10 The host VMM can remove a Secure EPT page using TDH.MEM.SEPT.REMOVE, freeing it for any use, provided all its entries are SEPT\_FREE. The host VMM should first perform the TLB tracking protocol on the page.

The host VMM should first call TDH.MEM.RANGE.BLOCK on the Secure EPT page. TDH.MEM.RANGE.BLOCK marks the parent EPT entry for that page as **SEPT\_BLOCKED** and records the TD epoch in the PAMT entry of the page.

Typically, the host VMM then calls TDH.MEM.TRACK and performs a round of IPIs. After that, there should be no active address translation to GPA range presented by the Secure EPT page to be removed.

15 The actual removal is done by TDH.MEM.SEPT.REMOVE which has the following inputs:

- The Secure EPT page GPA
- The EPT level

At a high level, TDH.MEM.SEPT.REMOVE works as follows:

- 20 1. Check the TLB tracking condition for the page.
2. Check that the mapping size of the page fits the input parameter.
3. Check that all 512 entries of the Secure EPT page are PT\_NDA.

If all checks pass, TDH.MEM.SEPT.REMOVE does the following:

4. Mark the EPT entry for the Secure EPT page as SEPT\_FREE.
5. Mark the PAMT entry of the Secure EPT page as PT\_NDA.

25 Once complete, the physical page should be free for use by the VMM for any purpose. To help avoid stability issues caused by cache line aliasing, the VMM should also assure that no cache lines associated with the page are in a Modified state. This is typically done by calling TDH.PHYMEM.PAGE.WBINVD.

### 7.14. Unblocking a GPA Range: TDH.MEM.RANGE.UNBLOCK

30 The host VMM can unblock previously blocked TD private GPA ranges using TDH.MEM.RANGE.UNBLOCK, returning them to their original state. 4KB, 2MB and 1MB GPA ranges can be unblocked.

The host VMM should first complete the TLB tracking protocol on the GPA range. It typically calls TDH.MEM.TRACK and performs a round of IPIs. After that, there should be no active address translation to target page.

The actual unblocking is done by TDH.MEM.RANGE.UNBLOCK which has the following inputs:

- 35 • The GPA
- The GPA range level (4KB, 2MB or 1GB)

At a high level, TDH.MEM.RANGE.UNBLOCK works as follows:

1. Check the TLB tracking condition for the GPA range.
2. Check that the mapping size of the GPA range fits the input parameter.

If all checks pass, TDH.MEM.RANGE.UNBLOCK does the following:

- 40 3. Mark the EPT entry for the target GPA as SEPT\_PRESENT (if it was SEPT\_BLOCKED) or SEPT\_PENDING (if it was SEPT\_PENDING\_BLOCKED).

Refer also to the software flow described in 3.3.1.5.

## 8. TD VCPU

This chapter discusses multiple items related to TD VCPUs.

### 8.1. TD VCPU Initial State

Intel SDM, Vol. 3, 9.1.1 Processor State after Reset

#### 8.1.1. Overview

As designed, most of the TD VCPU initial state is the same as the processor architectural state after INIT. However, there are some differences:

- The TD VCPU starts its life in protected (32-bit) non-paged mode, not in real mode. It is allowed only to switch to 64b mode. This impacts the initial state of segment registers, CRs and MSRs. Mode restrictions in TDX non-root mode are described in 9.2.
- The IA32\_EFER MSR is initialized to support the CPU modes described in 9.2.
- The initial values of some GPRs provide some basic information to the guest TD as described in 8.1.2 below. This information should be sufficient for the vBIOS to set up paging tables and switch as soon as possible to 64b mode, where it can use the TDCALL leaf functions.

See also the TDVPS fields in 19.2 and TD VMCS guest state area in 19.2.4.1.

#### 8.1.2. Initial State of Guest TD GPRs

As designed, the following initial state is different than the architectural INIT state:

**Table 8.1: Initial Values of GPRs Different from their Architectural INIT Values**

Register	Bits	Initial Value
RBX	5:0	GPAW, the effective GPA width (in bits) for this TD (do not confuse with MAXPA) – SHARED bit is at GPA bit GPAW-1 Only GPAW values 48 and 52 are possible.
	63:6	Reserved: set to 0
RCX, R8	63:0	The value of RCX and R8 is provided as an input to TDH.VP.INIT (the same value in both GPRs). No checking is done on this value; the intention is for vBIOS to read RCX immediately after the first TDH.VP.ENTER, and use the RCX value appropriately as set by software convention.
RDX	31:0	Set to the virtualized Family/Model/Stepping returned by CPUID(1).EAX. The value is calculated by TDH.SYS.INIT as to have the minimum Stepping ID across all packages.
	63:32	Reserved: set to 0
RSI	31:0	Virtual CPU index, starting from 0 and allocated sequentially on each successful TDH.VP.INIT
	63:32	Reserved: set to 0
RIP	63:0	Set to 0xFFFFFFFF0 (i.e., 4GB - 16B)

#### 8.1.3. Initial State of CRs

As designed, the following initial state is different than the architectural INIT state:

- CR0 is initialized to 0x0021 – bits PE (0) and NE (5) are set to 1, and all other bits are cleared to 0. See 9.5.1 for details.
- CR4 is initialized to 0x2040 – bits MCE (6) and VMXE (13) are set to 1, and all other bits are cleared to 0. Note that the virtualized value of VMXE is 0, due to the setting of the TD VMCS “CR4 guest/host mask” and “CR4 read shadow” controls. See 9.5.2 for details.

#### 8.1.4. Initial State of Segment Registers

As designed, the following initial state is different than the architectural INIT state:

- CS, DS, ES, FS, GS and SS are initialized with a base of 0 and limit of 0xFFFFFFFF.
- LDTR, TR and GDTR are initialized with a base of 0 and limit of 0xFFFF.
- IDTR is initialized as invalid (limit of 0).

For details, see 19.2.4.1.1.

#### 8.1.5. Initial State of MSRs

As designed, the following initial state is different than the architectural INIT state:

- IA32\_EFER is initialized to 0x901 – SCE (bit 0), LME (bit 8) and NXE (bit 11) are set to 1, and all other bits are cleared to 0.

## 8.2. TD VCPU TLB Address Space Identifier (ASID)

Non-root mode cached address translations are tagged with unique Address Space Identifiers (ASIDs). The goal of TD ASIDs is to reduce the need to flush TLB entries on TD Entry and TD Exit due the associated performance costs as a result of the flushing.

### 8.2.1. TD ASID Components

Table 8.2 below shows a high-level view of the components of the TD ASID. The exact structure is micro-architectural.

**Table 8.2: TD ASID**

Field	Size (Bits)	Description and TDX Usage
<b>SEAM</b>	1	This is an implicit bit 16 of VPID not directly visible to software. It is set to 1 by the CPU in SEAM mode. This bit prevents overlap with legacy (non-TDX) ASIDs.
<b>VPID</b>	16	Set by the Intel TDX module to VCPU_INDEX, a unique index of a VCPU in a TD, plus 1 (since VCPU_INDEX starts with 0 which is not a value VPID number for non-root mode)
<b>EPTP</b>	40	Bits [51:12] of the EPTP, which for a TD points to the <b>Secure</b> EPT root – HKID bits are cleared to 0  Note that EPTP is unique per TD and is used as an ASID component for <b>both Secure EPT and Shared EPT</b> translations caching.
<b>PCID</b>	16	Same as legacy PCID

### 8.2.2. INVEPT by the Host VMM for Managing the Shared EPT

The same ASID based on the TD's EPTP is used for caching both secure and shared EPT translations (remember: EPTP is the HPA of the **secure** EPT root page). Thus, to flush shared EPT translations, the host VMM uses INVEPT specifying the TD's EPTP, not its Shared EPTP. The host VMM can obtain the value of EPTP from the TD VMCSs using TDH.VP.RD.

## 8.3. VCPU-to-LP Association

### 8.3.1. Non-Coherent Caching

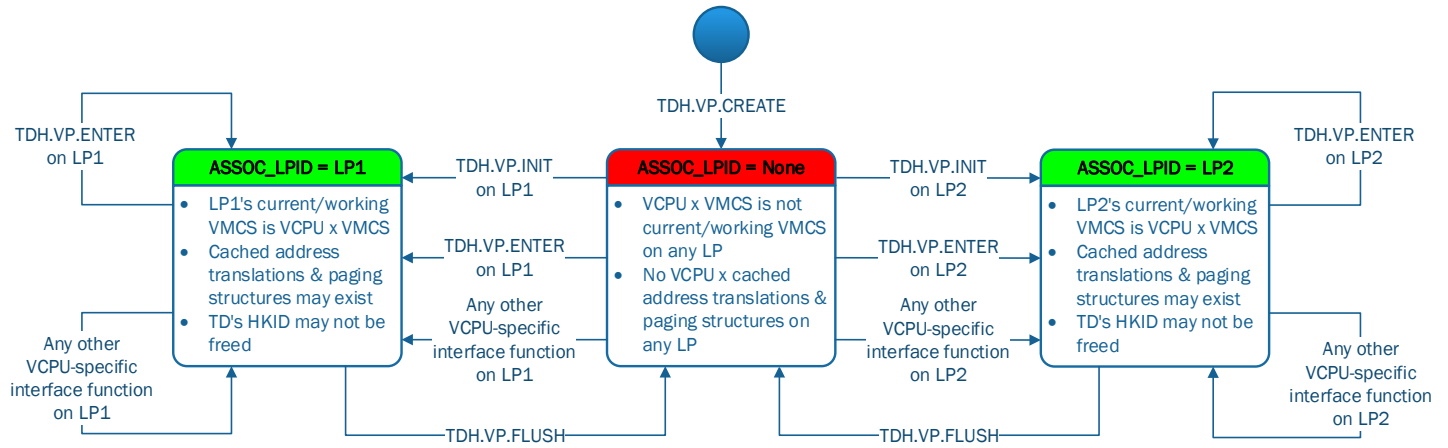
Some TD VCPU state is non-coherently cached. This includes:

- Address translations (TLB/PxE entries) must be explicitly flushed in case they may be stale.

- TD VMCS is cached by the CPU. VMX architecture requires making a VMCS current by VMPTRLD before using it with most VMX instructions, and then explicitly writing it to memory and making it non-current by VMCLEAR before the VMCS memory image can be handled (e.g., by making it current on another LP).

This non-coherent caching implies that some explicit and/or implicit operations are done to help guarantee correctness. This is described in the following sections.

**8.3.2. Intel TDX Functions for VCPU-LP Association and Dis-Association**



**Figure 8.1: VCPU Association State Machine**

The following Intel TDX module mechanisms are designed to help assure correct and secure operation:

- TD VCPU to LP association is many-to-one. A TD VCPU can be associated with at most one LP at any given time. An LP may be associated with multiple VCPUs.
- VCPU to LP association is implicitly done by any VCPU-specific SEAMCALL flow, including TDH.VP.ENTER. Those flows check that the VCPU is either already associated with the current LP or is not associated with any LP.
- If the host VMM wishes to associate a VCPU with another LP, it must explicitly flush the VCPU state on the LP currently associated with it using **TDH.VP.FLUSH**. This function performs TD ASID, and extended paging structure (EPxE) caches TLB flush and VMCLEAR. For details, see 20.2.23.
- If the VMM wishes to reclaim the TD's private HKID, thus making the TDVPS memory inaccessible, it must explicitly flush the VCPU state on the LP currently associated with it. This is described in 4.4.

**8.3.3. Performance Considerations**

- Migrating VCPUs between LPs is costly. As described above, it involves flushing address translation caches, paging structure caches and VMCS cache. The host VMM should minimize that for best performance.
- Address translation and paging structure caches are flushed at TD-scope on the current LP. This flushing impacts the (possibly non-typical) case where multiple VCPUs of the same TD are associated with a single LP.

**8.4. VCPU Activity State Machine**

The VCPU activity state machine, controlled by TDVPS.STATE as shown in Table 8.3 below and shown in Figure 8.2 below, helps assure the following:

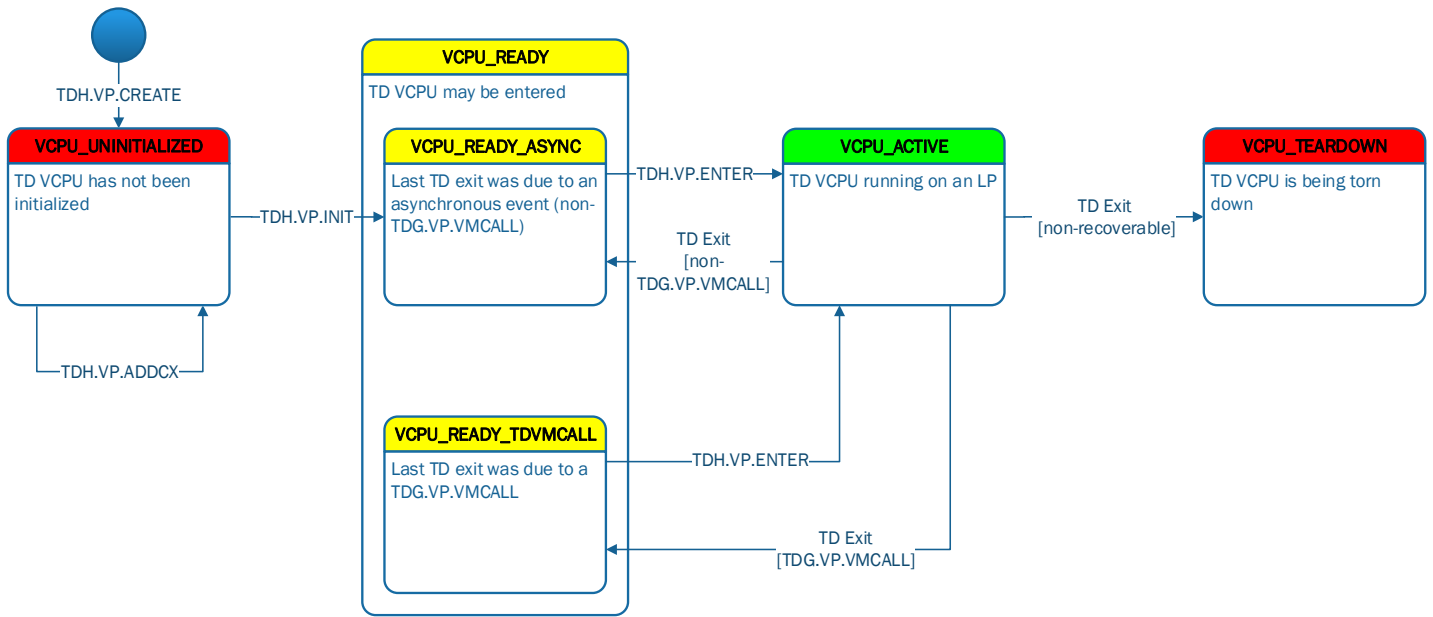
- A VCPU can be entered only when its logical TDVPS control structure, composed of TDVPR and TDVPX pages, is available in memory and has been initialized.
- A VCPU can be entered only if its state is consistent (no non-recoverable TD exit happened).
- TD entry is done properly, depending on whether it is the first entry or on the last TD exit type.

**Table 8.3: TDVPS.STATE Definition**

State Name	Description
<b>VCPU_UNINITIALIZED</b>	VCPU has not been initialized yet by TDH.VP.INIT.
<b>VCPU_READY</b>	This is a super-state with 2 sub-states. In this super-state, VCPU can be entered.
<b>VCPU_READY_ASYNC</b>	Last TD exit was due to an asynchronous event (non-TDG.VP.VMCALL). VCPU state has been fully saved on TD exit and will be restored on the next TD entry.
<b>VCPU_READY_TDG.VP.VMCALL</b>	Last TD exit was due to a TDG.VP.VMCALL. On the next TD entry, most GPR and all XMM state will be forwarded to the guest TD from the host VMM.
<b>VCPU_ACTIVE</b>	VCPU is active (TDX non-root mode) on some LP.
<b>VCPU_TEARDOWN</b>	VCPU is being torn down.

TD Entry and TD Exit transitions normally toggle between the VCPU\_READY super-state and the VCPU\_ACTIVE state, except when a non-recoverable TD Exit (Triple Fault, Non-Commit with a TD context corruption indication) transitions to a VCPU\_TEARDOWN state.

5



**Figure 8.2: VCPU Activity State Machine**

## 9. TDX CPU Virtualization (Non-Root Mode Operation)

This chapter describes how the Intel TDX module virtualizes the CPU to a guest TD.

### 9.1. Guest TD Run Time Environment Enumeration

Guest software can be designed to run either as a TD, as a legacy virtual machine, or directly on the CPU, based on enumeration of its run-time environment. Figure 9.1 below shows a typical flow used by guest software.

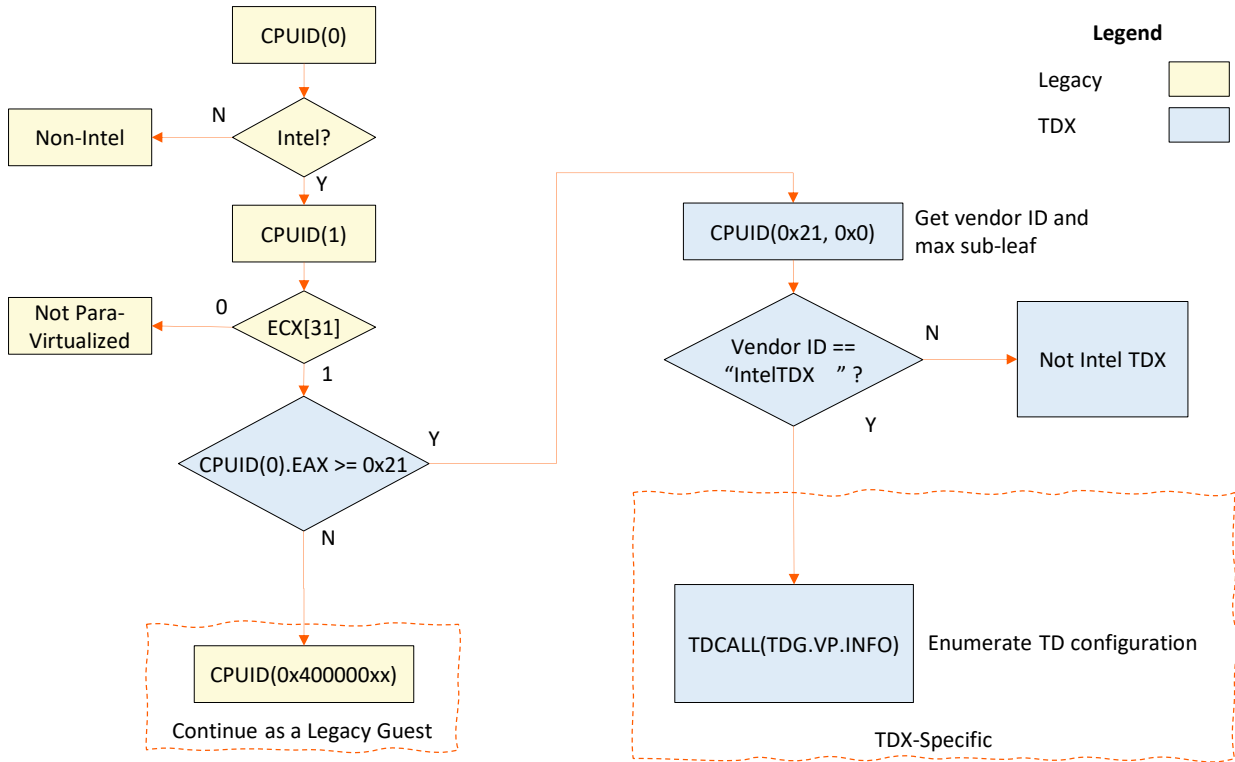


Figure 9.1: Typical Run-Time Environment Enumeration by a Guest TD

CPUID leaf 0x21 emulation is done by the Intel TDX module. Sub-leaf 0 returns the values shown below. Other sub-leaves return 0 in RAX/RBX/RCX/RDX.

Table 9.1: TDX Enumeration by CPUID(0x21,0)

GPR	Value (Hex)	Description
EAX	0x00000000	Maximum sub-leaf number
EBX	0x65746E49	“Inte”
ECX	0x20202020	“ ”
EDX	0x5844546C	“1TDX”

Once the guest software discovers that it runs as a TD, it can use TDG.VP.INFO to get basic information.

### 9.2. CPU Mode Restrictions

- Intel SDM, Vol. 3, 2.2 Modes of Operation
- Intel SDM, Vol. 3, 9.8.5 Initializing IA-32e Mode
- Intel SDM, Vol. 3, 11.5.1 Cache Control Registers and Bits
- Intel SDM, Vol. 3, 24.6.6 Guest/Host Masks and Read Shadows for CR0 and CR4

A TD OS running in TDX non-root mode is required to be a 64-bit OS. The Intel TDX module helps enforce this with the restrictions described below.



**Table 9.2: CPU Mode Restrictions in TDX Non-Root Mode**

Restriction	Description
<b>CPU and Paging Modes</b>	<p>In TDX non-root mode, the CPU is allowed to run in the following modes:</p> <ul style="list-style-type: none"> <li>• Protected mode (32-bit) with no paging (CR0.PG == 0)</li> <li>• IA-32e mode with 4-level or 5-level paging (CR0.PG == 1), with the sub-modes controlled by CS.L: <ul style="list-style-type: none"> <li>○ 64-bit mode</li> <li>○ Compatibility (32-bit) mode</li> </ul> </li> </ul> <p>To achieve this, CR0.PE and IA32_EFER.LME are enforced to 1, as described in the following sections.</p>
<b>Execute Disable</b>	<p>When running in IA-32e mode, the PT Execute Disable bit (63) is always enabled.</p> <p>To achieve this, IA32_EFER.NXE is enforced to 1, as described in the following sections.</p>
<b>Caching is Always Enabled</b>	<p>The guest TD runs in Normal Cache Mode.</p> <p>To achieve this, CR0.CD and CR0.NW are enforced to 0, as described in the following sections.</p>

### 9.3. Instructions Restrictions

The Intel TDX module is designed to block certain instructions from executing in TDX non-root mode. Execution of those instructions results in a VM exit to the Intel TDX module, which then injects either a #UD or a #VE to the guest TD, as described in 9.9.

Execution of other instructions may be conditionally blocked, depending on feature enabling, as described in the following sections.

#### 9.3.1. Instructions that Cause a #UD Unconditionally

- ENQCMD, ENQCMD5
- ENCLS, ENCLV
- Most VMX instructions: INVEPT, INVVPID, VMCLEAR, VMFUNC, VMLAUNCH, VMPTRLD, VMPTRST, VMREAD, VMRESUME, VMWRITE, VMXOFF, VMXON
- RSM
- GETSEC

#### 9.3.2. Instructions that Cause a #VE Unconditionally

- String I/O (INS\*, OUTS\*), IN, OUT
- HLT
- MONITOR, MWAIT
- WBINVD, INVD
- VMCALL

#### 9.3.3. Instructions that Cause a #UD or #VE Depending on Feature Enabling

- PCONFIG (see 9.14)

## 9.4. Extended Feature Set

Intel SDM, Vol. 1, 13

Managing State Using the XSAVE Feature Set

Intel SDM, Vol. 3, 13

System Programming for Instruction Set Extensions and Processor Extended State

### 9.4.1. Allowed Extended Features Control

- 5 At the guest TD scope, **TDCS.XFAM (Extended Features Allowed Mask)** is provided as an input during guest TD build process. XFAM is a 64b mask, using the **state-component bitmap** format used by extended state ISA (XSAVE, XRSTOR, XCRO, IA32\_XSS etc.), which specifies the set of extended features the TD is allowed to use.

XFAM is checked to be compliant with the set of extended features supported by the CPU, as enumerated by CPUID and the allowed bit combinations, as shown in Table 9.3 below.

### 10 9.4.2. Extended State Isolation

The Intel TDX module helps assure that any guest TD extended state is saved and isolated from the host VMM across TD exit and entry. It is the VMM's responsibility to save its own extended state across TD entry and exit.

- Before TDH.VP.ENTER, the host VMM should save (e.g., using XSAVES) any extended state that the guest TD VCPU is allowed to use (per XFAM) and the host VMM expects to need after TDH.VP.ENTER is complete.
- 15 • The TDH.VP.ENTER function loads the extended state that the TD VCPU is allowed to use, per XFAM, from the VCPU's TDVPS. An exception to this is when TDH.VP.ENTER follows a previous TDG.VP.VMCALL – in the case TDH.VP.ENTER does not load the XMM state (corresponding to XFAM bit 1) from TDVPS, but passes it directly from the host VMM.
- On an asynchronous TD exit, the Intel TDX module saves the extended state that the TD VCPU was allowed to use, per XFAM, to the VCPU's TDVPS. It then clears the extended state.
- 20 • On TDG.VP.VMCALL, the Intel TDX module works similarly, but it selectively does not clear some of the XMM register state (corresponding to XFAM bit 1). That XMM state is passed directly to the host VMM.
- On completion of TDH.VP.ENTER (following TD exit), the VMM may restore any extended state that it saved before TDH.VP.ENTER.

### 9.4.3. Extended Features Execution Control

- 25 The Intel TDX module is designed to prohibit the guest TD from using any extended feature not allowed by XFAM. Many extended state features are controlled by XCRO and IA32\_XSS MSR. Other features are controlled by CR4 or by specific MSRs.

<b>XCRO and IA32_XSS MSR</b>	On XSETBV, which attempts to write to XCRO, and on WRMSR of IA32_XSS, the following cases cause a #GP(0): <ul style="list-style-type: none"> <li>• The new value is not natively valid for XCRO or IA32_XSS (it sets reserved bits, sets bits for features not recognized by the Intel TDX module, or uses illegal bit combinations).</li> <li>• The new value has any bits set that are not allowed by XFAM.</li> </ul>
<b>CR4</b>	On MOV to CR4, the guest TD attempts to set bits not allowed according to XFAM will cause a #GP(0).
<b>Other MSRs</b>	The guest TD attempts to write or read certain MSRs that are not enabled according to XFAM can cause a #GP(0) or a #VE, as described below.

The following table describes how a guest TD executes each of the extended features.

Table 9.3: Extended Features Enumeration and Execution Control

Bits	U/S	Feature	Enumeration <sup>8</sup>	XFAM Value	Description
0	U	FP	Always available	1	Always enabled
1	U	SSE	Always available	1	Always enabled
2	U	AVX	CPUID(0xD,0x0).EAX[2] CPUID(0x7,0x0).EBX[2] CPUID(0x7,0x0).ECX[10:9] CPUID(0x7,0x1).EAX[5] CPUID(0xD, 0x2).*	0 or 1	Execution is directly controlled by XCRO.
4:3	U	MPX	CPUID(0xD,0x0).EAX[4:3] CPUID(0x7,0x0).EBX[14] CPUID(0xD, 0x3).* CPUID(0xD, 0x4).*	00	MPX is being deprecated.
7:5	U	AVX512	CPUID(0xD,0x0).EAX[7:5] CPUID(0x7,0x0).EBX[31:30, 28:26, 21, 17:16] CPUID(0x7,0x0).ECX[14, 12:11, 6, 1] CPUID(0x7,0x0).EDX[8] CPUID(0x7,0x1).EAX[5] CPUID(0xD, 0x5).* CPUID(0xD, 0x6).* CPUID(0xD, 0x7).*	000 or 111	Execution is directly controlled by XCRO. AVX512 may be enabled only if AVX is enabled – i.e., XFAM[7:5] may be set to 111 only when XFAM[2] is set to 1.
8	S	PT (RTIT)	CPUID(0xD,0x1).ECX[8] CPUID(0x7,0x0).EBX[25] CPUID(0x14).* CPUID(0xD, 0x8).*	0 or 1	Execution is controlled by IA32_RTIT_CTL. If PT is enabled by XFAM, the guest TD is allowed access to all IA32_RTIT_* MSRs. Otherwise, any access causes #GP(0).
9	U	PK	CPUID(0xD,0x0).EAX[9] CPUID(0xD, 0x9).*	0 or 1	Execution is controlled by CR4.PKE (bit 22). If PK is disabled by XFAM, the guest TD is disallowed from setting CR4.PKE. An attempt to set this bit causes a #GP(0).
10	S	ENQCMD (PASID)	CPUID(0xD,0x1).ECX[10] CPUID(0xD, 0xA).*	0	Execution is controlled by IA32_PASID MSR. There is no direct I/O from guest TDs. ENQCMD and ENQCMDs from the guest TD are not supported and cause a #UD. Access to IA32_PASID causes a #GP(0).
12:11	S	CET	CPUID(0xD,0x1).ECX[12:11] CPUID(0xD, 0xB).* CPUID(0xD, 0xC).*	00 or 11	Execution is controlled by CR4.CET (bit 23). If CET is disabled by XFAM, the guest TD is disallowed from setting CR4.CET. An attempt to set this bit causes a #GP(0).

<sup>8</sup> An extended feature controlled by bits N:M is available if all bits in the range N:M returned by CPUID are set to 1.

Bits	U/S	Feature	Enumeration <sup>8</sup>	XFAM Value	Description
13	S	HDC	CPUID(0xD,0x1).ECX[13] CPUID(0xD, 0xD).*	0	Hardware Duty Cycle is controlled by package-scope IA32_PKG_HDC_CTL and LP-scope IA32_PM_CTL1 MSRs. HDC is disabled. Any guest TD access to the above MSRs causes a #VE.
14	S	ULI	CPUID(0xD,0x1).ECX[14] CPUID(0x7,0x0).EDX[5] CPUID(0xD, 0xE).*	0 or 1	Execution is controlled by CR4.UINT (bit 25). If ULI is disabled by XFAM, then: <ul style="list-style-type: none"> <li>The guest TD is disallowed from setting CR4.ULI. An attempt to set this bit causes a #GP(0).</li> <li>The guest TD is disallowed access to all IA32_UINT_* MSRs. Any access causes a #GP(0).</li> </ul>
15	S	LBR	CPUID(0xD,0x1).ECX[15] CPUID(0x7,0x0).EDX[19] CPUID(0xD, 0xF).* CPUID(0x1C).*	0 or 1	Execution is controlled by IA32_LBR_CTL. If LBR is disabled by XFAM, the guest TD is disallowed access to all IA32_LBR_* MSRs. Any access causes a #GP(0).
16	S	HWP	CPUID(0xD,0x1).ECX[16] CPUID(0xD, 0x10).*	0	Execution of Hardware-Controlled Performance State is controlled by IA32_HWP MSRs. This feature is disabled. Access to any of the above MSRs causes a #VE.
18:17	U	AMX	CPUID(0xD,0x0).EAX[18:17] CPUID(0xD, 0x11).* CPUID(0xD, 0x12).*	00 or 11	Advanced Matrix Extensions (AMX) is directly controlled by XCRO.

## 9.5. CR Handling

### 9.5.1. CR0

- 5 Intel SDM, Vol. 3, 2.5 Control Registers
- Intel SDM, Vol. 3, 23.8 Restrictions on VMX Operation
- Intel SDM, Vol. 3, 24.6.6 Guest/Host Masks and Read Shadows for CR0 and CR4
- Intel SDM, Vol. 3, 25.6 Unrestricted Guests

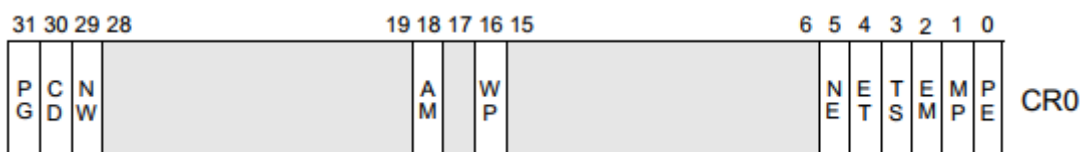


Figure 9.2: CR0

10 From the guest TD’s point of view, as virtualized by the Intel TDX module, CR0 bits PE (0) and NE (5) are always set to 1, and bits NW (29) and CD (30) are always cleared to 0.

Guest TD writes to CR0 are handled by the Intel TDX module as follows:

- Writes to CR0 that are architecturally illegal (such as attempts to set bits that must be 0), or writes to CR0 that set architecturally illegal bit combinations, result in a #GP(0).
- 15 • Writes to CR0 that are architecturally illegal, but not permitted by the TDX architecture (such as clearing CR0.CD) result in a #VE.
- Other writes are allowed.

## 9.5.2. CR4

### Intel SDM, Vol. 3, 24.6.6 Guest/Host Masks and Read Shadows for CR0 and CR4

If a CPU feature is not enabled for the guest TD, the guest TD's attempt to set the corresponding CR4 bit can result in a #GP(0):

- 5 1. Depending on the TD's XFAM, guest TD modification of CR4 bits PKE (22), CET (23) and UINT (25) is prevented. Any guest TD attempt to change those bits results in a #GP(0).
  2. If the TD's ATTRIBUTES.KL is 0, guest TD attempts to set bit KL (19) results in a #GP(0).
  3. If the TD's ATTRIBUTES.PKS is 0, guest TD attempts to set bit PKS (24) results in a #GP(0). See 9.13 below.
  4. If the TD's ATTRIBUTES.PERFMON is 0, guest TD attempts to set bit PCE (8) results in a #GP(0). See 13.2.
- 10 In addition, any guest TD attempts to modify any of the architecturally reserved CR4 bits, or to set architectural-illegal bit combinations, can result in a #GP(0).

From the guest TD's point of view, the following bits are virtualized as fixed by Intel TDX module. Guest TD attempts to modify their values result in a #VE:

- CR4 bit MCE (6) is fixed to 1.
- 15 • CR4 bits VMXE (13) and SMXE (14) are fixed to 0.

## 9.6. MSR Handling

### 9.6.1. Overview

From the guest TD's point of view, as virtualized by the Intel TDX module, MSRs are divided into the following categories:

- MSRs that are context-switched on TD entry and exit – guest TD access to such MSRs may be full, partial or none
- 20 • MSRs that are not context-switched, but guest TD access is read-only
- MSRs that are not context-switched, and are inaccessible to the guest TD

MSR behavior can be either fixed or dependent on the TD configuration via the XFAM, ATTRIBUTES and CPUID configuration parameters. The host VMM has no direct interface to configure specific MSR behavior (e.g., it cannot set a specific MSR to TD exit on write). Instead, guest TD access violations to MSRs can cause a #GP(0) in most cases where the MSR is enumerated as inaccessible by the Intel TDX module via CPUID virtualization. In other cases, guest TD access violations to MSRs can cause a #VE. A guest TD that wishes to access an MSR that is not allowed by the Intel TDX module should do so via explicit requests from the host VMM using TDCALL(TDG.VP.VMCALL).

A detailed list of MSR virtualization is provided in 16.1.

## 9.7. CPUID Virtualization

### 9.7.1. CPUID Configuration by the Host VMM

For some CPUID leaves and sub-leaves, the virtualized bit fields of CPUID return values (in guest EAX/EBX/ECX/EDX) are configurable by the host VMM. For such cases, the Intel TDX module architecture defines two virtualization types:

**Table 9.4: Host VMM Configurable CPUID Field Virtualization**

CPUID Field Virtualization	Description	Comments
<b>As Configured</b>	Bit fields for which the host VMM configures the value seen by the guest TD. Configuration is done on TDH.MNG.INIT.	
<b>As Configured (if Native)</b>	Bit fields for which the host VMM configures the value such that the guest TD either sees their native value or a value of 0. Configuration is done on TDH.MNG.INIT.	If a CPUID bit enumerates a CPU feature, and the feature is natively supported, then the feature can either be allowed by the host VMM, or it will be effectively deprecated for the guest TD.

The above CPUID fields can be specified by the host VMM at guest TD initialization time TDH.MNG.INIT using the TD\_PARAMS input structure of TDH.MNG.INIT. TDH.MNG.INIT is described in 20.2.15, and its input TD\_PARAMS structure is described in 18.2. Configuration is further classified as follows:

**Table 9.5: CPUID Configuration by the TD\_PARAMS Input of TDH.MNG.INIT**

TD_PARAMS Section	Description
<b>CPUID_CONFIG</b>	Bit fields configurable directly based on a configuration table
<b>XFAM</b>	Bit fields configurable based on the guest TD's XFAM XFAM control of extended features virtualization is described in 9.4.
<b>ATTRIBUTES</b>	Bit fields configurable based on the guest TD's ATTRIBUTES
<b>Other</b>	Bits fields configurable based on some other field of TD_PARAMS

A detailed list of CPUID virtualization is provided in 16.2. For any valid CPUID leaf / sub-leaf combination that is not listed, the Intel TDX module injects a #VE.

The host VMM should always consult the list of directly configurable CPUID leaves and sub-leaves, as enumerated by TDH.SYS.INFO, described in 12.1.3.3.

### 9.7.2. Unconditional #VE for all CPUID Leaves and Sub-Leaves

The guest TD may use the TDG.VP.CPUIDVE.SET to toggle on or off the unconditional injection of #VE on all CPUID leaves and sub-leaves. That can be done in supervisor mode (CPL == 0) and/or user mode (CPL > 0). For example, this enables the TD OS to control CPUID as seen by drivers or by user-level code. TDG.VP.CPUIDVE.SET is described in 20.3.5.

## 9.8. Interrupt Handling and APIC Virtualization

Intel SDM, Vol. 3, 24.6.8 Controls for APIC Virtualization  
Intel SDM, Vol. 3, 29 APIC Virtualization and Virtual Interrupts

### 9.8.1. Virtual APIC Mode

- Guest TDs must use virtualized x2APIC mode. xAPIC mode (using memory mapped APIC access) is not allowed.
- Guest TD attempts to RDMSR or WRMSR the IA32\_APIC\_BASE MSR cause a #VE to the guest TD. The guest TD cannot disable the APIC.

### 9.8.2. Virtual APIC Access by Guest TD

Intel SDM, Vol. 3, 29.5 Virtualizing MSR-Based APIC Access

Guest TDs are allowed access to a subset of the virtual APIC registers, which are virtualized by the CPU as described in [Intel SDM, Vol. 3, 29.5]. Access to other registers can cause a #VE. The guest TD is expected to use a software protocol over TDG.VP.VMCALL to request such operations from the host VMM.

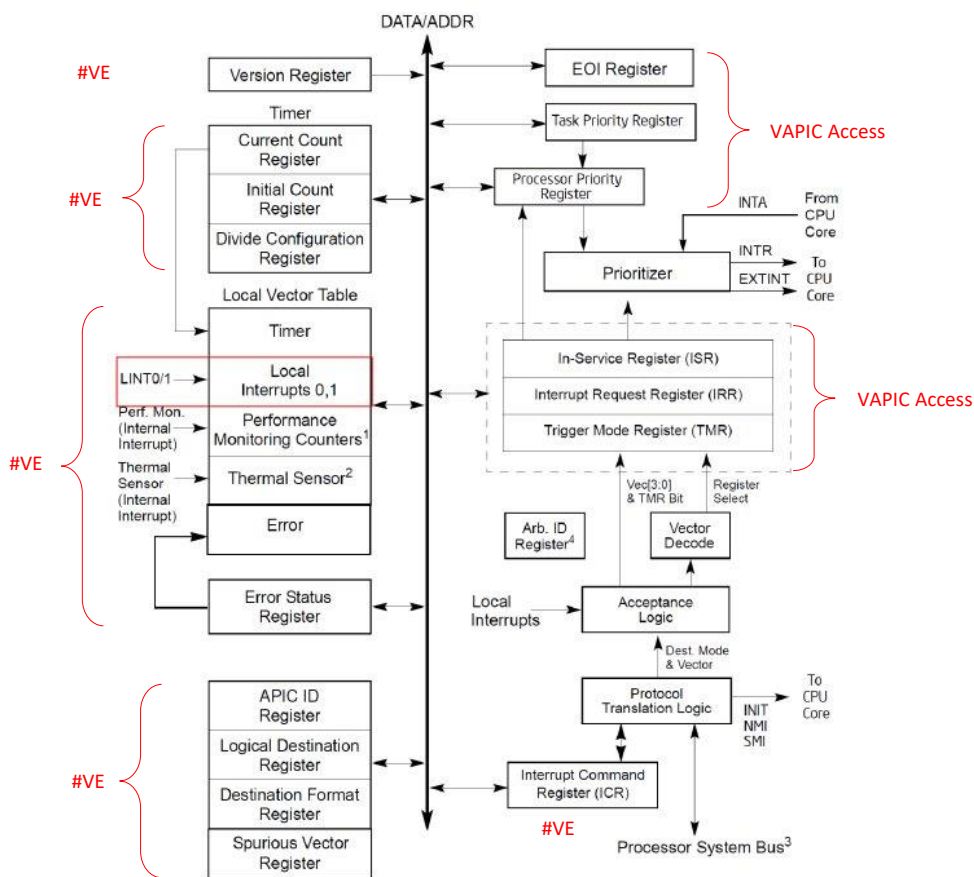


Figure 9.3: Virtual APIC Access by Guest TD

Table 9.6: x2APIC MSRs Access

MSR Range	MSR Name(s)	Description	Operation
0x802	IA32_X2APIC_APICID	APIC ID	#VE
0x803	IA32_X2APIC_VERSION	APIC version	#VE
0x80D	IA32_X2APIC_LDR	Local destination register	#VE
0x80F	IA32_X2APIC_SIVR	Spurious interrupt vector	#VE
0x828	IA32_X2APIC_ESR	Error status	#VE
0x830	IA32_X2APIC_ICR	Interrupt command	#VE
0x82F, 0x837-0x832, 0x83A	IA32_X2APIC_LVT_*	Local vector table registers	#VE
0x838, 0x839, 0x83E	IA32_X2APIC_*_COUNT, IA32_X2APIC_DCR	APIC timer registers	#VE
0x801-0x800, 0x807-0x804, 0x82E-0x829, 0x831, 0x8FF-0x840	Reserved		#GP(0)
Other MSR in the range 0x8FF-0x800			Access to VAPIC page (see [Intel SDM, Vol. 3, 29.5])

### 9.8.3. Posted Interrupts

#### Intel SDM, Vol. 3, 29.6 Posted-Interrupt Processing

Non-NMI interrupt injection into the guest TD by the host VMM or the IOMMU can be done through the posted-interrupt mechanism. If there are pending interrupts in the posted-interrupt descriptor (PID), the VMM can post a self IPI with the notify vector prior to TD entry.

- The posted-interrupt descriptor (PID) resides in a shared page, directly accessible by the host VMM. The VMM must set the TD VMCS's "posted-interrupt descriptor address" control (using the TDH.VP.WR function) to the PA and shared HKID of the posted-interrupt descriptor.
- The host VMM must set the TD VMCS's "posted-interrupt notification vector" control using the TDH.VP.WR function.
- To post pending interrupts in the PID, the host VMM can generate a self IPI with the notification vector prior to TD entry.

When a posted-interrupt notification vector is recognized in TDX non-root mode, the CPU processes the posted-interrupt descriptor as described in the [Intel SDM].

If needed, the guest TD may use a software protocol over TDCALL(TDG.VP.VMCALL) to ask the VMM to stop interrupt delivery through the PID.

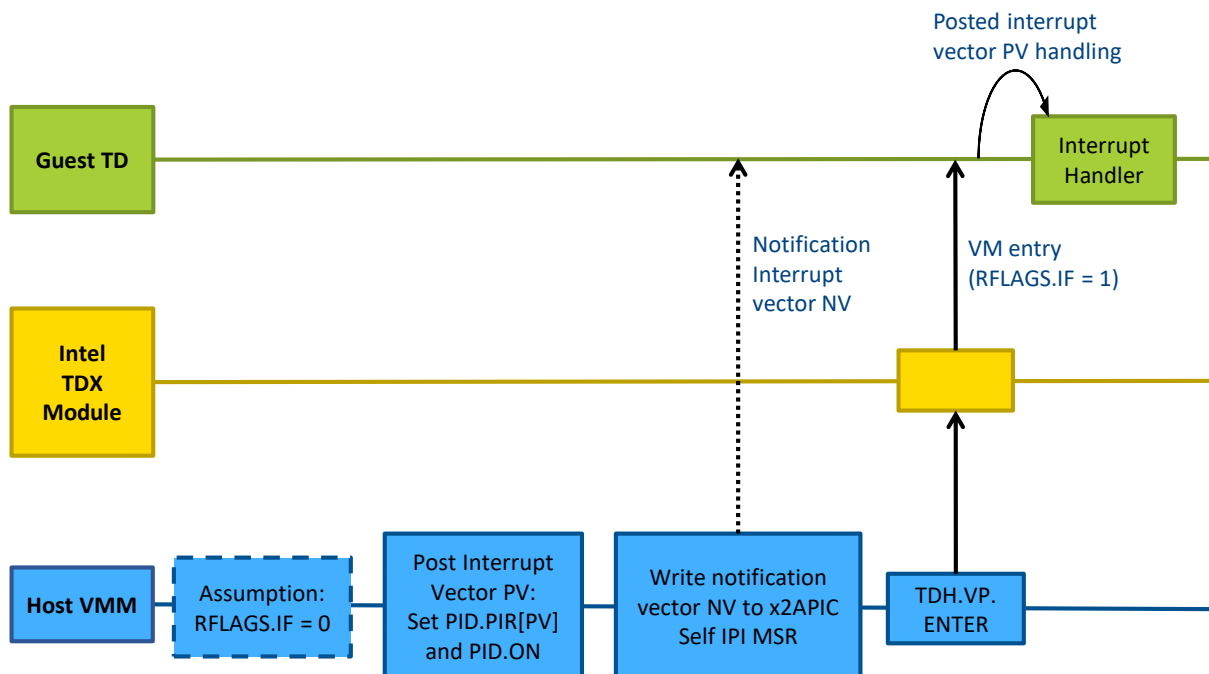


Figure 9.4: Typical Sequence for Posted Interrupt Injection to the Current LP

### 9.8.4. Cross-TD-VCPU IPI

To perform a cross-VCPU IPI, the guest TD ILP should request an operation from the host VMM using TDG.VP.VMCALL. The VMM can then inject an interrupt into the guest TD's RLPs using the posted interrupt mechanism, as described in 9.8.3 above. This is an untrusted operation; thus, the TD needs to track its completion.

### 9.8.5. Virtual NMI Injection

The host VMM can request the Intel TDX module to inject an NMI into a guest TD VCPU using the TDH.VP.WR function, by setting the PEND\_NMI TDVPS field to 1. This can be done only when the VCPU is not active (a VCPU can be associated with at most one LP). Following that, the host VMM can call TDH.VP. ENTER to run the VCPU; the Intel TDX module will attempt to inject the NMI as soon as possible.

The host VMM can use TDH.VP.RD to read PEND\_NMI and get the status of NMI injection. A value of 0 indicates that NMI has been injected into the guest TD VCPU. The host VMM also may choose to clear PEND\_NMI before it is injected.



## 9.9. Virtualization Exception (#VE)

Intel SDM, Vol. 3, 24.9.4 Information for VM Exits Due to Instruction Execution

Intel SDM, Vol. 3, 25.5.6 Virtualization Exceptions

Intel SDM, Vol. 3, 27.2.5 Information for VM Exits Due to Instruction Execution

- 5 The Intel TDX module extends the VMX architectural usage of #VE to para-virtualize memory address translation. It injects #VE into the guest TD in multiple cases where an operation is not allowed by TDX, but an architectural exception is not applicable (e.g., #GP(0)). Such cases include disallowed instruction executions, disallowed MSR accesses, many CPUID leaves, etc.

10 The intended usage is for the TDX-enlightened guest TD OS to have a #VE handler. By analyzing the #VE information, the handler would be able to virtualize the requested operation for non-enlightened parts of the guest TD – e.g. drivers and applications.

### 9.9.1. Virtualization Exception Information

The **virtualization-exception information area** (VE\_INFO) is maintained as part of TDVPS. It is not intended to be directly accessible to the guest TD. Instead, the information can be retrieved using the **TDG.VP.VEINFO.GET** function (see 20.3.5).

- 15 This is a simple way to help assure the availability and privacy of this area.

**Table 9.7: Virtualization Exception Information Area (VE\_INFO), based on [Intel SDM, Vol. 3, Table 25-1]**

Section	Field	Offset (Bytes)	Size (Bytes)	Description
Architectural	EXIT_REASON	0	4	The value that would have been saved into the VMCS as an exit reason if a VM exit had occurred instead of the virtualization exception.
	VALID	4	4	0 indicates that VE_INFO has no valid contents. The CPU and the Intel TDX module will not update VE_INFO if VALID is not 0. After updating VE_INFO, the CPU and the Intel TDX module write 0xFFFFFFFF to the VALID field.
	EXIT_QUALIFICATION	8	8	The value that would have been saved into the VMCS as an exit qualification if a VM exit had occurred instead of the virtualization exception.
	GLA	16	8	The value that would have been saved into the VMCS as a guest-linear address if a VM exit had occurred instead of the virtualization exception.
	GPA	24	8	The value that would have been saved into the VMCS as a guest-physical address if a VM exit had occurred instead of the virtualization exception.
	EPTP_INDEX	32	2	The current value of the EPTP index VM-execution control
Non-Architectural	INSTRUCTION_LENGTH	Non-arch.	4	The 32-bit value that would have been saved into the VMCS as VM-exit instruction length if a legacy VM exit had occurred instead of the virtualization exception.
	INSTRUCTION_INFORMATION	Non-arch.	4	The 32-bit value that would have been saved into the VMCS as VM-exit instruction information if a legacy VM exit had occurred instead of the virtualization exception.

20 The architectural section format for VE\_INFO is as defined in the [Intel SDM], and it is used directly by the CPU when it injects a #VE (see 9.9.2 below). VE\_INFO can also be used for #VE injected by the Intel TDX module. Some VE\_INFO fields are applicable only for some exit reasons.

VE\_INFO.VALID is initialized to 0, and it is set to 0xFFFFFFFF when a #VE is injected to the guest TD. When handling a #VE, the guest TD retrieves the #VE information using the **TDG.VP.VEINFO.GET** function (see 20.3.5).

TDG.VP.VEINFO.GET checks that VE\_INFO.VALID is 0xFFFFFFFF. After reading the information, it sets VE\_INFO.VALID to 0.

### 9.9.2. #VE Injection by the CPU due to EPT Violations

#VE is enabled unconditionally for TDX non-root operation. The Intel TDX module sets the TD VMCS **EPT-violation #VE** VM-execution control to 1.

For shared memory accesses (i.e., when GPA.SHARED == 1), as with legacy VMX, the VMM can choose which pages are eligible for #VE mutation based on the value of the Shared EPTE bit 63.

For private memory accesses (GPA.SHARED == 0), an EPT Violation causes a TD Exit in most cases (an exception to this is described in 9.10.1 below). The Intel TDX module sets the Suppress VE bit (63) of all Secure EPT entries.

### 9.9.3. #VE Injected by the Intel TDX Module

#VE may be injected by the Intel TDX module as a result of guest TD execution of a disallowed instruction (see 9.3 above), a disallowed MSR access (see 9.6 above), or CPUID virtualization (see 9.7 above).

If, when attempting to inject a #VE, the Intel TDX module discovers that the guest TD has not yet retrieved the information for a previous #VE (i.e., VE\_INFO.VALID is not 0), the TDX module injects a #DF into the guest TD to indicate a #VE overrun.

## 9.10. Secure and Shared Extended Page Tables (EPTs)

EPT is enabled in TDX non-root mode. TDX non-root mode uses two EPTs: Secure EPT, and Shared EPT.

EPT level is the same for both Secure and Shared EPT. If the guest TD's GPA width is greater than 48 bits (TDCS.GPAW is 1), then 5-level EPT trees are used. Otherwise, 4-level EPT trees can be used.

For further Secure EPT details, refer to Chapter 7.

EPT violations and misconfigurations generally cause a TD Exit, except for the cases described below.

### 9.10.1. GPAW-Related EPT Violations

GPA bits higher than the SHARED bit are considered reserved and must be 0. Address translation with any of the reserved bits set to 1 cause a #PF with PFEC (Page Fault Error Code) RSVD bit set.

### 9.10.2. EPT Violation Mutated into #VE (Shared EPT Only)

The host VMM can configure the Shared EPT to deliver EPT violations to the guest TD as #VE exceptions for usages such as MMIO, as described in 9.9 above.

## 9.11. Prevention of TD-Induced Denial of Service

VMs, including TDs, can exploit Intel ISA characteristics to cause performance and functional Denial of Service (DOS) to the VMM. The Intel architecture has several mechanisms that help prevent such DOS cases. This section describes how those mechanisms are used in the context of TDX.

The guest TD OS can enable debug exception traps due to bus locks by setting IA32\_DEBUGCTL.BUS\_LOCK\_DETECT bit (2), which is disabled by default. When enabled, the feature works identically to how it functions in legacy VMX non-root mode or in non-VMX mode. The IA32\_DEBUGCTL MSR and DR6 are part of the state that is saved and restored on VM exit and VM entry, respectively. If the delivery of #DB was pre-empted by a trap-like VM exit, then the pending debug exceptions (including due to BUS\_LOCK\_DETECT if pending) are saved in TD VMCS and restored on subsequent VM Entry. For fault-like VM Exit due to conditions such as EPT violation and EPT misconfiguration that are encountered during execution of an instruction, there is no pending debug exception recorded, including the bus lock debug exception.

### 9.11.1. Bus Lock TD Exit

Bus lock TD exit is disabled by default. The host VMM can enable the TD VMCS "bus-lock detection" VM execution control using the TDH.VP.WR function. If enabled, the processor generates a bus lock VM exit (exit reason 74) following execution

of an instruction (or an iteration of a REP prefixed instruction) if the processor detects that one or more bus locks were caused by the instruction that was executed. The Intel TDX module then completes a TD exit.

- If an instruction (or an iteration of a REP prefixed string instruction) that successfully caused a bus lock subsequently faults, then a bus lock VM exit (exit reason 74) occurs on the instruction boundary following delivery of the fault (including any nested faults).
- If delivery of bus lock VM exit was pre-empted by a higher priority VM exit (e.g., EPT Misconfiguration, EPT Violation, etc.), then a “bus lock detected” notification bit (bit 26) is set in the exit reason to indicate that one or more bus locks were successfully acquired prior to this VM Exit. The Intel TDX module reflects this to the host VMM on TD exit.
- If the delivery of bus lock VM exit was pre-empted by an EPT Violation and that EPT Violation was mutated into a #VE, then the bus lock VM exit is pending at the EOM of the delivery of the #VE.

### 9.11.2. Notification TD Exit

Notification TD exit is disabled by default. The host VMM can write the TD VCMS “notify window” and “notification exiting” execution controls using the TDH.VP.WR function. If enabled and configured, then if the processor detects a no-commit case, the processor causes a notification VM exit (exit reason 75) which the Intel TDX module converts to the TD exit.

The conditions that cause a notification TD exit are the same as those in legacy VMX non-root mode. An example of such a case is the nested #AC exception. If an #AC exception occurs during the delivery of a previous #AC exception, then the CPU may get into an endless loop of #AC without responding to external events.

Bit 0 (VM context invalid) of the exit qualification indicates whether the guest TD context is corrupted and not valid in the TD VMCS. If this bit is set to 1, then it is a non-recoverable situation; thus, the Intel TDX module marks the TD as disabled to help prevent further TD entry. If no TD context corruption occurred (exit qualification bit 0 is cleared to 0), then the TD may be resumed normally.

## 9.12. Time Stamp Counter (TSC)

Intel SDM, Vol. 3, 10.5.4.1	TSC-Deadline Mode
Intel SDM, Vol. 3, 24.6.5	Time-Stamp Counter Offset and Multiplier
Intel SDM, Vol. 3, 25.3	Changes to Instruction Behavior in VMX Non-Root Operation

### 9.12.1. TSC Virtualization

For virtual time stamp counter (TSC) values read by guest TDs, the Intel TDX module is designed to achieve the following:

- Virtual TSC values are consistent among all the TD’s VCPUs at the level supported by the CPU, see below.
- The virtual TSC value for any single VCPU is monotonously incrementing (except roll over from  $2^{64}-1$  to 0).
- The virtual TSC frequency is determined by TD configuration.

The host VMM is required to do the following:

- Set up the same IA32\_TSC\_ADJUST values on all LPs before initializing the Intel TDX module.
- Make sure IA32\_TSC\_ADJUST is not modified from its initial value before calling SEAMCALL.

The Intel TDX module checks the above as part of TDH.VP.ENTER and any other SEAMCALL leaf function that reads TSC.

The virtualized TSC is designed to have the following characteristics:

- The virtual TSC frequency is specified by the host VMM as an input to TDH.MNG.INIT in units of 25MHz – it can be between 40 and 400 (corresponding to a range of 1GHz to 10GHz).
- The virtual TSC starts counting from 0 at TDH.MNG.INIT time.
- TSC parameters are enumerated to the guest TD by CPUID(0x15).
- Guest TDs are not allowed to modify the TSC. WRMSR attempts of IA32\_TIME\_STAMP\_COUNTER result in a #VE.
- Guest TDs are not allowed to access IA32\_TSC\_ADJUST because its value is meaningless to them. WRMSR or RDMSR attempts result in a #VE.
- RDTSCP is supported. This instruction returns the contents of the IA32\_TSC\_AUX MSR in RCX. the Intel TDX module allows the guest TD to access that MSR and context-switches it on TD entry and exit as part of the VCPU state in TDVPS.
- Guest TDs are not allowed to access IA32\_TSC\_DEADLINE. WRMSR or RDMSR attempts result in a #VE.

### 9.13. Supervisor Protection Keys (PKS)

By design, guest TD usage of Supervisor Protection Keys (PKS) is controlled by the ATTRIBUTES.PKS bit (see 18.2.1). When PKS is supported by the CPU and ATTRIBUTES.PKS is set to 1, the following features are available to the guest TD:

- CPUID virtualization enumerates PKS availability to the guest TD.
- Guest TDs may enable PKS by setting CR4.PKS flag.
- Guest TDs may access the PKS state using the IA32\_PKRS MSR.

### 9.14. Intel® Total Memory Encryption (Intel® TME) and Multi-Key Total Memory Encryption (MKTME)

Guest TDs may not directly use the Intel TME and MKTME MSRs and the PCONFIG instruction. The Intel TDX module supports para-virtualization of this ISA, as described below.

#### 9.14.1. TME Virtualization

TME is enumerated by CPUID(0x7, 0x0).ECX[13]. The host VMM can configure the virtualization of this bit as enabled or disabled on TDH.MNG.INIT. If enabled, then a guest TD access to the IA32\_TME\_\* MSRs (0x981 – 0x984) causes a #VE, allowing the guest TD's #VE handler to emulate the desired operation. Else, guest TD access to those MSRs causes a #UD.

#### 9.14.2. MKTME Virtualization

MKTME is enumerated by CPUID(0x7, 0x0).EDX[18]. The host VMM can configure the virtualization of this bit as enabled or disabled on TDH.MNG.INIT. If enabled, then the following operations cause a #VE (e.g., the guest TD #VE handler can then communicate with the host VMM over TDG.VP.VMCALL to request the desired operation):

- Guest TD access to the IA32\_MKTME\_PARTITIONING MSR (0x87)
- PCONFIG execution by the guest TD

If the host VMM configured CPUID(0x7, 0x0).EDX[18] virtualized value as 0, then:

- Guest TD access to the IA32\_MKTME\_PARTITIONING MSR (0x87) causes a #GP(0).
- PCONFIG execution by the guest TD causes a #UD.

### 9.15. Other Changes in TDX Non-Root Mode

#### 9.15.1. Tasking

Any task switch results in a VM exit to the Intel TDX module (this is a fixed-1 exit) which then performs a TD exit to the host VMM.

The VMM is expected not to reenter the TD VCPU since this case is non-recoverable; the instruction that caused the task switch (CALL, JMP or IRET) will re-execute and cause another VM exit. If the task switch was incidental to an exception delivery, then the VM entry following TDH.VP.ENTER will reattempt the delivery and cause another task switch VM exit. The expected response from the VMM is to terminate this TD.

#### 9.15.2. PAUSE-Loop Exiting

##### Intel SDM, Vol. 3, 25.1.3 Instructions That Cause VM Exits Conditionally

The host VMM can only set the guest TD's "PAUSE-loop exiting" VM-execution control if the guest TD runs in debug mode (ATTRIBUTES.DEBUG is 1).

"PAUSE-loop exiting" allows the VMM to request an exit if the guest (in ring 0) executes PAUSE in a loop (e.g., busy-wait). This is intended to help avoid cases where a guest thread loops, waiting for another thread that is not currently scheduled by the VMM. However, modern enlightened guests use a VMM-provided service (hypercall) instead of PAUSE loops – this is the expected usage for Intel TDX.

## 10. Measurement and Attestation

### 10.1. TD Measurement

TDs have two types of measurement registers:

- **MRTD** helps provide static measurement of the TD build process and the initial contents of the TD.
- **RTMR** is an array of general-purpose measurement registers made available to the TD software to enable measuring additional logic and data loaded into the TD at run-time.

All TD measurements are reflected in TD attestations.

#### 10.1.1. MRTD: Build-Time Measurement Register

The Intel TDX module measures the TD during the build process. The measurement register TDCS.MRTD is a SHA384 digest of the build process, designed as follows:

- TDH.MNG.INIT begins the process by initializing the digest.
- TDH.MEM.PAGE.ADD adds a TD private page to the TD and inserts its properties (GPA) into the MRTD digest calculation.
- Control structure pages (TDR, TDCX, TDVPR and TDVPX) and Secure EPT pages are not measured.
- For pages whose data contribute to the TD, that data should be included in the TD measurement via TDH.MR.EXTEND. TDH.MR.EXTEND inserts the data contained in those pages and its GPA, in 256-byte chunks, into the digest calculation. If a page will be wiped and initialized by TD code, the loader may opt not to measure the initial contents of the page with TDH.MR.EXTEND.
- The measurement is then completed by TDH.MR.FINALIZE. Once completed, further TDH.MEM.PAGE.ADDs or TDEXTENDs will fail.

MRTD extension by GPA uses a 128B buffer which includes the GPA and the leaf function name for uniqueness.

#### 10.1.2. RTMR: Run-Time Measurement Registers

The RTMR array is initialized to zero on build, and it can be extended at run-time by the guest TD using the TDCALL(TDG.MR.RTMR.EXTEND) leaf. The syntax of the RTMR registers is designed to be similar to that of TPM PCRs, where a register's value after TDG.MR.RTMR.EXTEND(index=i, value=x) is:

```
RTMR[i] = SHA384(RTMR[i] || x);
```

Four RTMR registers are provided.

Typical expected usage is for TPM emulation during guest TD OS secure boot by the VBIOS.

### 10.2. TD Measurement Reporting

TD attestation is initiated from inside the TD by calling TDG.MR.REPORT and specifying a REPORTDATA value. TDG.MR.REPORT creates a TDREPORT\_STRUCT structure containing the TD measurements, initial configuration of the TD that was locked at finalization (TDH.MR.FINALIZE), the Intel TDX module measurements, and the REPORTDATA value. TDREPORT\_STRUCT structure is detailed in 18.5, and TDG.MR.REPORT is detailed in 20.3.3.

TDREPORT\_STRUCT is HMAC'ed using an HMAC key that is designed to be accessible only to the CPU. This helps protect the integrity of the structure and, by design, can only be verified on the local platform via the SGX ENCLU(EVERIFYREPORT2) instruction. By design, TDREPORT\_STRUCT cannot be verified off platform; it first must be converted into signed Quotes, as described in 10.3 below.

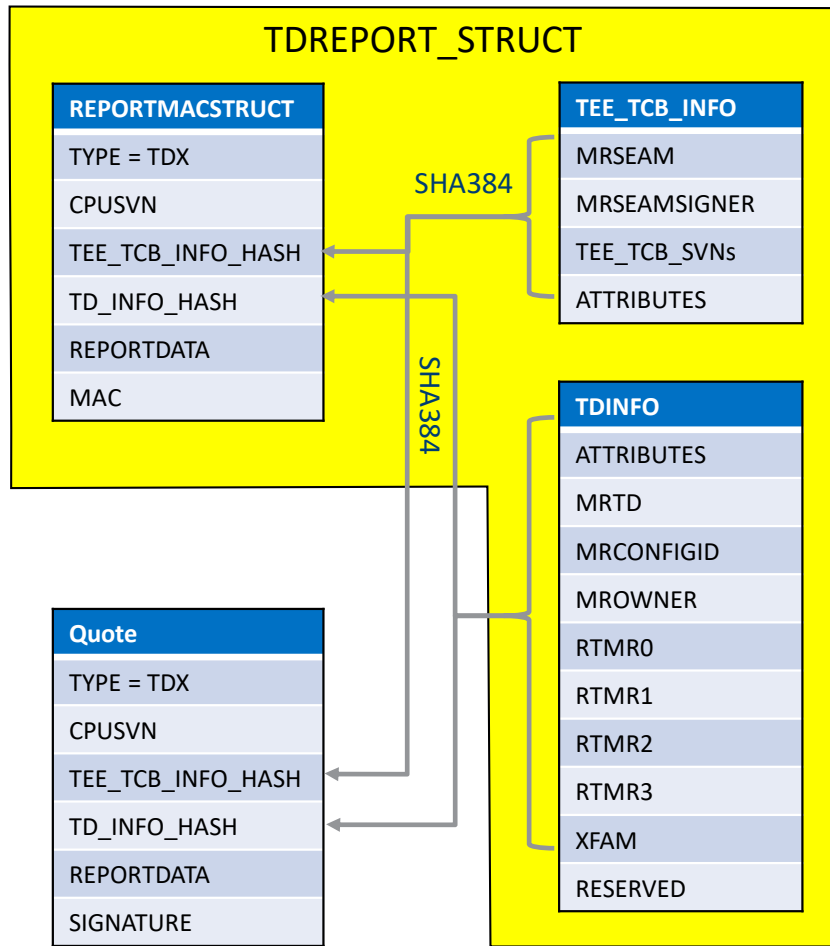


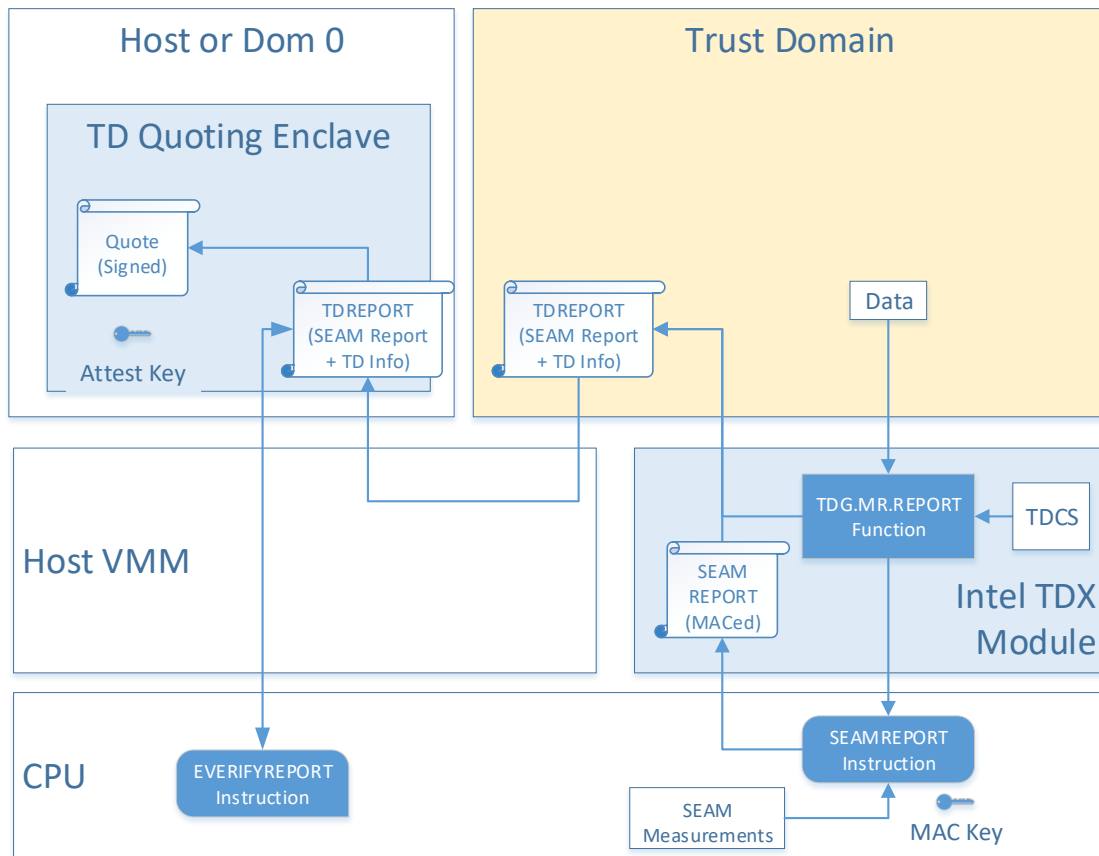
Figure 10.1: TDX Measurement Reporting

### 10.3. TD Measurement Quoting

To create a remotely verifiable attestation, the TDREPORT\_STRUCT should be converted into a Quote signed by a certified Quote signing key.

#### 10.3.1. Intel SGX-Based Attestation

The Intel SGX attestation architecture is designed to provide facilities for multiple Quoting Enclaves from multiple providers. This is intended to allow the host to instantiate a Quoting Enclave for Intel SGX attestations and another Quoting Enclave for TD attestation without interference — i.e., each provider can supply its own quoting enclave, and the quoting enclave for Intel SGX and for Intel TDX may be separate; the design does not require the quoting enclave to run inside the TD.



**Figure 10.2: High-Level View of the Intel SGX-Based TD Attestation**

Quote generation using a quoting enclave is typically performed as follows:

1. Guest TD invokes the TDCALL(TDG.MR.REPORT) function.
- 5 2. The Intel TDX module uses the SEAMREPORT instruction to create MAC'ed TDREPORT\_STRUCT with the Intel TDX module measurements from CPU and TD measurements from TDCS.
3. Guest TD uses TDCALL(TDG.VP.VMCALL) to request that TDREPORT\_STRUCT be converted into Quote.
4. The TD Quoting enclave uses EVERIFYREPORT2 to check the TDREPORT\_STRUCT. This allows the Quoting Enclave to check the report without requiring direct access to the CPU's HMAC key. Once the integrity of the TDREPORT\_STRUCT has been verified, the TD Quoting Enclave signs the TDREPORT\_STRUCT body with an ECDSA 384 signing key.
- 10

#### 10.4. Quote Signing Key

The Intel SGX infrastructure provides primitives and a certificate infrastructure to allow Quoting Enclaves to certify their own Quoting Keys. The Intel SGX Provisioning Certification Enclave (PCE) uses an Intel-Certified ECDSA-256 signing key to issue certificates to Quoting Enclaves for their attestation keys. Intel offers a service to allow third parties to download these certificates.

- 15

Typically, on first launch, the TD Quoting Enclave generates a random ECDSA 384-bit quoting key. It then contacts the Provisioning Certification Enclave which uses its signing key to sign the new quoting key's public key.

Note that the TD Quoting Enclave uses an ECDSA 384 bit key, while the PCE certifies it with an ECDSA-256 key. This is due to limitations of the SPR platform.

- 20

#### 10.5. TCB Recovery

The Intel TDX architecture has several levels of TCB:

- CPU HW level, which includes microcode patch, ACMs and PFAT
- Intel TDX module software
- 25 • Attestation Enclaves which include the TD Quoting Enclave and Provisioning Certification Enclave

The TCB Recovery story is different for each level. The existing SGX TCB Recovery model for CPU level items applies in the same way with TDX and SGX. The model requires a restart of the platform to take effect. The Intel TDX module can be unloaded and reloaded to reflect an upgraded Intel TDX module. The enclaves can be upgraded at run-time, but if the PCE is upgraded, the design requires a new certificate to be downloaded.



## 11.I/O Support

This chapter specifies the Intel TDX I/O model.

### 11.1. Overview

Intel TDX architecture does not prescribe a specific software convention to perform I/O from the guest TD. Guest TD providers have many choices to provide I/O to the guest. The common I/O models are emulated devices, para-virtualized devices, SRIOV devices and Direct Device assignments. Guest TD providers can choose to offer the combinations of I/O models based on the workload and use case. To virtualize MMIO, the following options can be utilized:

- **Para-Virtualized Drivers** can replace MMIO accesses with TDG.VP.VMCALL to invoke VMM provided MMIO emulation functions.
- **MMIO Emulation by #VE Handlers** can use non-para-virtualized drivers in the guest TD, with the emulation performed by the #VE handler. EPT and #VE mechanisms can be used to reflect violations to the #VE handler in the guest TD on access to virtual MMIO ranges. These violations can invoke VMM-provided MMIO emulation functions through TDG.VP.VMCALL. In this model, the #VE handler is expected to emulate the faulting instruction in the guest TD.

### 11.2. Paravirtualized I/O

Para-virtualization (e.g., using virtio APIs in KVM, etc.) helps provide a mechanism for the guest TD to use devices on the host machine that are owned and managed by the VMM. The guest TD drivers can use the TDG.VP.VMCALL function to invoke the functions provided by the VMM to perform I/O. The TD drivers must ensure that the data buffers passed to/from functions invoked using TDG.VP.VMCALL are placed in the TD's shared memory space.

### 11.3. MMIO Emulation and Emulated Devices

An alternate technique that the guest TD may employ to invoke VMM functions for I/O is to emulate MMIO access from legacy device drivers. To support this use model, the VMM may enable reflection of EPT violation to emulated MMIO guest physical addresses as virtualization exceptions (#VE), as described in 9.9. A #VE exception handler in the guest TD OS can emulate the instruction causing the #VE, and as part of the emulation, it can invoke the I/O functions provided by the VMM using TDCALL(TDG.VP.VMCALL). Similar to the paravirtualized I/O model, the TD software must ensure that the data buffers passed to/from functions invoked using TDG.VP.VMCALL are placed in the TD's shared memory space.

### 11.4. Direct Device Assignment (DDA) and SRIOV

The VMM may assign devices directly to the guest TD. The addresses mapping the MMIO resources of such devices must be mapped in the shared memory space of the TD. When submitting data buffers to these devices, the guest TD must locate the data buffers in shared memory such that the directly assigned device can move data in/out of such buffers using DMA. The data buffers placed in shared memory should be programmed in IOMMU page tables.

The SRIOV virtual function devices assigned to guest TD also follow the DDA guidelines stated above with respect to MMIO and data buffers. The control plane of the virtual function would use the soft or hard mechanism to configure the virtual functions:

- The soft mechanism would use para-virtualization to configure the virtual function.
- The hard mechanism would use hardware mailboxes accessed using MMIO in the shared memory region.

### 11.5. IOMMU – DMA Remapping

The IOMMU uses the VT-d remapping tables to translate GPA in the DMA from device to an HPA. The VT-d remapping tables will reflect the mapping of memory used by I/O devices in the guest TD. The programming of the VT-d remapping tables and management will be done by the VMM.

Only shared GPA memory should be mapped in the VT-d tables:

- If the result of the translation results in a physical address with a TD private key ID, then the IOMMU will abort the transaction and report a VT-d DMA remapping failure.

- If the GPA in the transaction that is input to the IOMMU is private (SHARED bit is 0), then the IOMMU may abort the transaction and report a VT-d DMA remapping failure, even if the translated physical address is with a non-private HKID. This is intended to support debug wherein a TD or VMM could program a bad GPA into the device.

### **11.6. Shared Virtual Memory (SVM)**

- 5 Shared Virtual Memory enables applications to access buffers directly accessed by the devices. The VT-d tables help provide the mechanism to map application buffers using the first-level and second-level page tables to provide applications access to the same memory accessed by devices.

SVM should be avoided because VT-d tables can only map shared memory.

## 12. Intel TDX Module Lifecycle: Enumeration, Initialization and Shutdown

This chapter discusses the design of the Intel TDX module life cycle: how its capabilities are enumerated by the host VMM, how it is initialized, how it is configured and how it is shut down.

### 12.1. Overview

#### 5 12.1.1. Initialization and Configuration Flow

The Intel TDX module initialization and configuration typically happens as described below:

**Table 12.1: Typical Intel TDX Module Enumeration, Initialization and Configuration Sequence**

	Step	Intel TDX Function	Description
1	CMR Configuration & Checking	N/A	BIOS configures convertible memory regions (CMRs); MCHECK checks them and securely stores the information.
2	Intel TDX Module Loading	N/A	OS/VMM launches the SEAMLDR ACM which loads the Intel TDX module.
3	Global Initialization	TDH.SYS.INIT	The host VMM calls TDH.SYS.INIT once. This function performs global initialization of the Intel TDX module.
4	LP Initialization	TDH.SYS.LP.INIT (each LP)	The host VMM calls TDH.SYS.LP.INIT once on each logical processor. This function performs LP-scope, core-scope and package-scope initialization, checking and configuration of the platform and the Intel TDX module.
5	Enumeration	TDH.SYS.INFO	The host VMM calls TDH.SYS.INFO to retrieve Intel TDX module information and convertible memory (CMR) information.
6	Global Configuration	TDH.SYS.CONFIG	The host VMM calls TDH.SYS.CONFIG once, providing a set of configuration parameters including a table of TDMRs. This function performs global configuration of the Intel TDX module.
7	Cache Flush	N/A	The host VMM flushes any MODIFIED cache lines that may exist for the PAMT ranges, using, e.g., TDWBINVD on each package.
8	Key Configuration	TDH.SYS.KEY.CONFIG (each package)	The host VMM calls TDH.SYS.KEY.CONFIG once on each package. This function configures the Intel TDX global private key on the hardware.
9	Intel TDX module is available	Any	Once TDH.SYS.KEY.CONFIG has executed successfully on all packages, any Intel TDX function may be executed on any LP.
10	TDMR and PAMT Initialization	TDH.SYS.TDMR.INIT (multiple)	The host VMM calls TDH.SYS.TDMR.INIT in a loop, gradually initializing the PAMT structure for each TDMR.
11	Memory is available	Any	Once each 1GB block of TDMR has been initialized by TDH.SYS.TDMR.INIT, it can be used to hold TD-private pages.

#### 12.1.2. Intel TDX Module Lifecycle State Machine

10 The Intel TDX lifecycle state machine helps track the module's life cycle through the initialization sequence and shutdown.

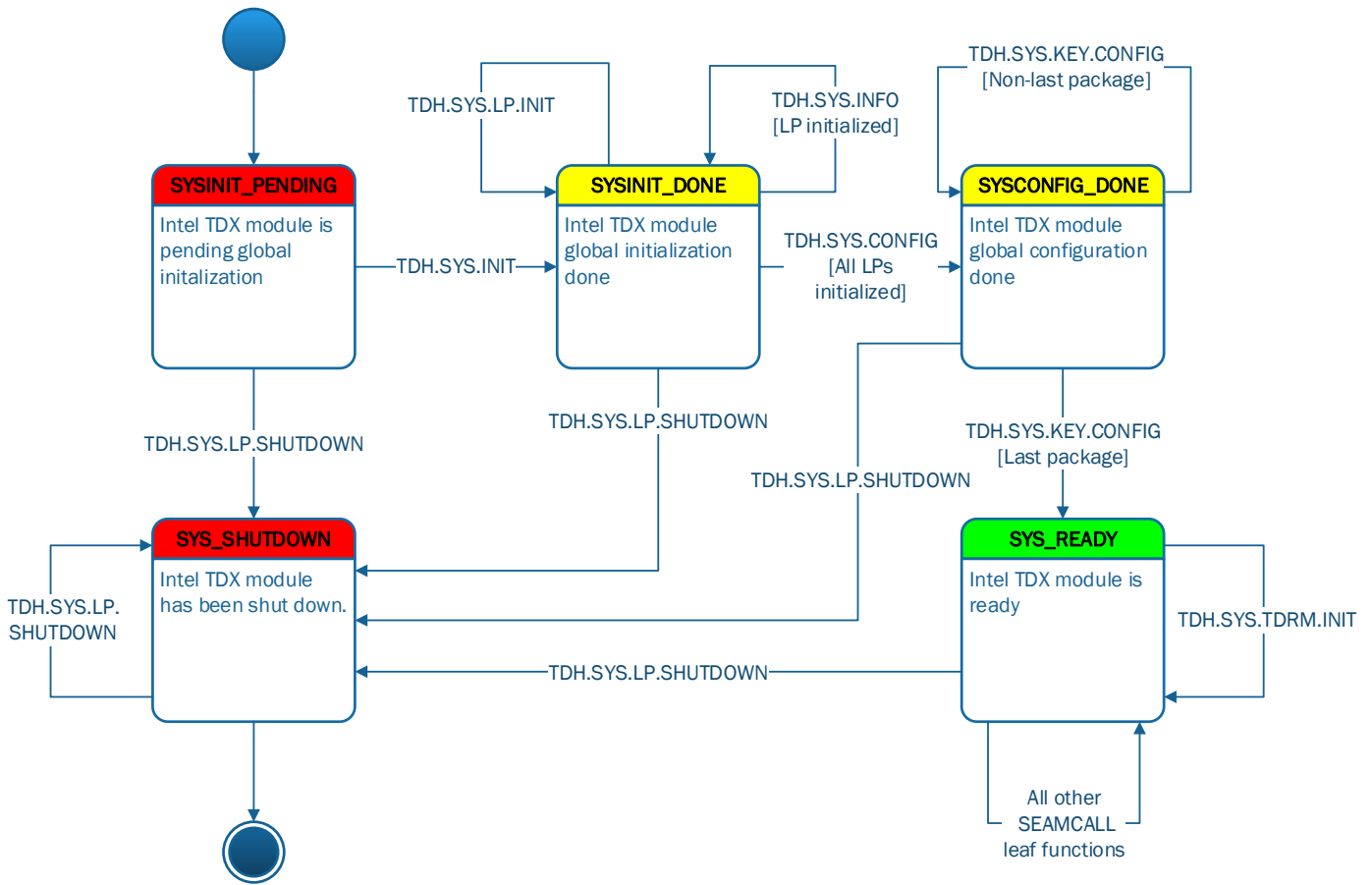


Figure 12.1: Intel TDX Module Lifecycle State Machine

Table 12.2: Intel TDX Module Lifecycle States

State Name	Description	Allowed SEAMCALL Leaf Functions
<b>SYSINIT_PENDING</b>	TDH.SYS.INIT has not been called yet.	TDH.SYS.INIT TDH.SYS.SHTDOWNLP
<b>SYSINIT_DONE</b>	TDH.SYS.INIT has completed successfully. TDH.SYS.LP.INIT must be called on each LP.	TDH.SYS.LP.INIT TDH.SYS.INFO (if current LP has been initialized) TDH.SYS.CONFIG (if all LPs have been initialized) TDH.SYS.SHTDOWNLP
<b>SYSCONFIG_DONE</b>	TDH.SYS.CONFIG has completed successfully. TDH.MNG.KEY.CONFIG must be called on each package.	TDH.SYS.KEY.CONFIG TDH.SYS.INFO TDH.SYS.SHTDOWNLP
<b>SYS_READY</b>	The Intel TDX module is ready for use.	Any
<b>SYS_SHUTDOWN</b>	Shutdown operation has been initiated by TDH.SYS.LP.SHUTDOWN.	TDH.SYS.SHTDOWNLP (once per LP)

### 12.1.3. Platform Compatibility and Configuration Checking

#### 12.1.3.1. Overview

The Intel TDX module is built assuming a certain set of core and platform features. Most platform configuration required to support the Intel TDX module is checked by MCHECK. However, some configuration is designed to be checked by the Intel TDX module. During the initialization process, the Intel TDX module is designed to check that the platform on which it is running is compatible with this core and platform feature set and/or that the same set of features is provided across the platform. Some of the checks are done per core, and some are done per package. Most of the details are part of the Intel TDX module detailed design.

#### 12.1.3.2. MSR Sampling and Checks

TDH.SYS.INIT reads and checks the contents of some MSRs. In many cases, the MSR value read by TDH.SYS.INIT is also checked for consistency (i.e., having the same values) by TDH.SYS.LP.INIT. In other cases, TDH.SYS.LP.INIT may perform additional checks.

#### 12.1.3.3. CPUID Sampling, Checks and Enumeration

**Note:** CPUID virtualization is described in 9.7.

The TDH.SYS.INIT and TDH.SYS.LP.INIT functions sample CPUID leaf and sub-leaf return values. This is intended to check compatibility with the Intel TDX module and with any guest TD operation. If any of these checks fail, Intel TDX module initialization is designed to fail.

The TDH.SYS.INFO function may be called by the host VMM to enumerate the directly configurable and allowable CPUID fields, using the TDSYSINFO\_STRUCT described in 18.6.1.

### 12.1.4. Physical Memory Configuration Overview

Configuration of the physical memory available to the Intel TDX module (TDMRs) and its associated metadata (PAMT arrays) is done using the TDH.SYS.CONFIG function.

#### 12.1.4.1. Intel TDX ISA Background: Convertible Memory Ranges (CMRs)

A 4KB memory page is defined as **convertible** if it can be used to hold an Intel TDX private memory page or any Intel TDX control structure pages while helping guarantee Intel TDX security properties (i.e., if it can be **converted** from a Shared page to a Private page).

**Convertible Memory Ranges (CMRs)** are defined as physical address ranges that are declared by BIOS, and checked by MCHECK, to hold only convertible memory pages.

CMRs have the following characteristics:

- CMR configuration is "soft" – no hardware range registers are used.
- Each CMR defines a single contiguous physical address range.
- All the memory within each CMR is convertible, and it must comply with the rules checked by MCHECK.
- Each CMR has its own size. CMR size is a multiple of 4KB, and it is **not** required to be a power of two.
- CMRs cannot overlap with each other.
- CMRs must reside within the effective physical address range of the platform (after taking into account the most significant PA bits stolen for Key IDs).
- CMRs are configured at platform scope (no separate configuration per package).
- The maximum number of CMRs is implementation specific. It is not explicitly enumerated; it is deduced from Family/Model/Stepping information provided by CPUID.
  - The maximum number of CMRs is 32.
- CMRs are available on systems with TDX ISA capabilities as enumerated by the IA32\_MTRRCAP.SEAMRR bit.
- CMR configuration is checked by MCHECK and cannot be modified afterwards.

MCHECK stores the CMR table in a pre-defined location in SEAMRR's SEAMCFG region so it can be read later and trusted by the Intel TDX module.

### 12.1.4.2. TDMRs and PAMT Arrays Configuration

TDMRs and PAMTs are described in 6.1. This section provides an overview of their configuration and their relationships to CMRs.

#### 12.1.4.2.1. Background: Reserved Areas within TDMRs

5 As described in 6.1, the Intel TDX module physical memory management is done using PAMT Blocks – each holding the metadata of a 1GB block of TDMR. This implies that TDMR granularity must be 1GB.

However, there is a requirement for the host VMM to be able to allocate memory at granularities smaller than 1GB. This is especially important in systems that have a relatively small amount of memory.

10 To support the two requirements above, the Intel TDX module's design allows arbitrary reserved areas within TDMRs. Reserved areas are still covered by PAMT. However, during initialization their respective PAMT entries are marked with a PT\_RSVD page type, so pages in reserved areas are not used by the Intel TDX module for allocating privately encrypted memory pages (but they can be used for PAMT areas, see below).

Only the non-reserved parts of a TDMR are required to be inside CMRs.

#### 12.1.4.2.2. Background: Three PAMT Areas

15 As described in 6.1, a logical PAMT Block is composed of 1 PAMT\_1G entry, 512 PAMT\_2M entries and  $512^2$  PAMT\_4K entries. Thus, the overall size of a PAMT Block, and as a result of the whole PAMT, is not a power of 2.

However, the host VMM may only be able to allocate memory buffers for PAMT in sizes that are a power of 2.

20 To enable this, buffers for PAMT\_1G entries, PAMT\_2M entries and PAMT\_4K entries are allocated separately. As a result, if the host VMM allocates a TDMR whose size is a power of 2, its three respective PAMT areas will also have sizes that are a power of 2.

PAMT areas are required to be inside CMRs because PAMT is encrypted with a private HKID.

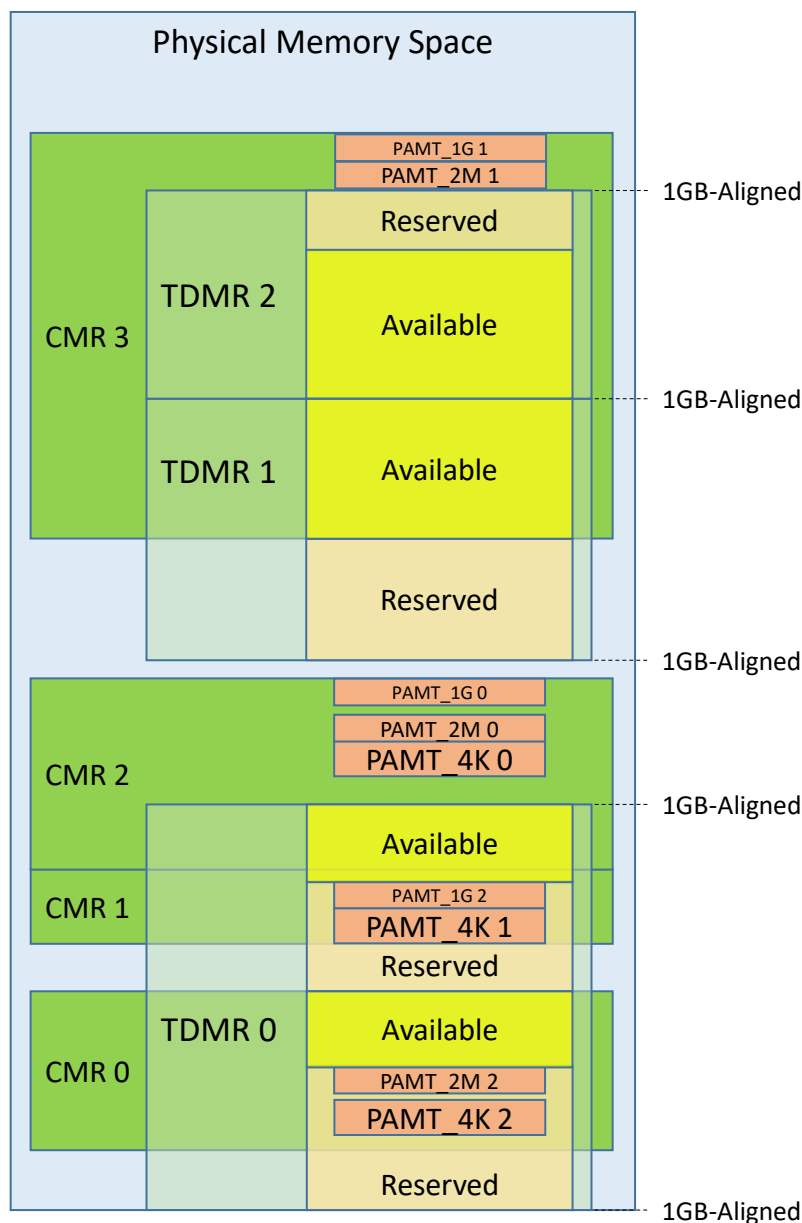


Figure 12.2: Example of Convertible Memory Ranges (CMRs) vs. Trust Domain Memory Regions (TDMRs)

12.1.4.2.3. Configuration Rules

In addition to the rules described in 6.1, the following rules apply to TDMR configuration as related to CMRs:

- 5 • Any non-reserved 4KB page within a TDMR must be convertible – i.e., it must be within a CMR.
- Reserved areas within a TDMR need not be within a CMR.

Three PAMT areas must be configured for each TMDR – one for each physical page size controlled by PAMT:

- 10 • Area for PAMT\_4K entries
- Area for PAMT\_2M entries
- Area for PAMT\_1G entries

PAMT areas have the following attributes:

- 15 • A PAMT area size is directly proportional to the TDMR with which it is associated. The size ratio is enumerated by TDH.SYS.INFO.
- A PAMT area must reside in convertible memory – i.e., each PAMT area page must be a CMR page.
- PAMT areas must not overlap with TDRM non-reserved areas; however, they may reside within TDMR reserved areas (as long as these are convertible).
- PAMT areas must not overlap with each other.

## 12.2. Intel TDX Module Initialization Interface

### 12.2.1. Global Initialization: TDH.SYS.INIT

TDH.SYS.INIT is intended to globally initialize the Intel TDX module. It works as follows:

1. Initialize Intel TDX module global data.
2. Sample and check platform features that need to be checked for platform-wide compatibility – i.e., the Intel TDX module supports several options, but they must be the same across platform. These are later checked on each LP.
3. Sample and check the platform configuration on the current LP. For example, TDH.SYS.INIT samples SMRR and SMRR2, checks they are locked and do not overlap any CMR, and stores their values to be checked later on each LP.
4. Set the system state to SYSINIT\_DONE.

10 For a detailed description of TDH.SYS.INIT, see 20.2.33.

### 12.2.2. LP-Scope Initialization: TDH.SYS.LP.INIT

TDH.SYS.LP.INIT is intended to perform LP-scope, core-scope and package-scope initialization of the Intel TDX module. It can be called only after TDH.SYS.INIT completes successfully, and it can run concurrently on multiple LPs. At a high level, TDH.SYS.LP.INIT works as follows:

- 15 1. Do a global EPT flush (INVEPT type 2).
2. Initialize Intel TDX module LP-scope data.
3. Check features and configuration compatibility and uniformity – once per LP, core or package, depending on the scope of the checked feature or configuration:
  - 3.1. Check features compatibility with the Intel TDX module.
  - 20 3.2. Check configuration uniformity.

For a detailed description of TDH.SYS.LP.INIT, see 20.2.33.

### 12.2.3. Enumeration: TDH.SYS.INFO

Once an LP has been initialized, the host VMM can call TDH.SYS.INFO on that LP to help enumerate the Intel TDX module capabilities and platform configuration.

- 25 • Intel TDX module capabilities are enumerated in the returned TDSYSINFO\_STRUCT (see 18.6.1).
- Convertible Memory Ranges (CMRs), as previously set by BIOS and checked by MCHECK, are enumerated in the returned CMR\_INFO table (see 18.6.3).

For a detailed description of TDH.SYS.INFO, see 20.2.32.

### 12.2.4. Global Configuration: TDH.SYS.CONFIG

30 After performing global and LP-scope initialization, the host VMM can call TDH.SYS.CONFIG to globally configure the Intel TDX module, providing the following information:

- **TDMR and PAMT Table**, where each entry contains a TDMR base address, size and corresponding PAMT reserved area base address and size. The table format (TDMR\_INFO) is described in 18.6.4. Refer to 6.1 for definition of TDMRs.
- 35 • The **HKID** to be used by the Intel TDX module for its global private key, used for encrypting PAMT and TDRs.

For a detailed description of TDH.SYS.CONFIG, see 20.2.31.

### 12.2.5. Package-Scope Key Configuration: TDH.SYS.KEY.CONFIG

After performing global configuration, the host VMM calls TDH.SYS.KEY.CONFIG to perform package-scope configuration of the Intel TDX module's global private key on the hardware.

40 For a detailed description of TDH.SYS.KEY.CONFIG, see 20.2.32.



### 12.3. TDMR and PAMT Initialization

TDMR and PAMT initialization procedure is designed to be performed **during VMM run-time**, after VMM boot. The host VMM should be able to work normally while initialization takes place, at any time using memory that has already been initialized. At a high level, TDMR initialization has the following characteristics:

- 5 • Initialization is performed gradually.
- Initialization function TDH.SYS.TDMR.INIT adheres to the latency rules of most Intel TDX functions – i.e., they take no more than a predefined number of clock cycles.
- Initialization function TDH.SYS.TDMR.INIT **can run concurrently on multiple LPs** if each concurrent flow initializes a **different TDMR**.
- 10 • After each 1GB page of a TDMR has been initialized, that 1GB page becomes available for use by any Intel TDX function that creates a private TD page or a control structure page – e.g., TDH.MEM.PAGE.ADD, TDH.VP.ADDCX, etc.

For each TDMR, the VMM should execute a loop of **TDH.SYS.TDMR.INIT** providing the TDMR start address (at 1GB granularity) as an input.

- 15 TDH.SYS.TDMR.INIT initializes an (implementation-defined) number of PAMT entries. The maximum number of PAMT entries to be initialized is designed to avoid latency issues. Initialization uses direct writes (MOVDIR64B).

Once the PAMT for each 1GB block of TDMR has been fully initialized, TDH.SYS.TDMR.INIT marks that 1GB block as ready for use; that means 4KB pages in this 1GB block may be converted to private pages – e.g., by TDH.MEM.PAGE.ADD. This can be done concurrently with adding and initializing other TDMRs.

For a detailed description of TDH.SYS.TDMR.INIT, see 20.2.37.

### 20 12.4. Intel TDX Module Shutdown

#### 12.4.1. Shutdown Initiated by the Host VMM (as Part of Module Update)

- The host VMM can initiate Intel TDX module shutdown at any time by calling the TDH.SYS.LP.SHUTDOWN function. This is intended for use as part of reloading the Intel TDX module without going through a warm or cold reset sequence. TDH.SYS.LP.SHUTDOWN is designed to set state variables to block all SEAMCALLs on the current LP and all SEAMCALL leaf functions except TDH.SYS.LP.SHUTDOWN on the other LPs. SEAMLDR, when instructed to reload a new Intel TDX module image, can check that TDH.SYS.SHUTDOWN has been executed on all LPs.
- 25

#### 12.4.2. Shutdown Initiated by a Fatal Error

By design, fatal errors during Intel TDX module execution cause an immediate LP shutdown. Subsequent SEAMCALLs on any LP throw a #GP(0) fault. This situation can only be recovered by a reset.

## 13. Debug and Profiling Architecture

The Intel TDX module debug architecture includes the following debug facilities:

**On-TD Debug:** Facilities for debugging a guest TD using software that runs inside the TD

**Off-TD Debug:** Facilities for debugging a guest TD, configured in debug mode, using software that runs outside the TD

### 13.1. On-TD Debug

Intel SDM, Vol. 3, 17      Debug, Branch Profile, TSC and Intel Resource Director Technology (Intel RDT) Features

#### 13.1.1. Overview

On-TD debug is the normal mode used to debug guest TD software. A debug agent resides inside the guest TD, and it can interact with external entities (e.g., a debugger) via standard I/O interfaces. The Intel TDX module is designed to virtualize and isolate TD debug capabilities from the host VMM and other guest TDs or legacy VMs. On-TD debug can be used for production or debug TDs – i.e., regardless of the guest TD's ATTRIBUTES.DEBUG state.

Guest TDs are allowed to use almost all architectural debug features supported by the processor, e.g.:

- Single stepping
- Code, data and I/O breakpoints
- INT3
- Bus lock detection
- DR access detection
- TSX debug

However, the TDX architecture does not allow guest TDs to toggle IA32\_DEBUGCTL uncore PMI enabling bit (13).

Guest TDs are allowed to use almost all architectural tracing features, e.g.:

- LBR (if allowed by the TD's XFAM, see 9.4)
- PT (if allowed by the TD's XFAM, see 9.4)
- BTS

However, the TDX architecture does not allow guest TDs to use BTM.

#### 13.1.2. Generic Debug Handling

##### 13.1.2.1. Context Switch

By design, the Intel TDX module context-switches all debug/tracing state that the guest TD is allowed to use.

- DR0-3, DR6 and IA32\_DS\_AREA MSR are context-switched in TDH.VP.ENTER and TD exit flows.
- RFLAGS, IA32\_DEBUGCTL MSR and DR7 are saved and cleared on VM exits from the guest TD and restored on VM entry to the guest TD.
- Pending debug traps are natively saved on VM exits from the guest TD and reloaded on VM entries using the TD VMCS PDE field.

##### 13.1.2.2. IA32\_DEBUGCTL MSR Virtualization

Intel SDM, Vol. 3, 17.4.1      IA32\_DEBUGCTL MSR

By design, IA32\_DEBUGCTL access by the guest TD is restricted as follows:

- Guest TD attempts to set any of the architecturally-reserved bits 63:15 and 5:2 result in a #GP(0).
- Guest TD attempts to set TDX-disallowed values result in a #VE. This includes the following cases:
  - Enable Uncore PMI by setting bit 13 to 1 (see 13.4 below).
  - Enable BTM by setting bits 7:6 to 0x1 (see details in 13.1.3 below).
- Uncore PMI is virtualized as disabled; bit 13 is read as 0 (see 13.4 below).

### 13.1.3. Debug Feature-Specific Handling

The following table discusses how specific debug features are handled.

**Table 13.1: Debug Feature-Specific Handling**

Debug Feature	How the Feature is Controlled	Handling
<b>Hardware Breakpoints</b>	<ul style="list-style-type: none"> <li>DR7, DR0-3 and DR6</li> </ul>	No special handling: DRs are context-switched.
<b>General Detect</b>	<ul style="list-style-type: none"> <li>DR7 bit 13 (GD)</li> </ul>	No special handling: DR7 is context-switched.
<b>TSX Debug</b>	<ul style="list-style-type: none"> <li>DR7 bit 11 (RTM)</li> <li>IA32_DEBUGCTL bit 15 (RTM)</li> </ul>	No special handling: DR7 and IA32_DEBUGCTL are context-switched.
<b>Single Stepping</b>	<ul style="list-style-type: none"> <li>RFLAGS bits 18 (Trap Flag) and 16 (Resume Flag)</li> <li>IA32_DEBUGCTL bit 1 (BTF)</li> </ul>	No special handling: RFLAGS and IA32_DEBUGCTL are context-switched.
<b>Bus-Lock Detection</b>	<ul style="list-style-type: none"> <li>IA32_DEBUGCTL bit 2 (BUS_LOCK_DETECT)</li> </ul>	No special handling: IA32_DEBUGCTL is context-switched.
<b>Software Breakpoints (INT1, INT3)</b>	None	No special handling: software breakpoints are stateless.
<b>Branch Trace Message (BTM)</b>	<ul style="list-style-type: none"> <li>IA32_DEBUGCTL bits 6 (TR) and 7 (BTS)</li> </ul>	<p>Not allowed: when a guest TD attempts to set IA32_DEBUGCTL[7:6] to 0x1, the Intel TDX module injects a #VE (see 13.1.2 above).</p> <p>In debug mode (ATTRIBUTES.DEBUG == 1), the host VMM is allowed to activate BTM by setting the above bits to 0x1.</p>
<b>Branch Trace Store (BTS)</b>	<ul style="list-style-type: none"> <li>IA32_DEBUGCTL bits 6 (TR), 7 (BTS), 8 (BTINT), 9 (BTS_OFF_OS) and 10 (BTS_OFF_USR)</li> </ul>	<p>No special handling: IA32_DEBUGCTL and IA32_DS_AREA are context-switched.</p> <p><b>Note:</b> The guest TD can configure BTS to raise PMI on buffer overflow (by setting BTINT = 1). However, since PMIs are virtualized by the host VMM, the guest TD should be ready to handle spurious, delayed and dropped PMIs. See Perfmon discussion in 13.2 below.</p>
<b>Processor Trace (PT)</b>	<ul style="list-style-type: none"> <li>IA32_RTIT_CONTROL</li> <li>Requires VMM's consent on TD initialization by setting TD_PARAMS.XFAM[8] to 1</li> </ul>	PT state handling as part of the extended feature set state is discussed in 9.4.
<b>Architectural Last Branch Records (LBRs)</b>	<ul style="list-style-type: none"> <li>IA32_LBR_CONTROL</li> <li>Requires VMM's consent on TD initialization by setting TD_PARAMS.XFAM[15] to 1</li> </ul>	LBR state handling as part of the extended feature set state is discussed in 9.4.
<b>Non-Architectural LBRs</b>	<ul style="list-style-type: none"> <li>IA32_DEBUGCTL bit 0 (LBR)</li> </ul>	Not allowed: a guest TD attempt to set IA32_DEBUGCTL[0] results in a #VE (see 13.1.2 above).

## 13.2. On-TD Performance Monitoring

Intel SDM, Vol. 3, 18 Performance Monitoring

### 13.2.1. Overview

The host VMM controls whether a guest TD can use the performance monitoring ISA using the TD's ATTRIBUTES.PERFMON bit – part of the TD\_PARAMS input to TDH.MNG.INIT (see 18.2.1).

By design, if a guest TD is allowed to use performance monitoring:

- The guest TD enumerates native Perfmon capabilities via CPUID leaf 0x0A.
- The guest TD is allowed to use all Perfmon ISA. This includes CR4.PCE, the RDPMC instruction and the Perfmon MSRs (see 13.2.2 below).
- Perfmon state is context-switched by the Intel TDX module across TD entry and exit transitions.

Context-switching the Perfmon state has a performance impact. TD entry and exit latencies are longer than when a guest TD is not allowed to use Perfmon.

By design, if a guest TD is not allowed to use performance monitoring:

- The guest TD enumerates no Perfmon capabilities. CPUID leaf 0x0A returns all 0s.
- The guest TD is not allowed to use Perfmon ISA.
- Perfmon state is not context-switched across TD entry and exit transitions.

Regardless of Perfmon enabling, per the design:

- IA32\_DS\_AREA MSR is context-switched across TD entry and exit transitions.
- Counter freeze control (IA32\_DEBUGCTL bit 12) is context-switched across TD entry and exit transitions.
- The uncore PMI enable bit (IA32\_DEBUGCTL bit 13) is preserved during SEAM mode execution, including Intel TDX module and guest TD execution. This bit is virtualized to the guest TD as 0, and the TD is prevented from setting it. See 13.4 below for details.

See also 13.1 above.

The Intel TDX module is designed to support performance monitoring as implemented on the GLC core:

- Architectural performance monitoring version 5, described in [Intel SDM, Vol. 3, 18.2.5]
- Exactly 8 performance monitoring counters (IA32\_PMC0 through IA32\_PMC7)
- Exactly 4 fixed counters (IA32\_FIXED\_CTR0 through IA32\_FIXED\_CTR3)
- Some non-architectural MSRs (see 13.2.2 below)

### 13.2.2. Performance Monitoring MSRs

Perfmon uses the following MSRs:

**Table 13.2: Performance Monitoring MSRs**

MSR	Comments	Enumeration	Reference
IA32_PMCx	multiple MSRs	CPUID(0x0A).EAX[15:8] The Intel TDX module requires the CPU to support 8 counters.	
IA32_PERFEVTSELx	multiple MSRs	CPUID(0x0A).EAX[15:8]	
MSR_OFFCORE_RSPx	2 MSRs, model-specific		
IA32_FIXED_CTRx	multiple MSRs	IA32_FIXED_CTRx is supported if (x < CPUID(0x0A).EDX[4:0]) or if (CPUID(0x0A).ECX[x] == 1). The Intel TDX module requires the CPU to support counters 0 through 3.	[Intel SDM, Vol. 3, 18.2.5.2]
IA32_PERF_METRICS			

MSR	Comments	Enumeration	Reference
IA32_PERF_CAPABILITIES			
IA32_FIXED_CTR_CTRL			
IA32_PERF_GLOBAL_STATUS			
IA32_PERF_GLOBAL_CTRL			
IA32_PERF_GLOBAL_STATUS_RESET			
IA32_PERF_GLOBAL_STATUS_SET			
IA32_PERF_GLOBAL_INUSE			
IA32_PEBS_ENABLE	model-specific		
MSR_PEBS_DATA_CFG	model-specific		
MSR_PEBS_LD_LAT	model-specific		
MSR_PEBS_FRONTEND	model-specific		
IA32_A_PMCx	multiple MSRs	CPUID(0x0A).EAX[15:8], IA32_PERF_CAPABILITIES[13]  The Intel TDX module requires the CPU to support 8 counters.	[Intel SDM, Vol. 3, 18.2.6]

MSR virtualization is described in 9.6.

### 13.2.3. Performance Monitoring Interrupts (PMIs)

By design, when a guest TD is allowed to use Perfmon, it can also configure the counters to raise PMI on overflow. When such a TD counter overflows, the physical interrupt or an NMI configured by the host VMM into the local APIC is delivered. This interrupt or NMI causes a VM exit, and it is delivered as a TD exit to the host VMM. The host VMM is then expected to inject the PMI into the guest TD, either as a virtual interrupt using the posted interrupt mechanism (see 9.8.3), or as virtual NMI using the NMI injection interface (see 9.8.4).

Since the host VMM is not trusted, the guest TD must be ready to handle spurious, delayed or dropped PMIs. Thus, it is recommended for the guest TD to use PEBS instead of PMIs in order to record TD state at counter overflows.

Uncore PMIs are discussed in 13.4 below.

## 13.3. Off-TD Debug

A guest TD is defined as **debuggable** if its ATTRIBUTES.DEBUG bit is 1. In this mode, the host VMM can use Intel TDX functions to access secret TD state that is not accessible for non-debuggable TDs.

A debuggable TD is, by nature, untrusted. Since the TD's ATTRIBUTES are included in the TDG.MR.REPORT, the TD's debuggability state can be known to any third party to which the TD attests.

The applicable Intel TDX functions are listed in Table 13.3 below. Note that some of the functions can access non-secret guest TD state regardless of the DEBUG attribute. The lists of state information that can be read and/or written in non-DEBUG and in DEBUG modes are detailed in the referenced sections.

**Table 13.3: Off-TD Debug Interface**

Intel TDX Function	ATTRIBUTES.DEBUG = 0	ATTRIBUTES.DEBUG = 1	References
TDH.MNG.RD/ TDH.MNG.WR	N/A	Access secret and non-secret TD-scope state in TDR and TDCS.	19.1, 20.2.20, 20.2.21
TDH.MEM.SEPT.RD/ TDH.MEM.SEPT.WR	Access Secure EPT entry	Access Secure EPT entry, see note below.	20.2.10, 20.2.12

Intel TDX Function	ATTRIBUTES.DEBUG = 0	ATTRIBUTES.DEBUG = 1	References
TDH.VP.RD/ TDH.VP.WR	Access non-secret TD VCPU state in TDVPS (including TD VMCS)	Access secret and non-secret TD VCPU state in TDVPS (including TD VMCS).	19.2
TDH.PHYMEM.PAGE.WR/ TDH.PHYMEM.PAGE.RD	N/A	Access TD-private memory.	20.2.23, 20.2.23
TDH.PHYMEM.PAGE.RDMD	Read page metadata (PAMT information)	Read page metadata (PAMT information).	20.2.27

### 13.3.1. Note on TDH.VP.WR in Debug Mode

In some debug mode cases, the host VMM can write architecturally illegal values to fields. This means that later VM entry checks by the CPU will fail, and the Intel TDX module is designed to handle these as fatal errors leading to its shutdown. In any case, the security of other guest TDs running in production mode should not be impacted.

In other debug mode cases, TDH.VP.WR allows setting of TDVPS fields to values that may impact the correct operation of the TD under debug. It is the responsibility of the host VMM to take this into consideration. Following are the intended applicable cases:

- TDH.VP.WR is allowed to enable BTM by setting guest IA32\_DEBUGCTL[7:6] to 0x1 (see 13.1.3).
- TDH.VP.WR is allowed to enable VM exit on exceptions other than MCE by setting the TD VMCS exception bitmap execution control. The Intel TDX module does not take this into account when handling VM exits that occur during event delivery.

### 13.3.2. Preventing Guest TD Corruption of DRs

The host-side debugger may need to have full control over guest DRs to help prevent their corruption by the guest TD. To do so, the debugger can do the following:

- Use TDH.VP.WR to set the TD VMCS GUEST\_DR7 field's Global Detect bit.
- Set the TD VMCS exception bitmap execution control to intercept debug exceptions.

## 13.4. Uncore Performance Monitoring Interrupts (Uncore PMIs)

By design, neither the Intel TDX module itself nor its guest TDs are allowed to use Uncore PMIs. The state of IA32\_DEBUGCTL MSR bit 13 (ENABLE\_UNCORE\_PMI) is preserved across SEAMCALL, SEAM root and non-root mode and SEAMRET, except for very short time periods immediately after SEAMCALL and VM exit.

## 13.5. System Profiling Mode

The Intel TDX module may be initialized in a system profiling mode by specifying the SYSPROF module attribute input to TDH.SYS.INIT (see 20.2.33). In this mode, the Intel TDX module and all guest TDs operation may be monitored by the host VMM using Perfmon counters.

When system profiling mode is on, guest TDs cannot be trusted. This fact is reflected to all guest TDs as part of their ATTRIBUTES (see 18.2.1). ATTRIBUTES is reflected in the TD attestation as part of TDINFO\_STRUCT (see 18.5.5). In addition, guest TDs cannot use on-TD performance monitoring (see 13.2 above).

## 14. Machine Check Handling

### 14.1. Machine Check Architecture Background

The **machine-check architecture (MCA)** provides a mechanism for detecting and reporting hardware (machine) errors. These include system bus errors, ECC errors, parity errors, cache errors and TLB errors. MCA consists of a set of model-specific registers (MSRs) that are used to set up machine checking, and it includes additional banks of MSRs used for recording errors that are detected. The processor signals the detection of an uncorrected machine-check error by generating a **machine-check exception (#MC)**, which is an abort class exception. The implementation of the machine-check architecture does not ordinarily permit the processor to be restarted reliably after generating a machine-check exception. However, the machine-check-exception handler can collect information about the machine-check error from the machine-check MSRs.

In native virtualized platforms, this machine-check exception handler is expected to be implemented in the Virtual Machine Monitor (VMM) or in a control-OS – both of which are considered to be outside the TCB for Trust Domains. Processors on which TDX will be supported also can report information on corrected machine-check errors and deliver a programmable interrupt for software to respond to MC errors – referred to as **corrected machine-check error interrupt (CMCI)**. Intel64 processors supporting MCA and CMCI also support an additional enhancement to support software recovery from certain **uncorrected recoverable machine check errors**.

### 14.2. Security Objectives for Machine Check Handling

TDX architecture aims to provide resiliency against confidentiality and integrity attacks by software and limited hardware attacks. Towards this goal, the TDX architecture helps enforce the enabling of memory integrity for all private HKIDs. The CPU memory controller computes the integrity check value (MAC) for the data (cache line) during writes, and it stores the MAC with the memory as meta-data. A 28-bit MAC is stored in the ECC bits

In addition to the MAC meta-data, the memory controller also maintains a 1-bit **TD Owner** meta-data for cache-lines belonging to pages assigned to a TD for use as TD private memory. The TD Owner bit is set for TD cache lines and is clear for non-TD cache lines, and it is also covered by ECC and included in MAC calculation.

By design, checking of memory integrity is performed during memory reads. Memory integrity errors on an integrity checking failure, which can occur due to inadvertent corruption of data or due to malicious corruption, are logged by the memory controller as **UCNA (uncorrected no-action required) UCR errors** – the cache line is poisoned, and a value of 0 is returned to the core. In addition, if the TD Owner bit was set, the memory controller marks the key itself as poisoned; any subsequent reads using that key on the same memory controller also return a poisoned and zeroed data to the code.

On a subsequent consumption (read) of the poisoned data by software, there are two possible scenarios:

**Scenario 1:** Core determines that the execution can continue, and it treats poison with exception semantics signaled as a **#MCE (Machine Check Exception) or MSMI (Machine-check System Management Interrupt)**.

**Scenario 2:** Core determines execution cannot continue, and it does an unbreakable shutdown (e.g., long flows).

The Intel TDX module programs the logical processors to handle both scenarios for two cases:

- When a guest TD (in SEAM non-root mode) is executing on a logical processor
- When the Intel TDX module (in SEAM root mode) is executing on a logical processor

This is described in the following sections.

**Hence, the security objectives for the Intel TDX module for Machine Check handling are:**

- Corruption of TD private data or Intel TDX module memory must be detectable before the decrypted corrupted data are consumed by the guest TD or the Intel TDX module.
- Host software must not be able to **repeatedly** cause machine-checks during Intel TDX module or guest TD operation.
- Host software must not be able to speculatively or non-speculatively access TD private memory to detect if a prior corruption attempt was successful in finding an integrity collision or failed and received zero-data.
- On an integrity violation machine-check, the affected guest TD and the key corresponding to its affected HKID must be unusable for normal operation of the TD – i.e., the TD may only be torn down.

### 14.3. Corrected Machine Check Interrupt (CMCI)

CMCI is delivered as a normal interrupt. If delivered during guest TD operation, this interrupt causes a VM exit, and Intel TDX module performs a TD exit to the host VMM. If delivered during Intel TDX module operation, this interrupt remains pending until either SEAMRET to the host VMM or until VM entry to a guest TD.

### 14.4. Handling #MC during Guest TD Operation

An MC HARD event results in an unbreakable shutdown.

An MC KIND event that occurs during guest TD operation (in SEAM non-root mode) cannot be delivered directly by the CPU to the guest TD (as an #MC exception) for recovery attempts. That is because the guest TD software will have no avenue to translate HPAs logged in MCA banks to GPAs needed for guest TD handling. Hence, an MC KIND event during guest TD execution is considered a fatal event for that TD, and the Intel TDX module is designed to prohibit further TD entry. The TD exits to the host VMM, indicating a TDH.VP.ENTER completion with a non-recoverable TD state. The exit reason and exit qualification are reported in GPRs. The host VMM then can analyze the #MC details and reclaim the TD memory, as described in 14.6 below.

### 14.5. Handling #MC during Intel TDX Module Operation

A machine check (kind) event that occurs during Intel TDX module operation (in SEAM root mode) forces a shutdown on a current LP. Shutdown also prevents subsequent SEAMCALL on any LP.

### 14.6. Reclaiming Memory after a Machine Check Event

A machine check can occur due to non-malicious cases – e.g., due to a bit flip caused by cosmic rays. Hence, it is a functional requirement to be able to reclaim memory for a guest TD that was stopped due to a machine check event.

14.4 above described how the Intel TDX module is designed to handle #MC during guest TD operation. At the same time, the platform broadcasts the MC event to other LPs. Other TDs executing on other LPs will similarly be marked as FATAL. Eventually, all LPs are executing in the host VMM’s #MC handler, where the VMM can interrogate the MC status registers. The host VMM can reclaim memory assigned to TDs in a FATAL state using the normal TD teardown flow (TDH.MNG.KEY.RECLAIMID, TDH.VP.FLUSH, TDH.PHYMEM.CACHE.WB, TDH.MNG.KEY.FREEID, TDH.PHYMEM.PAGE.RECLAIM).

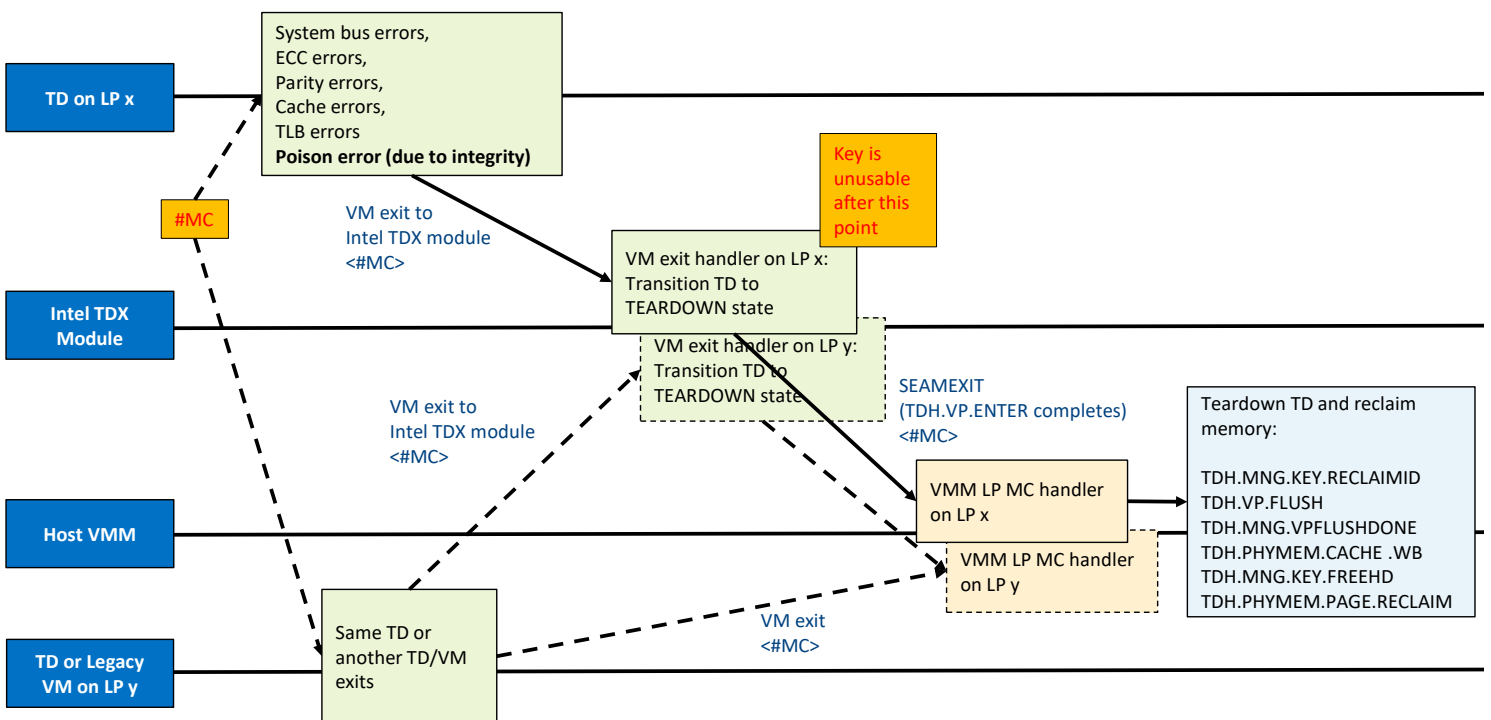


Figure 14.1: Example of Machine Check Handling and TD Memory Reclamation



## 15. General Aspects of the Intel TDX Interface Functions

### 15.1. Concurrency Restrictions and Enforcement

#### 15.1.1. Explicit Concurrency Restrictions

Intel TDX functions may specify concurrency restrictions on accessing one or more resources, as described below. In most cases, the restriction applies for the duration of the instruction execution. However, in some cases, the restriction applies for a longer duration. For example, TDH.VP.ENTER requires shared access to the TD-scope logical control structures TDR and TDCS, and it also requires shared access to TDVPS – the VCPU-scope logical control structure which applies during TDX non-root operation through TD Exit.

**Table 15.1: Concurrency Restrictions of Intel TDX Functions or Flows**

Concurrency Restriction	Description	Examples
<b>Exclusive Access</b>	During the period when an LP has an exclusive access to a certain resource, any attempt by another LP to concurrently execute an instruction that requires either an exclusive or a shared access to the same resource will fail.	<ul style="list-style-type: none"> <li>TDH.VP.CREATE requires an exclusive access to the TDVPR page.</li> </ul>
<b>Shared Access</b>	During the period when an LP has a shared access to a certain resource, any attempt by another LP to concurrently execute an instruction that requires an exclusive access to the same resource will fail. No such restriction exists on another LP that attempts to concurrently execute an instruction that requires a shared access.	<ul style="list-style-type: none"> <li>TDH.VP.CREATE requires a shared access to the TDR page.</li> <li>TDH.PHYMEM.CACHE.WB requires a shared access to the KOT.</li> </ul>

Software is expected to comply with the specified concurrency restrictions. The Intel TDX module helps enforce them (using internal locks) for proper TDX operation.

**Table 15.2: Concurrency Restrictions Cross-Table**

		Logical Processor Y		
		Concurrency Restriction	Exclusive	Shared
Logical Processor X	Exclusive	Not Allowed	Not Allowed	Allowed
	Shared	Not Allowed	Allowed	Allowed
	None	Allowed	Allowed	Allowed

Intel TDX functions do not wait on a resource that requires an exclusive or a shared access. If the resource is busy, the function fails immediately.

#### 15.1.2. Implicit Concurrency Restrictions

In some cases, Intel TDX functions and whole flows (e.g., TD Entry through TD Exit) may have **implicit** exclusive or shared access to resources. This means that the access restriction is implied by the architecture, but no direct enforcement is made by the flow itself.

An important case is TDX non-root mode. TDH.VP.ENTER acquires shared locks on the TD’s TDR and TDCS control structures and on the VCPU’s TDVPS control structure. These shared locks are released only on TD exit. Thus, during all the time the LP is in the logical TDX non-root mode, including during TDCALL leaf functions, the LP has implicit shared access to TDVPS, TDR and TDCS.

## 15.2. Memory and Resource Operands Access

Intel SDM, Vol. 3, 11.5.2	Precedence of Cache Controls
Intel SDM, Vol. 3, 11.11	Memory Type Range Registers (MTRRs)
Intel SDM, Vol. 3, 11.12	Page Attribute Table (PAT)

### 5 15.2.1. Overview

In this section, we discuss Intel TDX functions' memory and resource operands access from the following perspectives:

- Access semantics (shared, private, opaque and hidden)
- Explicit vs. implicit accesses
- Operand address specification (host-physical address, guest-physical address)
- 10 • Actual memory access (read or write) vs. memory reference

#### 15.2.1.1. Access Semantics

Access semantics, as used in this document, convey the intended purpose of the access. Intel TDX functions are designed to use one of the following access semantics when accessing their memory and/or platform resource parameters:

**Table 15.3: Access Semantics Definition**

Access Semantics	Description	Intel TDX Module Usage
<b>Shared</b>	Memory is accessed using one of the shared HKIDs (in the range 0 to MAX_MKTME_HKIDS - 1). This is mostly used for memory parameters accessed by the VMM.	<ul style="list-style-type: none"> <li>• Source page of TDH.MEM.PAGE.ADD</li> <li>• Memory operands of TDCALL leaf functions</li> </ul>
<b>Private</b>	The memory is mapped in the TD's private GPA space. Memory accessed using the target TD's private HKID (in the range MAX_MKTME_HKIDS - 1 to MAX_HKIDS - 1). Such memory pages can be mapped in the TD's private GPA space.	<ul style="list-style-type: none"> <li>• TD private pages</li> <li>• Secure EPT pages</li> </ul>
<b>Opaque</b>	Memory is addressable by the host VMM, but its content is not directly accessible to software or devices. Memory is encrypted using either the Intel TDX global private key (for TDR) or the TD's ephemeral private key (for other control structures).	<ul style="list-style-type: none"> <li>• TDR</li> <li>• TDCX</li> <li>• TDVPR</li> <li>• TDVPX</li> </ul>
<b>Hidden</b>	Access is to an Intel TDX module internal resource. That resource is not directly addressable as a memory operand to software or devices.	<ul style="list-style-type: none"> <li>• KOT</li> <li>• WBT</li> </ul>

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Note that on guest-side (TDCALL) functions, shared vs. private semantics is determined by the GPA provided as an operand to the function. A specific TDCALL leaf function may or may not impose a private or a shared access – e.g., TDG.MEM.PAGE.ACCEPT requires a private GPA, while TDG.MR.REPORT may work with either a private GPA or a shared GPA.

#### 20 15.2.1.2. Explicit vs. Implicit Access

An **explicit memory access** is defined as an access where the memory location is provided as explicit operand to an Intel TDX function. The address may be provided directly in a GPR or indirectly via some address field in a software-accessible memory data structure.

The HKID for accessing the memory can be inferred by the instruction – implicitly or explicitly from the explicitly provided access.

25

An **implicit memory access** is defined as an access to a platform physical memory address, or to some other resource, that is not passed as an operand of an instruction (either directly or indirectly) but is implied by use of the Intel TDX function. TDX architecture helps guarantee that an implicit access is performed correctly, or a proper error action is taken.

### 5 15.2.1.3. *Memory Operand Address Specification*

Host-side Intel TDX functions (SEAMCALL leaf functions) memory operands are specified using their **host-physical address (HPA)**, their **guest-physical address (GPA)**, or when a GPA-to-HPA mapping is done (e.g., TDH.MEM.PAGE.ADD) by **both HPA and GPA**.

In most cases, HPA for private or opaque access semantics must be specified with all HKID bits set to 0.

10 Guest-side Intel TDX functions (TDCALL leaf functions) memory operands are specified using their **guest-physical address (GPA)**.

### 15.2.1.4. *Memory Type*

#### 15.2.1.4.1. *Memory Type for Private and Opaque Accesses*

The memory type for **private** and **opaque** access semantics, which use a private HKID, is WB.

#### 15 15.2.1.4.2. *Memory Type for Shared Accesses*

Intel SDM, Vol. 3, 28.2.7.2 *Memory Type Used for Translated Guest-Physical Addresses*

The memory type for **shared** access semantics, which use a shared HKID, is determined as described below. Note that this is different from the way memory type is determined by the hardware during non-root mode operation. Rather, it is a best-effort approximation that is designed to still allow the host VMM some control over memory type.

- 20 • For **shared access during host-side (SEAMCALL) flows**, the memory type is determined by MTRRs.
- For **shared access during guest-side flows (VM exit from the guest TD)**, the memory type is determined by a combination of the Shared EPT and MTRRs.
  - If the memory type determined during Shared EPT walk is WB, then the effective memory type for the access is determined by MTRRs.
  - 25 ○ Else, the effective memory type for the access is UC.

#### 15.2.1.5. *Actual Memory Access vs. Memory Reference*

In some cases, Intel TDX functions only **reference** memory – i.e., use its address, but no actual access is done.

In other cases, Intel TDX functions **access** the memory – i.e., perform read or write (but not execute) operations.

## 15.2.1.6. Summary Table

Table 15.4: Memory Access Summary

Explicit/ Implicit	Intel TDX Function	Access Semantics	Address Operand	HKID Derivation	Memory Type	Example
Explicit	Host-Side (SEAMCALL Leaf)	Shared	HPA	Derived HPA operand's HKID bits	From MTRR	SRCPAGE operand of TDH.MEM.PAGE.ADD
		Private	HPA	TD's HKID	WB	Target page of TDH.PHYMEM.PAGE.RECLAIM
			GPA	TD's HKID	WB	CHUNK operand of TDH.MR.EXTEND
			HPA and GPA	TD's HKID	WB	Target page of TDH.MEM.PAGE.ADD
		Opaque	HPA	TD's HKID or Intel TDX global HKID	WB	TDVPR operand of TDADDVPR
	Guest-Side (TDCALL Leaf)	Shared	GPA	From Shared EPT	From Shared EPT and MTRR	REPORTDATA operand of TDG.MR.REPORT
		Private	GPA	TD's HKID	WB	Target page of TDG.MEM.PAGE.ACCEPT
Implicit	All	Private/ Opaque	N/A	TD's HKID or Intel TDX global HKID	WB	TDCS access by TDH.VP.ENTER
		Hidden	N/A	N/A	N/A	KOT access by TDH.MNG.KEY.CONFIG

## 15.3. Register Operands and CPU State Convention

- 5 [Intel SDM, Vol. 3, 24.9](#) [VM-Exit Information Fields](#)  
[Intel SDM, Vol. 3, App. C](#) [VMX Basic Exit Reasons](#)

## 15.3.1. Overview: Regular vs. Transition Leaf Functions

Intel TDX functions can be divided into transition functions and non-transition functions.

10 The **non-transition functions** are where SEAMCALL and TDCALL leaf functions behave as emulated CPU instructions from the perspective of the host VMM and the guest TD, respectively. In those cases, the meaning of input and output register operands is straightforward – similar to CPU instructions.

15 **Transition cases** are SEAMCALL(TDH.VP.ENTER) and TDCALL(TDG.VP.VMCALL) leaf functions, where a full cycle (until start of the next instruction) includes TD transitions to the guest TD or host VMM, respectively, and back to the host VMM or guest TD, respectively. In those cases, we look at the functions from the point of view of the caller. The meaning of input and output register operands is more complicated.

Both cases are explained in the following sections and in the function reference sections.

## 15.3.2. Interface Function Completion Status

20 Intel TDX function completion status is returned in RAX. The status is structured to provide as many details to software about error conditions as practically possible. At the same time, the status enables software to ignore details that it does not need. Software may parse the completion status at three detail levels, as described below.

### 15.3.2.1. *Least Detailed Level: Success/Warning/Error*

At this simplest level, software can differentiate among three cases:

**Table 15.5: Intel TDX Interface Functions Completion Status in RAX at Least Detailed Level**

RAX	Meaning	Description
0	Success	Function completed successfully
> 0 (0x00000000_00000001 – 0x7FFFFFFF_FFFFFFFF)	Informational / Warning	Function completed successfully, but with some informational or warning code – e.g., TDH.PHYMEM.PAGE.RECLAIM of a TDCX page that is already not VALID
< 0 (0x80000000_00000000 – 0xFFFFFFFF_FFFFFFFF)	Error	Function aborted due to some error

### 5 15.3.2.2. *Medium Detailed Level: Class and Recoverability*

At this level, software can understand the following information:

**Class:** The class of error or warning – e.g., Resource Busy

**Recoverability Hint:** Whether the function can be **retried** after some conditions have been corrected – e.g., if some resource was busy due to a concurrency error, retrying the function may succeed.

### 15.3.2.3. *Most Detailed Level*

At this level, software can understand more details of an error that happened – e.g., if TDH.VP.ADDCX fails, software may understand if it is due to a wrong number of TDVPX pages or due to the VCPU already being initialized.

**Table 15.6: Intel TDX Interface Functions Completion in RAX at Most Detailed Level**

Bits	Name	Description
63	ERROR	Instruction aborted due to error. 0: Indicates that the function completed successfully – possibly with some warnings. 1: Indicates that the function aborted due to some error.
62	RECOVERABLE	Recoverability hint – applicable only when ERROR is 1. 0: Indicates that the function may possibly be retried after some conditions have been corrected. 1: Indicates that the error is probably not recoverable.
61:48	RESERVED	Reserved – set to 0
47:40	CLASS	Class of the function completion status
39:32	DETAILS_L1	Details of the function completion status
31:0	DETAILS_L2	Additional details of the function completion status – e.g., includes: <ul style="list-style-type: none"> <li>• Implicit or explicit operand identifier</li> <li>• CPUID leaf or sub-leaf</li> <li>• MSR index</li> <li>• VMCS field code</li> <li>• VM exit reason</li> <li>• CMR index</li> </ul>

Bits	Name	Description
		<ul style="list-style-type: none"> <li>TDMR index</li> </ul>

Refer to 17.1 for a list of function completion codes.

### 15.3.3. Other CPU State Convention

All Intel TDX functions except TDH.VP.ENTER are designed to preserve the CPU state not explicitly defined as output.

- 5 TDH.VP.ENTER is a special case. In addition to explicit output operands discussed in 15.3.4 below, TDH.VP.ENTER is not designed to preserve the extended CPU state that the TD may use according to TDCS.XFAM.

The host VMM is expected to save any state it needs before calling TDH.VP.ENTER. Details are provided in the TDH.VP.ENTER leaf function definition (see 20.2.31).

### 15.3.4. Transition Cases: TD Entry and Exit

#### 10 15.3.4.1. TD Entry: TDH.VP.ENTER

##### Transfer of Host VMM State to TD Guest

By design, in the case of a TDH.VP.ENTER leaf function that follows a previous TDG.VP.VMCALL, the RCX input parameter of the previous TDG.VP.VMCALL is used as a bitmap. It selects the GPRs (from RBX, RDX, RBP, RDI, RSI and R8 through R15) and XMM registers whose value is transferred to the guest TD as-is. RAX is set to 0. See the TDG.VP.VMCALL description in 20.3.8.

The rest of the CPU state is restored from the TD VCPU state as saved on TDG.VP.VMCALL.

##### Output State (Back to the Host VMM)

On completion of TDH.VP.ENTER, a success – indicated by the ERROR bit (RAX[63]) being 0 – means that TD Entry into the TD guest was successful. The TD guest ran for some time and then exited to the Intel TDX module. That exit can be due to execution of TDG.VP.VMCAL) or due to an asynchronous exit (e.g., an EPT Violation). The Intel TDX module then executes SEAMRET, transferring control to the instruction following TDH.VP.ENTER. In this case, the DETAILS field (RAX[31:0]) format is designed to be the same as the VMX Exit reason.

25 If the completion of TDH.VP.ENTER (i.e., exit from the TD guest) was due to TDCALL(TDG.VP.VMCALL), then the RCX input parameter of TDG.VP.VMCALL is designed to be used as a bitmap. It selects the GPRs (from RBX, RDX, RBP, RDI, RSI and R8 through R15) and XMM registers whose value is passed to the host VMM as the output of TDH.VP.ENTER. RCX itself is passed as-is to the output of TDH.VP.ENTER, and RAX[31:0] indicates the **VMCALL** exit reason (see below). See the TDG.VP.VMCALL description in 20.3.8.

If the completion of TDH.VP.ENTER was due to another reason, then other VMX-like Exit Information fields are provided in other GPRs. Details are provided in the TDH.VP.ENTER leaf function definition (see 20.2.31).

- 30 By design, any GPRs and extended states that do not return values as described above are set to synthetic values. If the VMM uses any of them, it must explicitly save them before TDH.VP.ENTER and restore them afterward.

#### 15.3.4.2. TD Synchronous Exit: TDG.VP.VMCALL

##### Transfer of TD Guest State to Host VMM

35 In the case of a TDG.VP.VMCALL leaf function, the RCX input parameter of TDG.VP.VMCALL is designed to be used as a bitmap. It selects the GPRs (from RBX, RDX, RBP, RDI, RSI and R8 through R15) and XMM registers whose value is passed to the host VMM as the output of TDH.VP.ENTER. RCX itself is passed as-is to the output of TDH.VP.ENTER.

RAX provides TDH.VP.ENTER completion status (see above). All other CPU state components, including GPRs and XMM registers not selected by RCX, are saved in TDVPS and set to fixed values (see 19.2). The value of RCX itself is also saved to TDVPS.

### Output State (Back to the Guest TD)

On completion of TDG.VP.VMCALL, a success – indicated by the ERROR bit (RAX[63]) being 0 – means that a SEAMRET into the VMM was successful. The VMM ran for some and then executed TDH.VP.ENTER successfully (possibly on another LP). The Intel TDX module executed VMRESUME successfully, transferring control to the instruction following TDCALL.

- 5 In this case, the RCX input parameter of TDG.VP.VMCALL is designed to be used as a bitmap. It selects the GPRs (from RBX, RDX, RBP, RDI, RSI and R8 through R15) and XMM registers whose value reflects their state as input to TDH.VP.ENTER. All other CPU states, including GPRs and XMM registers not selected by RCX, are restored from TDVPS.

## SECTION 3: INTEL TDX APPLICATION BINARY INTERFACE (ABI) REFERENCE

This section serves as a detailed reference for the Intel TDX module ABI. This includes:

- 5 • CPU virtualization tables
- Constants
- Data types
- Variables
- Control structures
- 10 • functions

The reference contains software-visible details. It also contains some internal details at a level required for understanding the architecture.



## 16.ABI Reference: CPU Virtualization Tables

### 16.1. MSR Virtualization

Table 16.2 below describes how the Intel TDX module virtualizes MSRs to guest TDs. The table uses a notation that is described in Table 16.1 below.

5

**Table 16.1: MSR Virtualization Notation Definition**

Text	Virtualization
<b>Native</b>	Direct read or write from/to CPU
<b>Inject_GP(condition)</b>	TDX Module injects a #GP(0) if condition is true, else reads from CPU or write to CPU: <pre> if (condition)     #GP(0) else     Native                     </pre>
<b>Inject_GP_or_VE(condition)</b>	TDX Module injects a #GP(0) if condition is true, else it injects a #VE: <pre> if (condition)     #GP(0) else     #VE                     </pre>

For MSRs that are not listed in the table, the Intel TDX module injects a #VE on both RDMSR and WRMSR by the guest TD.

**Note:** The table below provides a high-level overview of MSR virtualization. Implementation details may differ.

10

**Table 16.2: MSR Virtualization**

MSR Index Range (Hex)			MSR Architectural Name	MSR Virtualization	
First (Hex)	Last (Hex)	Size (Hex)		On RDMSR	On WRMSR
0x10	0x10	0x1	IA32_TIME_STAMP_COUNTER	Native	#VE
0x48	0x48	0x1	IA32_SPEC_CTRL	Native	Native
0x49	0x49	0x1	IA32_PRED_CMD	Native	Native
0x87	0x87	0x1	IA32_MKTME_PARTITIONING	Inject_GP_or_VE (~virt. CPUID(7,0).EDX[18])	Inject_GP_or_VE (~virt. CPUID(7,0).EDX[18])
0x8C	0x8F	0x4	IA32_SGXLEPUBKEYHASHx	#GP(0)	#GP(0)
0x98	0x98	0x1	MSR_WBINVDP	Native	Native
0x99	0x99	0x1	MSR_WBNOINVDP	Native	Native
0x9A	0x9A	0x1	MSR_INTR_PENDING	Native	Native
0x9B	0x9B	0x1	IA32_SMM_MONITOR_CTL	#GP(0)	#GP(0)
0x9E	0x9E	0x1	IA32_SMBASE	#GP(0)	#GP(0)
0xC1	0xC8	0x8	IA32_PMCx	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)
0xE1	0xE1	0x1	IA32_UMWAIT_CONTROL	Inject_GP(~virt. CPUID(7,0).ECX[5])	Inject_GP(~virt. CPUID(7,0).ECX[5])
0x10A	0x10A	0x1	IA32_ARCH_CAPABILITIES	Native	Native
0x10B	0x10B	0x1	IA32_FLUSH_CMD	Native	Native
0x174	0x174	0x1	IA32_SYSENTER_CS	Native	Native
0x175	0x175	0x1	IA32_SYSENTER_ESP	Native	Native
0x176	0x176	0x1	IA32_SYSENTER_EIP	Native	Native
0x186	0x18D	0x8	IA32_PERFVTSELx	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)

MSR Index Range (Hex)			MSR Architectural Name	MSR Virtualization	
First (Hex)	Last (Hex)	Size (Hex)		On RDMSR	On WRMSR
0x1A0	0x1A0	0x1	IA32_MISC_ENABLE	if ~PERFMON RDMSR current value Indicate Perfmon and PEBS are unavailable: Bit 7 = 0 Bit 12 = 1 else Native	#VE
0x1A6	0x1A7	0x2	MSR_OFFCORE_RSPx	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)
0x1C4	0x1C4	0x1	IA32_XFD	Inject_GP(~(virt. CPUID(0xD,0x1).EAX[4]))	Inject_GP(~(virt. CPUID(0xD,0x1).EAX[4]))
0x1C5	0x1C5	0x1	IA32_XFD_ERR	Inject_GP(~(virt. CPUID(0xD,0x1).EAX[4]))	Inject_GP(~(virt. CPUID(0xD,0x1).EAX[4]))
0x1D9	0x1D9	0x1	IA32_DEBUGCTL	Clear ENABLE_UNCORE_PMI (bit 13)	#GP if illegal, #VE if value is not supported for TD
0x1F8	0x1F8	0x1	IA32_PLATFORM_DCA_CAP	Inject_GP_or_VE( ~virt. CPUID(0x1).ECX[18])	Inject_GP_or_VE( ~virt. CPUID(0x1).ECX[18])
0x1F9	0x1F9	0x1	IA32_CPU_DCA_CAP	Inject_GP_or_VE( ~virt. CPUID(0x1).ECX[18])	Inject_GP_or_VE( ~virt. CPUID(0x1).ECX[18])
0x1FA	0x1FA	0x1	IA32_DCA_0_CAP	Inject_GP_or_VE( ~virt. CPUID(0x1).ECX[18])	Inject_GP_or_VE( ~virt. CPUID(0x1).ECX[18])
0x277	0x277	0x1	IA32_PAT	Native	Native
0x309	0x30C	0x4	IA32_FIXED_CTRx	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)
0x329	0x329	0x1	IA32_PERF_METRICS	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)
0x345	0x345	0x1	IA32_PERF_CAPABILITIES	if ~PERFMON return 0 else if ~XFAM[8] clear bit 16 else Native	Inject_GP(~PERFMON)
0x38D	0x38D	0x1	IA32_FIXED_CTR_CTRL	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)
0x38E	0x38E	0x1	IA32_PERF_GLOBAL_STATUS	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)
0x38F	0x38F	0x1	IA32_PERF_GLOBAL_CTRL	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)
0x390	0x390	0x1	IA32_PERF_GLOBAL_STATUS_RESET	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)
0x391	0x391	0x1	IA32_PERF_GLOBAL_STATUS_SET	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)
0x392	0x392	0x1	IA32_PERF_GLOBAL_INUSE	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)
0x3F1	0x3F1	0x1	IA32_PEBBS_ENABLE	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)
0x3F2	0x3F2	0x1	MSR_PEBBS_DATA_CFG	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)
0x3F6	0x3F6	0x1	MSR_PEBBS_LD_LAT	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)
0x3F7	0x3F7	0x1	MSR_PEBBS_FRONTEND	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)
0x480	0x480	0x1	IA32_VMX_BASIC	#GP(0)	#GP(0)
0x481	0x481	0x1	IA32_VMX_PINBASED_CTLs	#GP(0)	#GP(0)
0x482	0x482	0x1	IA32_VMX_PROCBASED_CTLs	#GP(0)	#GP(0)
0x483	0x483	0x1	IA32_VMX_EXIT_CTLs	#GP(0)	#GP(0)
0x484	0x484	0x1	IA32_VMX_ENTRY_CTLs	#GP(0)	#GP(0)
0x485	0x485	0x1	IA32_VMX_MISC	#GP(0)	#GP(0)
0x486	0x486	0x1	IA32_VMX_CR0_FIXED0	#GP(0)	#GP(0)
0x487	0x487	0x1	IA32_VMX_CR0_FIXED1	#GP(0)	#GP(0)
0x488	0x488	0x1	IA32_VMX_CR4_FIXED0	#GP(0)	#GP(0)

MSR Index Range (Hex)			MSR Architectural Name	MSR Virtualization	
First (Hex)	Last (Hex)	Size (Hex)		On RDMSR	On WRMSR
0x489	0x489	0x1	IA32_VMX_CR4_FIXED1	#GP(0)	#GP(0)
0x48A	0x48A	0x1	IA32_VMX_VMCS_ENUM	#GP(0)	#GP(0)
0x48B	0x48B	0x1	IA32_VMX_PROCBASED_CTL52	#GP(0)	#GP(0)
0x48C	0x48C	0x1	IA32_VMX_EPT_VPID_CAP	#GP(0)	#GP(0)
0x48D	0x48D	0x1	IA32_VMX_TRUE_PINBASED_CTL5	#GP(0)	#GP(0)
0x48E	0x48E	0x1	IA32_VMX_TRUE_PROCBASED_CTL5	#GP(0)	#GP(0)
0x48F	0x48F	0x1	IA32_VMX_TRUE_EXIT_CTL5	#GP(0)	#GP(0)
0x490	0x490	0x1	IA32_VMX_TRUE_ENTRY_CTL5	#GP(0)	#GP(0)
0x491	0x491	0x1	IA32_VMX_VMFUNC	#GP(0)	#GP(0)
0x492	0x492	0x1	IA32_VMX_PROCBASED_CTL53	#GP(0)	#GP(0)
0x4C1	0x4C8	0x8	IA32_A_PMCx	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)
0x500	0x500	0x1	IA32_SGX_SVN_STATUS	#GP(0)	#GP(0)
0x560	0x560	0x1	IA32_RTIT_OUTPUT_BASE	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])
0x561	0x561	0x1	IA32_RTIT_OUTPUT_MASK_PTR5	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])
0x570	0x570	0x1	IA32_RTIT_CTL	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])
0x571	0x571	0x1	IA32_RTIT_STATUS	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])
0x572	0x572	0x1	IA32_RTIT_CR3_MATCH	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])
0x580	0x580	0x1	IA32_RTIT_ADDR0_A	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])
0x581	0x581	0x1	IA32_RTIT_ADDR0_B	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])
0x582	0x582	0x1	IA32_RTIT_ADDR1_A	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])
0x583	0x583	0x1	IA32_RTIT_ADDR1_B	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])
0x584	0x584	0x1	IA32_RTIT_ADDR2_A	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])
0x585	0x585	0x1	IA32_RTIT_ADDR2_B	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])
0x586	0x586	0x1	IA32_RTIT_ADDR3_A	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])
0x587	0x587	0x1	IA32_RTIT_ADDR3_B	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])
0x600	0x600	0x1	IA32_DS_AREA	Native	Native
0x6A0	0x6A0	0x1	IA32_U_CET	Inject_GP(~(XFAM[11]   XFAM[12]))	Inject_GP(~(XFAM[11]   XFAM[12]))
0x6A2	0x6A2	0x1	IA32_S_CET	Inject_GP(~(XFAM[11]   XFAM[12]))	Inject_GP(~(XFAM[11]   XFAM[12]))
0x6A4	0x6A4	0x1	IA32_PLO_SSP	Inject_GP(~(XFAM[11]   XFAM[12]))	Inject_GP(~(XFAM[11]   XFAM[12]))
0x6A5	0x6A5	0x1	IA32_PL1_SSP	Inject_GP(~(XFAM[11]   XFAM[12]))	Inject_GP(~(XFAM[11]   XFAM[12]))
0x6A6	0x6A6	0x1	IA32_PL2_SSP	Inject_GP(~(XFAM[11]   XFAM[12]))	Inject_GP(~(XFAM[11]   XFAM[12]))
0x6A7	0x6A7	0x1	IA32_PL3_SSP	Inject_GP(~(XFAM[11]   XFAM[12]))	Inject_GP(~(XFAM[11]   XFAM[12]))
0x6A8	0x6A8	0x1	IA32_INTERRUPT_SSP_TABLE_ADDR	Inject_GP(~(XFAM[11]   XFAM[12]))	Inject_GP(~(XFAM[11]   XFAM[12]))
0x6E1	0x6E1	0x1	IA32_PKRS	Inject_GP(~PKS)	Inject_GP(~PKS)
0x800	0x801	0x2	Reserved for xAPIC MSRs	#GP(0)	#GP(0)
0x804	0x807	0x4	Reserved for xAPIC MSRs	#GP(0)	#GP(0)
0x808	0x808	0x1	IA32_X2APIC_TPR	Native	Native
0x809	0x809	0x1	Reserved for xAPIC MSRs	Native	Native
0x80A	0x80A	0x1	IA32_X2APIC_PPR	Native	Native
0x80B	0x80B	0x1	IA32_X2APIC_EOI	Native	Native
0x80C	0x80C	0x1	Reserved for xAPIC MSRs	Native	Native
0x80E	0x80E	0x1	Reserved for xAPIC MSRs	Native	Native

MSR Index Range (Hex)			MSR Architectural Name	MSR Virtualization	
First (Hex)	Last (Hex)	Size (Hex)		On RDMSR	On WRMSR
0x810	0x817	0x8	IA32_X2APIC_ISRx	Native	Native
0x818	0x81F	0x8	IA32_X2APIC_TMRx	Native	Native
0x820	0x827	0x8	IA32_X2APIC_IRRx	Native	Native
0x83F	0x83F	0x1	IA32_X2APIC_SELF_IPI	Native	Native
0x840	0x87F	0x40	Reserved for xAPIC MSRs	#GP(0)	#GP(0)
0x880	0x8BF	0x40	Reserved for xAPIC MSRs	#GP(0)	#GP(0)
0x8C0	0x8FF	0x40	Reserved for xAPIC MSRs	#GP(0)	#GP(0)
0x981	0x981	0x1	IA32_TME_CAPABILITY	Inject_GP_or_VE (~virt. CPUID(7,0).ECX[13])	Inject_GP_or_VE (~virt. CPUID(7,0).ECX[13])
0x982	0x982	0x1	IA32_TME_ACTIVATE	Inject_GP_or_VE (~virt. CPUID(7,0).ECX[13])	Inject_GP_or_VE (~virt. CPUID(7,0).ECX[13])
0x983	0x983	0x1	IA32_TME_EXCLUDE_MASK	Inject_GP_or_VE (~virt. CPUID(7,0).ECX[13])	Inject_GP_or_VE (~virt. CPUID(7,0).ECX[13])
0x984	0x984	0x1	IA32_TME_EXCLUDE_BASE	Inject_GP_or_VE (~virt. CPUID(7,0).ECX[13])	Inject_GP_or_VE (~virt. CPUID(7,0).ECX[13])
0x985	0x985	0x1	IA32_UINT_RR	Inject_GP(~XFAM[14])	Inject_GP(~XFAM[14])
0x986	0x986	0x1	IA32_UINT_HANDLER	Inject_GP(~XFAM[14])	Inject_GP(~XFAM[14])
0x987	0x987	0x1	IA32_UINT_STACKADJUST	Inject_GP(~XFAM[14])	Inject_GP(~XFAM[14])
0x988	0x988	0x1	IA32_UINT_MISC	Inject_GP(~XFAM[14])	Inject_GP(~XFAM[14])
0x989	0x989	0x1	IA32_UINT_PD	Inject_GP(~XFAM[14])	Inject_GP(~XFAM[14])
0x98A	0x98A	0x1	IA32_UINT_TT	Inject_GP(~XFAM[14])	Inject_GP(~XFAM[14])
0xC80	0xC80	0x1	IA32_DEBUG_INTERFACE	Native	#VE
0xD90	0xD90	0x1	IA32_BNDCFGS	#GP(0)	#GP(0)
0xD93	0xD93	0x1	IA32_PASID	#GP(0)	#GP(0)
0xDA0	0xDA0	0x1	IA32_XSS	Native	if illegal or does not match XFAM #GP(0) else Write to CPU
0x1200	0x12FF	0x100	IA32_LBR_INFO	Inject_GP(~XFAM[15])	Inject_GP(~XFAM[15])
0x14CE	0x14CE	0x1	IA32_LBR_CTL	Inject_GP(~XFAM[15])	Inject_GP(~XFAM[15])
0x14CF	0x14CF	0x1	IA32_LBR_DEPTH	Inject_GP(~XFAM[15])	Inject_GP(~XFAM[15])
0x1500	0x15FF	0x100	IA32_LBR_FROM_IP	Inject_GP(~XFAM[15])	Inject_GP(~XFAM[15])
0x1600	0x16FF	0x100	IA32_LBR_TO_IP	Inject_GP(~XFAM[15])	Inject_GP(~XFAM[15])
0xC0000080	0xC0000080	0x1	IA32_EFER	Native	#VE
0xC0000081	0xC0000081	0x1	IA32_STAR	Native	Native
0xC0000082	0xC0000082	0x1	IA32_LSTAR	Native	Native
0xC0000084	0xC0000084	0x1	IA32_FMASK	Native	Native
0xC0000100	0xC0000100	0x1	IA32_FSBASE	Native	Native
0xC0000101	0xC0000101	0x1	IA32_GSBASE	Native	Native
0xC0000102	0xC0000102	0x1	IA32_KERNEL_GS_BASE	Native	Native
0xC0000103	0xC0000103	0x1	IA32_TSC_AUX	Native	Native

## 16.2. CPUID Virtualization

Table 16.4 below describes how the Intel TDX module virtualizes CPUID to guest TDs. Note the following:

- The “Configuration by TDH.MNG.INIT” column details which section of the TD\_PARAMS structure is used for configuring how each CPUID bit field is virtualized.
- The “Virtualization” column uses a notation defined in Table 16.3 below.
- If the guest TD executes CPUID with a valid leaf / sub-leaf number combination that is not listed in the table, the Intel TDX module injects a #VE.
- The host VMM should always consult the list of CPUID leaves and sub-leaves configured by TD\_PARAMS.CPUID\_CONFIG, as enumerated by TDH.SYS.INFO, described in 12.1.3.3.

**Table 16.3: CPUID Virtualization Notation Definition**

CPUID Bit Field Virtualization	Meaning	Virtualization Details
As Configured	Virtual bit field value reflects the host VMM configuration.	
As Configured (if Native)	If the native bit field value returned by executing CPUID is 0, then the virtual bit field value is 0. Else, the virtual bit field value reflects the host VMM configuration.	
Calculated	Bit field is calculated by the Intel TDX module.	Calculation method
Fixed	The virtual bit field value is fixed.	Bit field value
Native	The virtual bit field value reflects the native value returned by executing CPUID.	

**Note:** The table below provides a high-level overview of CPUID virtualization. Implementation details may differ.

**Table 16.4: CPUID Virtualization Overview**

CPUID Field					Configuration by TDH.MNG.INIT		Virtualization	
Reg.	MSB	LSB	Field Size	Field Name	TD_PARAMS Section	Configuration Details	Virtualization Type	Virtualization Details
<b>Leaf 0x0</b>								
EAX	31	0	32	MaxIndex	N/A		Native	
EBX	31	0	32	Genu	N/A		Native	
ECX	31	0	32	ntel	N/A		Native	
EDX	31	0	32	inel	N/A		Native	
<b>Leaf 0x1</b>								
EAX	3	0	4	Stepping ID	N/A		Calculated	Min. of all packages
EAX	7	4	4	Model ID	N/A		Native	
EAX	11	8	4	Family ID	N/A		Native	
EAX	13	12	2	Processor Type	N/A		Native	
EAX	15	14	2	Reserved_15_14	N/A		Fixed	0x0
EAX	19	16	4	Extended Model ID	N/A		Native	
EAX	27	20	8	Extended Family ID	N/A		Native	
EAX	31	28	4	Reserved_31_28	N/A		Fixed	0x0
EBX	7	0	8	Brand Index	N/A		Native	
EBX	15	8	8	CLFLUSH Line Size	N/A		Fixed	0x8
EBX	23	16	8	Maximum Addressable IDs	CPUID_CONFIG		As Configured	
EBX	31	24	8	Initial APIC ID	N/A		Calculated	TDVPS.VCPU_INDEX[7:0]
ECX	0	0	1	SSE3	N/A		Native	
ECX	1	1	1	PCLMULQDQ	N/A		Native	
ECX	2	2	1	DTES64	N/A		Native	
ECX	3	3	1	MONITOR	N/A		Fixed	0x0
ECX	4	4	1	DS-CPL	N/A		Native	
ECX	5	5	1	VMX	N/A		Fixed	0x0
ECX	6	6	1	SMX	N/A		Fixed	0x0
ECX	7	7	1	EST	CPUID_CONFIG		As Configured (if Native)	
ECX	8	8	1	TM2	CPUID_CONFIG		As Configured (if Native)	
ECX	9	9	1	SSSE3	N/A		Native	
ECX	10	10	1	CNXT-ID	N/A		Native	
ECX	11	11	1	SDBG	N/A		Native	
ECX	12	12	1	FMA	XFAM	XFAM[2]	As Configured (if Native)	
ECX	13	13	1	CMPXCHG16B	N/A		Fixed	0x1

CPUID Field					Configuration by TDH.MNG.INIT		Virtualization	
Reg.	MSB	LSB	Field Size	Field Name	TD_PARAMS Section	Configuration Details	Virtualization Type	Virtualization Details
ECX	14	14	1	xTPR Update Control	CPUID_CONFIG		As Configured (if Native)	
ECX	15	15	1	PDCM	N/A		Fixed	0x1
ECX	16	16	1	Reserved_16	N/A		Fixed	0x0
ECX	17	17	1	PCID	N/A		Native	
ECX	18	18	1	DCA	CPUID_CONFIG		As Configured (if Native)	
ECX	19	19	1	SSE4_1	N/A		Native	
ECX	20	20	1	SSE4_2	N/A		Native	
ECX	21	21	1	x2APIC	N/A		Fixed	0x1
ECX	22	22	1	MOVBE	N/A		Native	
ECX	23	23	1	POPCNT	N/A		Native	
ECX	24	24	1	TSC-Deadline	N/A		Native	
ECX	25	25	1	AESNI	N/A		Fixed	0x1
ECX	26	26	1	XSAVE	N/A		Fixed	0x1
ECX	27	27	1	OSXSAVE	N/A		Calculated	CR4.OSXSAVE
ECX	28	28	1	AVX	XFAM	XFAM[2]	As Configured (if Native)	
ECX	29	29	1	F16C	XFAM	XFAM[2]	As Configured (if Native)	
ECX	30	30	1	RDRAND	N/A		Fixed	0x1
ECX	31	31	1	Reserved_31	N/A		Fixed	0x1
EDX	0	0	1	FPU	N/A		Native	
EDX	1	1	1	VME	N/A		Native	
EDX	2	2	1	DE	N/A		Native	
EDX	3	3	1	PSE	N/A		Native	
EDX	4	4	1	TSC	N/A		Native	
EDX	5	5	1	MSR	N/A		Fixed	0x1
EDX	6	6	1	PAE	N/A		Fixed	0x1
EDX	7	7	1	MCE	N/A		Fixed	0x1
EDX	8	8	1	CX8	N/A		Native	
EDX	9	9	1	APIC	N/A		Fixed	0x1
EDX	10	10	1	Reserved_10	N/A		Fixed	0x0
EDX	11	11	1	SEP	N/A		Native	
EDX	12	12	1	MTRR	N/A		Fixed	0x1
EDX	13	13	1	PGE	N/A		Native	
EDX	14	14	1	MCA	N/A		Fixed	0x1
EDX	15	15	1	CMOV	N/A		Native	
EDX	16	16	1	PAT	N/A		Native	
EDX	17	17	1	PSE-36	N/A		Native	
EDX	18	18	1	PSN	N/A		Native	
EDX	19	19	1	CLFSH	N/A		Fixed	0x1
EDX	20	20	1	Reserved_20	N/A		Fixed	0x0
EDX	21	21	1	DS	N/A		Fixed	0x1
EDX	22	22	1	ACPI	CPUID_CONFIG		As Configured (if Native)	
EDX	23	23	1	MMX	N/A		Native	
EDX	24	24	1	FXSR	N/A		Native	
EDX	25	25	1	SSE	N/A		Native	
EDX	26	26	1	SSE2	N/A		Native	
EDX	27	27	1	SS	N/A		Native	
EDX	28	28	1	HTT	CPUID_CONFIG		As Configured (if Native)	
EDX	29	29	1	TM	CPUID_CONFIG		As Configured (if Native)	
EDX	30	30	1	Reserved_30	N/A		Fixed	0x0
EDX	31	31	1	PBE	CPUID_CONFIG		As Configured (if Native)	
<b>Leaf 0x3</b>								
EAX	31	0	32	Reserved	N/A		Fixed	0x0
EBX	31	0	32	Reserved	N/A		Fixed	0x0
ECX	31	0	32	Reserved	N/A		Fixed	0x0
EDX	31	0	32	Reserved	N/A		Fixed	0x0
<b>Leaf 0x4 / Sub-Leaf 0x0</b>								
EAX	4	0	5	Type	CPUID_CONFIG		As Configured	
EAX	7	5	3	Level	CPUID_CONFIG		As Configured	
EAX	8	8	1	Self Initializing	CPUID_CONFIG		As Configured	
EAX	9	9	1	Fully Associative	CPUID_CONFIG		As Configured	
EAX	13	10	4	Reserved	CPUID_CONFIG		As Configured	
EAX	25	14	12	Addressable IDs Sharing this Cache	CPUID_CONFIG		As Configured	
EAX	31	26	6	Addressable IDs for Cores in Package	CPUID_CONFIG		As Configured	
EBX	11	0	12	L	N/A		Native	
EBX	21	12	10	P	CPUID_CONFIG		As Configured	
EBX	31	22	10	W	CPUID_CONFIG		As Configured	
ECX	31	0	32	Number of Sets	CPUID_CONFIG		As Configured	
EDX	0	0	1	WBINVD	CPUID_CONFIG		As Configured	

CPUID Field					Configuration by TDH.MNG.INIT		Virtualization	
Reg.	MSB	LSB	Field Size	Field Name	TD_PARAMS Section	Configuration Details	Virtualization Type	Virtualization Details
EDX	1	1	1	Cache Inclusiveness	CPUID_CONFIG		As Configured	
EDX	2	2	1	Reserved_31_2	CPUID_CONFIG		As Configured	
EDX	31	3	29	0	CPUID_CONFIG		As Configured	
<b>Leaf 0x4 / Sub-Leaf 0x1</b>								
EAX	4	0	5	Type	CPUID_CONFIG		As Configured	
EAX	7	5	3	Level	CPUID_CONFIG		As Configured	
EAX	8	8	1	Self Initializing	CPUID_CONFIG		As Configured	
EAX	9	9	1	Fully Associative	CPUID_CONFIG		As Configured	
EAX	13	10	4	Reserved	CPUID_CONFIG		As Configured	
EAX	25	14	12	Addressable IDs Sharing this Cache	CPUID_CONFIG		As Configured	
EAX	31	26	6	Addressable IDs for Cores in Package	CPUID_CONFIG		As Configured	
EBX	11	0	12	L	N/A		Native	
EBX	21	12	10	P	CPUID_CONFIG		As Configured	
EBX	31	22	10	W	CPUID_CONFIG		As Configured	
ECX	31	0	32	Number of Sets	CPUID_CONFIG		As Configured	
EDX	0	0	1	WBINVD	CPUID_CONFIG		As Configured	
EDX	1	1	1	Cache Inclusiveness	CPUID_CONFIG		As Configured	
EDX	2	2	1	Reserved_31_2	CPUID_CONFIG		As Configured	
EDX	31	3	29	0	CPUID_CONFIG		As Configured	
<b>Leaf 0x4 / Sub-Leaf 0x2</b>								
EAX	4	0	5	Type	CPUID_CONFIG		As Configured	
EAX	7	5	3	Level	CPUID_CONFIG		As Configured	
EAX	8	8	1	Self Initializing	CPUID_CONFIG		As Configured	
EAX	9	9	1	Fully Associative	CPUID_CONFIG		As Configured	
EAX	13	10	4	Reserved_13_10	CPUID_CONFIG		As Configured	
EAX	25	14	12	Addressable IDs Sharing this Cache	CPUID_CONFIG		As Configured	
EAX	31	26	6	Addressable IDs for Cores in Package	CPUID_CONFIG		As Configured	
EBX	11	0	12	L	N/A		Native	
EBX	21	12	10	P	CPUID_CONFIG		As Configured	
EBX	31	22	10	W	CPUID_CONFIG		As Configured	
ECX	31	0	32	Number of Sets	CPUID_CONFIG		As Configured	
EDX	0	0	1	WBINVD	CPUID_CONFIG		As Configured	
EDX	1	1	1	Cache Inclusiveness	CPUID_CONFIG		As Configured	
EDX	2	2	1	Reserved_31_2	CPUID_CONFIG		As Configured	
EDX	31	3	29	0	CPUID_CONFIG		As Configured	
<b>Leaf 0x4 / Sub-Leaf 0x3</b>								
EAX	4	0	5	Type	CPUID_CONFIG		As Configured	
EAX	7	5	3	Level	CPUID_CONFIG		As Configured	
EAX	8	8	1	Self Initializing	CPUID_CONFIG		As Configured	
EAX	9	9	1	Fully Associative	CPUID_CONFIG		As Configured	
EAX	13	10	4	Reserved_13_10	CPUID_CONFIG		As Configured	
EAX	25	14	12	Addressable IDs Sharing this Cache	CPUID_CONFIG		As Configured	
EAX	31	26	6	Addressable IDs for Cores in Package	CPUID_CONFIG		As Configured	
EBX	11	0	12	L	N/A		Native	
EBX	21	12	10	P	CPUID_CONFIG		As Configured	
EBX	31	22	10	W	CPUID_CONFIG		As Configured	
ECX	31	0	32	Number of Sets	CPUID_CONFIG		As Configured	
EDX	0	0	1	WBINVD	CPUID_CONFIG		As Configured	
EDX	1	1	1	Cache Inclusiveness	CPUID_CONFIG		As Configured	
EDX	2	2	1	Complex cache indexing	CPUID_CONFIG		As Configured	
EDX	31	3	29	Reserved_31_3	CPUID_CONFIG		As Configured	
<b>Leaf 0x4 / Sub-Leaf 0x4</b>								
EAX	4	0	5	Type	N/A		Fixed	0x0
EAX	7	5	3	Level	N/A		Fixed	0x0
EAX	8	8	1	Self Initializing	N/A		Fixed	0x0
EAX	9	9	1	Fully Associative	N/A		Fixed	0x0
EAX	13	10	4	Reserved	N/A		Fixed	0x0
EAX	25	14	12	Addressable IDs Sharing this Cache	N/A		Fixed	0x0
EAX	31	26	6	Addressable IDs for Cores in Package	N/A		Fixed	0x0
EBX	11	0	12	L	N/A		Fixed	0x0
EBX	21	12	10	P	N/A		Fixed	0x0
EBX	31	22	10	W	N/A		Fixed	0x0
ECX	31	0	32	Number of Sets	N/A		Fixed	0x0
EDX	0	0	1	WBINVD	N/A		Fixed	0x0
EDX	1	1	1	Cache Inclusiveness	N/A		Fixed	0x0
EDX	2	2	1	Complex Cache Indexing	N/A		Fixed	0x0
EDX	31	3	29	Reserved	N/A		Fixed	0x0
<b>Leaf 0x7 / Sub-Leaf 0x0</b>								

CPUID Field					Configuration by TDH.MNG.INIT		Virtualization	
Reg.	MSB	LSB	Field Size	Field Name	TD_PARAMS Section	Configuration Details	Virtualization Type	Virtualization Details
EAX	31	0	32	Max Sub-Leaves	N/A		Fixed	0x1
EBX	0	0	1	FSGSBASE	N/A		Fixed	0x1
EBX	1	1	1	IA32_TSC_ADJUST	N/A		Fixed	0x0
EBX	2	2	1	SGX	N/A		Fixed	0x0
EBX	3	3	1	BMI1	CPUID_CONFIG		As Configured (if Native)	
EBX	4	4	1	HLE	N/A		Native	
EBX	5	5	1	AVX2	XFAM	XFAM[2]	As Configured (if Native)	
EBX	6	6	1	FDP_EXCPTN_ONLY	N/A		Native	
EBX	7	7	1	SMEP	N/A		Native	
EBX	8	8	1	BMI2	CPUID_CONFIG		As Configured (if Native)	
EBX	9	9	1	Enhanced REP MOVSB/STOSB	N/A		Native	
EBX	10	10	1	INVPCID	N/A		Native	
EBX	11	11	1	RTM	N/A		Fixed	0x1
EBX	12	12	1	PQM	CPUID_CONFIG		As Configured (if Native)	
EBX	13	13	1	FCS/FDS Deprecation	N/A		Native	
EBX	14	14	1	MPX	N/A		Fixed	0x0
EBX	15	15	1	Cache QoS Enforcement	CPUID_CONFIG		As Configured (if Native)	
EBX	16	16	1	AVX512F	XFAM	XFAM[7:5]	As Configured (if Native)	
EBX	17	17	1	AVX512DQ	XFAM	XFAM[7:5]	As Configured (if Native)	
EBX	18	18	1	RDSEED	N/A		Fixed	0x1
EBX	19	19	1	ADCX/ADOX	CPUID_CONFIG		As Configured (if Native)	
EBX	20	20	1	SMAP/CLAC/STAC	N/A		Fixed	0x1
EBX	21	21	1	AVX512_IFMA	XFAM	XFAM[7:5]	As Configured (if Native)	
EBX	22	22	1	PCOMMIT	N/A		Native	
EBX	23	23	1	CLFLUSHOPT	N/A		Fixed	0x1
EBX	24	24	1	CLWB	N/A		Fixed	0x1
EBX	25	25	1	RTIT	XFAM	XFAM[8]	As Configured (if Native)	
EBX	26	26	1	AVX512PF	XFAM	XFAM[7:5]	As Configured (if Native)	
EBX	27	27	1	AVX512ER	XFAM	XFAM[7:5]	As Configured (if Native)	
EBX	28	28	1	AVX512CD	XFAM	XFAM[7:5]	As Configured (if Native)	
EBX	29	29	1	SHA	N/A		Fixed	0x1
EBX	30	30	1	AVX512BW	XFAM	XFAM[7:5]	As Configured (if Native)	
EBX	31	31	1	AVX512VL	XFAM	XFAM[7:5]	As Configured (if Native)	
ECX	0	0	1	PREFETCHWT1	N/A		Native	
ECX	1	1	1	AVX512VBMI	XFAM	XFAM[7:5]	As Configured (if Native)	
ECX	2	2	1	UMIP	N/A		Native	
ECX	3	3	1	PKU	XFAM	XFAM[9]	As Configured (if Native)	
ECX	4	4	1	OSPKE	N/A		Calculated	CR4.PKE
ECX	5	5	1	MONITORX/MWAITX	CPUID_CONFIG		As Configured (if Native)	
ECX	6	6	1	AVX512_VBMI2	XFAM	XFAM[7:5]	As Configured (if Native)	
ECX	7	7	1	CET Shadow Stack	XFAM	XFAM[12:11]	As Configured (if Native)	
ECX	8	8	1	GFNI	N/A		Native	
ECX	9	9	1	VAES	XFAM	XFAM[2]	As Configured (if Native)	
ECX	10	10	1	VPCLMULQDQ	XFAM	XFAM[2]	As Configured (if Native)	
ECX	11	11	1	AVX512_VNNI	XFAM	XFAM[7:5]	As Configured (if Native)	
ECX	12	12	1	AVX512_BITALG	XFAM	XFAM[7:5]	As Configured (if Native)	
ECX	13	13	1	TME	CPUID_CONFIG		As Configured (if Native)	
ECX	14	14	1	AVX512_VPOPCNTDQ	XFAM	XFAM[7:5]	As Configured (if Native)	
ECX	15	15	1	FZM	N/A		Fixed	0x0
ECX	16	16	1	57 bit Address Support	N/A		Native	
ECX	21	17	5	MAWAU for MPX	N/A		Fixed	0x0
ECX	22	22	1	RDPID	N/A		Native	
ECX	23	23	1	KL_ENABLED	ATTRIBUTES	KL	As Configured (if Native)	
ECX	24	24	1	BUSLOCK	N/A		Native	
ECX	25	25	1	CLDEMOTE	N/A		Native	
ECX	26	26	1	MPRR	N/A		Native	
ECX	27	27	1	MOVDIRI	N/A		Native	
ECX	28	28	1	MOVDIR64B	N/A		Fixed	0x1
ECX	29	29	1	ENQCMD	N/A		Fixed	0x0
ECX	30	30	1	SGX_LC	N/A		Fixed	0x0
ECX	31	31	1	PKS	ATTRIBUTES	PKS	As Configured (if Native)	
EDX	0	0	1	SGX_TEM	N/A		Fixed	0x0
EDX	1	1	1	SGX_KEYS	N/A		Fixed	0x0
EDX	2	2	1	AVX512_4VNNI	XFAM	XFAM[7:5]	As Configured (if Native)	
EDX	3	3	1	AVX512_4FMAPS	XFAM	XFAM[7:5]	As Configured (if Native)	
EDX	4	4	1	Fast Short REP MOV	N/A		Native	
EDX	5	5	1	ULI	XFAM	XFAM[14]	As Configured (if Native)	
EDX	6	6	1	Reserved_6	N/A		Fixed	0x0



CPUID Field					Configuration by TDH.MNG.INIT		Virtualization	
Reg.	MSB	LSB	Field Size	Field Name	TD_PARAMS Section	Configuration Details	Virtualization Type	Virtualization Details
EDX	7	7	1	Reserved_7	N/A		Fixed	0x0
EDX	8	8	1	AVX512_VP2INTERSECT	XFAM	XFAM[7:5]	As Configured (if Native)	
EDX	9	9	1	Reserved_9	N/A		Fixed	0x0
EDX	10	10	1	MD_CLEAR supported	N/A		Native	
EDX	11	11	1	Reserved_11	N/A		Fixed	0x0
EDX	12	12	1	Reserved_12	N/A		Fixed	0x0
EDX	13	13	1	Reserved_13	N/A		Fixed	0x0
EDX	14	14	1	SERIALIZE Inst	N/A		Native	
EDX	15	15	1	Hetero Part	N/A		Native	
EDX	16	16	1	TSXLDTRK	N/A		Native	
EDX	17	17	1	Reserved_17	N/A		Fixed	0x0
EDX	18	18	1	PCONFIG	CPUID_CONFIG		As Configured (if Native)	
EDX	19	19	1	Architectural LBR support	XFAM	XFAM[15]	As Configured (if Native)	
EDX	20	20	1	CET	XFAM	XFAM[12:11]	As Configured (if Native)	
EDX	21	21	1	Reserved_21	N/A		Fixed	0x0
EDX	22	22	1	TMUL_AMX-BF16	XFAM	XFAM[18:17]	As Configured (if Native)	
EDX	23	23	1	FP16	XFAM	XFAM[7:5]	As Configured (if Native)	
EDX	24	24	1	TMUL_AMX-TILE	XFAM	XFAM[18:17]	As Configured (if Native)	
EDX	25	25	1	TMUL_AMX-INT8	XFAM	XFAM[18:17]	As Configured (if Native)	
EDX	26	26	1	IBRS (indirect branch restricted speculation)	N/A		Fixed	0x1
EDX	27	27	1	STIBP (single thread indirect branch predictors)	N/A		Native	
EDX	28	28	1	L1D_FLUSH. IA32_FLUSH_CMD support.	N/A		Native	
EDX	29	29	1	IA32_ARCH_CAPABILITIES Support	N/A		Fixed	0x1
EDX	30	30	1	IA32_CORE_CAPABILITIES Present	N/A		Fixed	0x1
EDX	31	31	1	SSBD (Speculative Store Bypass Disable)	N/A		Fixed	0x1
<b>Leaf 0x7 / Sub-Leaf 0x1</b>								
EAX	2	0	3	Reserved_3_0	N/A		Fixed	0x0
EAX	3	3	1	Reserved_4	N/A		Fixed	0x0
EAX	4	4	1	ADL_VNNI	XFAM	XFAM[7:5]	As Configured (if Native)	
EAX	5	5	1	AVX512_BF16	XFAM	XFAM[7:5]	As Configured (if Native)	
EAX	6	6	1	Reserved_6	N/A		Fixed	0x0
EAX	7	7	1	Reserved_7	N/A		Fixed	0x0
EAX	8	8	1	Reserved_8	N/A		Fixed	0x0
EAX	9	9	1	DEDUP	N/A		Native	
EAX	10	10	1	Fast Zero-Length MOVSB	N/A		Native	
EAX	11	11	1	Fast Short STOSB	N/A		Native	
EAX	12	12	1	Fast short CMPSB/SCASB	N/A		Native	
EAX	21	13	9	Reserved_21_13	N/A		Fixed	0x0
EAX	22	22	1	HRESET	N/A		Fixed	0x0
EAX	23	23	1	Reserved_23	N/A		Fixed	0x0
EAX	24	24	1	Reserved_24	N/A		Fixed	0x0
EAX	31	25	7	Reserved_31_25	N/A		Fixed	0x0
EBX	31	0	32	Reserved	N/A		Fixed	0x0
ECX	31	0	32	Reserved	N/A		Fixed	0x0
EDX	31	0	32	Reserved	N/A		Fixed	0x0
<b>Leaf 0x8</b>								
EAX	31	0	32	Reserved	N/A		Fixed	0x0
EBX	31	0	32	Reserved	N/A		Fixed	0x0
ECX	31	0	32	Reserved	N/A		Fixed	0x0
EDX	31	0	32	Reserved	N/A		Fixed	0x0
<b>Leaf 0xa</b>								
EAX	7	0	8	Version	ATTRIBUTES	PERFMON	As Configured (if Native)	
EAX	15	8	8	Number of GP Counters	ATTRIBUTES	PERFMON	As Configured (if Native)	
EAX	23	16	8	Width of GP Counters	ATTRIBUTES	PERFMON	As Configured (if Native)	
EAX	31	24	8	Length of EBX Vector	ATTRIBUTES	PERFMON	As Configured (if Native)	
EBX	0	0	1	Core Cycles Not Available	ATTRIBUTES	PERFMON	As Configured (if Native)	
EBX	1	1	1	Instructions Retired Not Available	ATTRIBUTES	PERFMON	As Configured (if Native)	
EBX	2	2	1	Reference Cycles Not Available	ATTRIBUTES	PERFMON	As Configured (if Native)	
EBX	3	3	1	Last-Level Cache References Not Available	ATTRIBUTES	PERFMON	As Configured (if Native)	
EBX	4	4	1	Last-Level Cache Misses Not Available	ATTRIBUTES	PERFMON	As Configured (if Native)	
EBX	5	5	1	Branch Instruction Retired Not Available	ATTRIBUTES	PERFMON	As Configured (if Native)	
EBX	6	6	1	Branch Mispredict Retired Not Available	ATTRIBUTES	PERFMON	As Configured (if Native)	
EBX	31	7	25	Reserved	ATTRIBUTES	PERFMON	As Configured (if Native)	
ECX	3	0	4	Fixed Counter Support	ATTRIBUTES	PERFMON	As Configured (if Native)	
ECX	31	4	28	Reserved	ATTRIBUTES	PERFMON	As Configured (if Native)	
EDX	4	0	5	Number of Fixed-Function Counters	ATTRIBUTES	PERFMON	As Configured (if Native)	
EDX	12	5	8	Width of Fixed-Function Counters	ATTRIBUTES	PERFMON	As Configured (if Native)	
EDX	13	13	1	Reserved_13	ATTRIBUTES	PERFMON	As Configured (if Native)	

CPUID Field					Configuration by TDH.MNG.INIT		Virtualization	
Reg.	MSB	LSB	Field Size	Field Name	TD_PARAMS Section	Configuration Details	Virtualization Type	Virtualization Details
EDX	14	14	1	Reserved_14	ATTRIBUTES	PERFMON	As Configured (if Native)	
EDX	15	15	1	AnyThread Deprecation	ATTRIBUTES	PERFMON	As Configured (if Native)	
EDX	16	16	1	TopDown Support	ATTRIBUTES	PERFMON	As Configured (if Native)	
EDX	23	17	7	Reserved_23_17	ATTRIBUTES	PERFMON	As Configured (if Native)	
EDX	31	24	8	Bit Vector Length	ATTRIBUTES	PERFMON	As Configured (if Native)	
<b>Leaf 0xd / Sub-Leaf 0x0</b>								
EAX	0	0	1	X87	N/A		Fixed	0x1
EAX	1	1	1	SSE	N/A		Fixed	0x1
EAX	2	2	1	AVX256	XFAM	XFAM[2]	As Configured (if Native)	
EAX	3	3	1	PL_BNDREGS	N/A		Fixed	0x0
EAX	4	4	1	PL_BNDCFS	N/A		Fixed	0x0
EAX	5	5	1	KMASK	XFAM	XFAM[7:5]	As Configured (if Native)	
EAX	6	6	1	AVX3 ZMM 15:0	XFAM	XFAM[7:5]	As Configured (if Native)	
EAX	7	7	1	AVX3 ZMM 31:18	XFAM	XFAM[7:5]	As Configured (if Native)	
EAX	8	8	1	Reserved_8	N/A		Fixed	0x0
EAX	9	9	1	PKRU	XFAM	XFAM[9]	As Configured (if Native)	
EAX	16	10	7	Reserved_16_10	N/A		Fixed	0x0
EAX	17	17	1	AMX - XTILECFG	XFAM	XFAM[18:17]	As Configured (if Native)	
EAX	18	18	1	AMX - XTILEDATA	XFAM	XFAM[18:17]	As Configured (if Native)	
EAX	31	19	13	Reserved_31_19	N/A		Fixed	0x0
EBX	31	0	32	Max Bytes for Enabled Features	N/A		Calculated	Native
ECX	31	0	32	Max Bytes for Supported Features	XFAM		As Configured	
EDX	31	0	32	Reserved	N/A		Fixed	0x0
<b>Leaf 0xd / Sub-Leaf 0x1</b>								
EAX	0	0	1	Supports XSAVEOPT	N/A		Fixed	0x1
EAX	1	1	1	Supports XSAVEC and compacted XRSTOR	N/A		Fixed	0x1
EAX	2	2	1	Supports XGETBV with ECX = 1	N/A		Native	
EAX	3	3	1	Supports XSAVES/XRSTORS and IA32_XSS	N/A		Fixed	0x1
EAX	4	4	1	XFD support	XFAM		As Configured	
EAX	31	5	27	Reserved	N/A		Fixed	0x0
EBX	31	0	32	Max Bytes for Enabled Features	N/A		Calculated	Native
ECX	7	0	8	reserved_7_0	N/A		Fixed	0x0
ECX	8	8	1	XSS_RTIT	XFAM	XFAM[8]	As Configured (if Native)	
ECX	9	9	1	reserved_9	N/A		Fixed	0x0
ECX	10	10	1	PASID	N/A		Fixed	0x0
ECX	11	11	1	U_CET	XFAM	XFAM[12:11]	As Configured (if Native)	
ECX	12	12	1	S_CET	XFAM	XFAM[12:11]	As Configured (if Native)	
ECX	13	13	1	HDC	N/A		Fixed	0x0
ECX	14	14	1	ULI/UNIT	XFAM	XFAM[14]	As Configured (if Native)	
ECX	15	15	1	XSS_ARCH_LBRS	XFAM	XFAM[15]	As Configured (if Native)	
ECX	16	16	1	HWP Request	N/A		Fixed	0x0
ECX	31	17	15	Reserved_31_17	N/A		Fixed	0x0
EDX	31	0	32	Reserved	N/A		Fixed	0x0
<b>Leaf 0xd / Sub-Leaves 0x2-0x12</b>								
EAX	31	0	32	Size	XFAM	XFAM[n]	As Configured (if Native)	
EBX	31	0	32	Offset	XFAM	XFAM[n]	As Configured (if Native)	
ECX	0	0	1	IA32_XSS	XFAM	XFAM[n]	As Configured (if Native)	
ECX	1	1	1	0	XFAM	XFAM[n]	As Configured (if Native)	
ECX	31	2	30	0	XFAM	XFAM[n]	As Configured (if Native)	
EDX	31	0	32	Reserved	XFAM	XFAM[n]	As Configured (if Native)	
<b>Leaf 0xe</b>								
EAX	31	0	32	Reserved	N/A		Fixed	0x0
EBX	31	0	32	Reserved	N/A		Fixed	0x0
ECX	31	0	32	Reserved	N/A		Fixed	0x0
EDX	31	0	32	Reserved	N/A		Fixed	0x0
<b>Leaf 0x11</b>								
EAX	31	0	32	Reserved	N/A		Fixed	0x0
EBX	31	0	32	Reserved	N/A		Fixed	0x0
ECX	31	0	32	Reserved	N/A		Fixed	0x0
EDX	31	0	32	Reserved	N/A		Fixed	0x0
<b>Leaf 0x12</b>								
EAX	31	0	32	Reserved	N/A		Fixed	0x0
EBX	31	0	32	Reserved	N/A		Fixed	0x0
ECX	31	0	32	Reserved	N/A		Fixed	0x0
EDX	31	0	32	Reserved	N/A		Fixed	0x0
<b>Leaf 0x13</b>								
EAX	31	0	32	Reserved	N/A		Fixed	0x0
EBX	31	0	32	Reserved	N/A		Fixed	0x0

CPUID Field					Configuration by TDH.MNG.INIT		Virtualization	
Reg.	MSB	LSB	Field Size	Field Name	TD_PARAMS Section	Configuration Details	Virtualization Type	Virtualization Details
ECX	31	0	32	Reserved	N/A		Fixed	0x0
EDX	31	0	32	Reserved	N/A		Fixed	0x0
<b>Leaf 0x14 / Sub-Leaf 0x0</b>								
EAX	31	0	32	Max Valid Subleaf	XFAM	XFAM[8]	As Configured (if Native)	
EBX	0	0	1	CR3 Filtering	XFAM	XFAM[8]	As Configured (if Native)	
EBX	1	1	1	Cycle Accurate Mode	XFAM	XFAM[8]	As Configured (if Native)	
EBX	2	2	1	IP Filtering	XFAM	XFAM[8]	As Configured (if Native)	
EBX	3	3	1	MSRs Preserved Across Warm Reset	XFAM	XFAM[8]	As Configured (if Native)	
EBX	4	4	1	PTWRITE Support	XFAM	XFAM[8]	As Configured (if Native)	
EBX	5	5	1	Power Event Trace Support	XFAM	XFAM[8]	As Configured (if Native)	
EBX	6	6	1	PSB/PMI Injection Support	XFAM	XFAM[8]	As Configured (if Native)	
EBX	7	7	1	PT Event Trace Support	XFAM	XFAM[8]	As Configured (if Native)	
EBX	31	8	24	Reserved	XFAM	XFAM[8]	As Configured (if Native)	
ECX	0	0	1	ToPA Output Supported	XFAM	XFAM[8]	As Configured (if Native)	
ECX	1	1	1	ToPA Tables Support Multiple Regions	XFAM	XFAM[8]	As Configured (if Native)	
ECX	2	2	1	Single-Range Output Supported	XFAM	XFAM[8]	As Configured (if Native)	
ECX	30	3	28	Reserved	XFAM	XFAM[8]	As Configured (if Native)	
ECX	31	31	1	IP Payload Contains LIP	XFAM	XFAM[8]	As Configured (if Native)	
EDX	31	0	32	Reserved	XFAM	XFAM[8]	As Configured (if Native)	
<b>Leaf 0x14 / Sub-Leaf 0x1</b>								
EAX	1	0	2	MTC Period Options	XFAM	XFAM[8]	As Configured (if Native)	
EAX	15	2	14	Reserved	XFAM	XFAM[8]	As Configured (if Native)	
EAX	31	16	16	Number of Address Ranges Supported	XFAM	XFAM[8]	As Configured (if Native)	
EBX	15	0	16	Cycle Thresholds	XFAM	XFAM[8]	As Configured (if Native)	
EBX	31	16	16	PSB Frequencies	XFAM	XFAM[8]	As Configured (if Native)	
ECX	31	0	32	Reserved	XFAM	XFAM[8]	As Configured (if Native)	
EDX	31	0	32	Reserved	XFAM	XFAM[8]	As Configured (if Native)	
<b>Leaf 0x15</b>								
EAX	31	0	32	Denominator	N/A		Fixed	0x1
EBX	31	0	32	Numerator	Other	TSC_FREQUENCY	As Configured	
ECX	31	0	32	Nominal ART Frequency	N/A		Fixed	0x017D7840
EDX	31	0	32	Reserved	N/A		Fixed	0x0
<b>Leaf 0x19</b>								
EAX	0	0	1	CPL0 Restriction	ATTRIBUTES	KL	As Configured (if Native)	
EAX	1	1	1	Decrypt only Restriction	ATTRIBUTES	KL	As Configured (if Native)	
EAX	2	2	1	Encrypt only Restriction	ATTRIBUTES	KL	As Configured (if Native)	
EAX	3	3	1	Process Restriction	ATTRIBUTES	KL	As Configured (if Native)	
EAX	31	4	28	Reserved_31_4	ATTRIBUTES	KL	As Configured (if Native)	
EBX	0	0	1	AES KL Enabled	ATTRIBUTES	KL	As Configured (if Native)	
EBX	1	1	1	Reserved	ATTRIBUTES	KL	As Configured (if Native)	
EBX	2	2	1	AES wide KL Support	ATTRIBUTES	KL	As Configured (if Native)	
EBX	3	3	1	Reserved	ATTRIBUTES	KL	As Configured (if Native)	
EBX	4	4	1	IW Key Backup Support	ATTRIBUTES	KL	As Configured (if Native)	
EBX	31	5	27	Reserved	ATTRIBUTES	KL	As Configured (if Native)	
ECX	0	0	1	LOADIWKEY No Backup parameter Support	ATTRIBUTES	KL	As Configured (if Native)	
ECX	1	1	1	Random IWKey Support	N/A		Fixed	0x0
ECX	31	2	30	Reserved	N/A		Fixed	0x0
EDX	31	0	32	Reserved	N/A		Fixed	0x0
<b>Leaf 0x1c</b>								
EAX	7	0	8	Supported LBR depth values	XFAM	XFAM[15]	As Configured (if Native)	
EAX	29	8	22	Reserved_29_8	XFAM	XFAM[15]	As Configured (if Native)	
EAX	30	30	1	Deep C-state May Reset	XFAM	XFAM[15]	As Configured (if Native)	
EAX	31	31	1	IP values contain LIP	XFAM	XFAM[15]	As Configured (if Native)	
EBX	0	0	1	CPL Filtering Supported	XFAM	XFAM[15]	As Configured (if Native)	
EBX	1	1	1	Branch Filtering Supported	XFAM	XFAM[15]	As Configured (if Native)	
EBX	2	2	1	Call-stack Mode Supported	XFAM	XFAM[15]	As Configured (if Native)	
EBX	31	3	29	Reserved_31_3	XFAM	XFAM[15]	As Configured (if Native)	
ECX	0	0	1	Mispredict Bit Supported	XFAM	XFAM[15]	As Configured (if Native)	
ECX	1	1	1	Timed LBRs Supported	XFAM	XFAM[15]	As Configured (if Native)	
ECX	2	2	1	Branch Type Field Supported	XFAM	XFAM[15]	As Configured (if Native)	
ECX	31	3	29	Reserved_31_3	XFAM	XFAM[15]	As Configured (if Native)	
EDX	31	0	32	Reserved	XFAM	XFAM[15]	As Configured (if Native)	
<b>Leaf 0x1d / Sub-Leaf 0x0</b>								
EAX	0	0	1	TILE support	XFAM	XFAM[18:17]	As Configured (if Native)	
EAX	31	1	31	Reserved_31_1	XFAM	XFAM[18:17]	As Configured (if Native)	
EBX	31	0	32	Reserved	XFAM	XFAM[18:17]	As Configured (if Native)	
ECX	31	0	32	Reserved	XFAM	XFAM[18:17]	As Configured (if Native)	
EDX	31	0	32	Reserved	XFAM	XFAM[18:17]	As Configured (if Native)	

CPUID Field				Configuration by TDH.MNG.INIT		Virtualization		
Reg.	MSB	LSB	Field Size	Field Name	TD_PARAMS Section	Configuration Details	Virtualization Type	Virtualization Details
<b>Leaf 0x1d / Sub-Leaf 0x1</b>								
EAX	15	0	16	total_tile_bytes	XFAM	XFAM[18:17]	As Configured (if Native)	
EAX	31	16	16	bytes_per_tile	XFAM	XFAM[18:17]	As Configured (if Native)	
EBX	15	0	16	bytes_per_row	XFAM	XFAM[18:17]	As Configured (if Native)	
EBX	31	16	16	max_names	XFAM	XFAM[18:17]	As Configured (if Native)	
ECX	15	0	16	max_rows	XFAM	XFAM[18:17]	As Configured (if Native)	
ECX	31	16	16	Reserved_31_16	XFAM	XFAM[18:17]	As Configured (if Native)	
EDX	31	0	32	Reserved	XFAM	XFAM[18:17]	As Configured (if Native)	
<b>Leaf 0x1e</b>								
EAX	31	0	32	Reserved	XFAM	XFAM[18:17]	As Configured (if Native)	
EBX	7	0	8	impl.tmul_maxk (rows or cols)	XFAM	XFAM[18:17]	As Configured (if Native)	
EBX	23	8	16	impl.tmul_maxn (column bytes)	XFAM	XFAM[18:17]	As Configured (if Native)	
EBX	31	24	8	Reserved_31_24	XFAM	XFAM[18:17]	As Configured (if Native)	
ECX	31	0	32	Reserved	XFAM	XFAM[18:17]	As Configured (if Native)	
EDX	31	0	32	Reserved	XFAM	XFAM[18:17]	As Configured (if Native)	
<b>Leaf 0x80000000</b>								
EAX	31	0	32	MaxIndex	N/A		Native	
EBX	31	0	32	Reserved	N/A		Fixed	0x0
ECX	31	0	32	Reserved	N/A		Fixed	0x0
EDX	31	0	32	Reserved	N/A		Fixed	0x0
<b>Leaf 0x80000001</b>								
EAX	31	0	32	Reserved	N/A		Fixed	0x0
EBX	31	0	32	Reserved	N/A		Fixed	0x0
ECX	0	0	1	LAHF/SAHF in 64-bit Mode	N/A		Native	
ECX	4	1	4	Reserved_4_1	N/A		Fixed	0x0
ECX	5	5	1	LZCNT	N/A		Native	
ECX	7	6	2	Reserved_7_6	N/A		Fixed	0x0
ECX	8	8	1	PREFETCHW	N/A		Native	
ECX	31	9	23	Reserved_31_9	N/A		Fixed	0x0
EDX	10	0	11	Reserved_10_0	N/A		Fixed	0x0
EDX	11	11	1	SYSCALL/SYSRET in 64-bit Mode	N/A		Native	
EDX	19	12	8	Reserved_19_12	N/A		Fixed	0x0
EDX	20	20	1	Execute Disable Bit	N/A		Fixed	0x1
EDX	25	21	5	Reserved_25_21	N/A		Fixed	0x0
EDX	26	26	1	1GB Pages	N/A		Fixed	0x1
EDX	27	27	1	RDTSCP and IA32_TSC_AUX	N/A		Fixed	0x1
EDX	28	28	1	Reserved_28	N/A		Fixed	0x0
EDX	29	29	1	Intel 64	N/A		Fixed	0x1
EDX	31	30	2	Reserved_31_30	N/A		Fixed	0x0
<b>Leaf 0x80000008</b>								
EAX	7	0	8	Number of Physical Address Bits	N/A		Native	
EAX	15	8	8	Number of Linear Address Bits	N/A		Native	
EAX	31	16	16	Reserved	N/A		Fixed	0x0
EBX	8	0	9	Reserved_8_0	N/A		Fixed	0x0
EBX	9	9	1	WBNOINVD support	N/A		Fixed	0x1
EBX	31	10	22	Reserved_31_10	N/A		Fixed	0x0
ECX	31	0	32	Reserved	N/A		Fixed	0x0
EDX	31	0	32	Reserved	N/A		Fixed	0x0

## 17.ABI Reference: Constants

This chapter describes the constants designed to be used in the Intel TDX module.

### 17.1. Interface Function Completion Status Codes

**Note:** This section provides a high-level overview of function completion status, as defined. Implementation details may differ.

This section defines the function completion status codes. The structure of the status codes is described in 15.3.2. Three tables are provided below: class table, code table and operand ID table.

#### 17.1.1. Function Completion Status Code Classes (Bits 47:40)

Table 17.1: Function Completion Status Code Classes (Bits 47:40) Definition

Class ID	Class Name	Description
0	General	General function completion status
1	Invalid Operand	An invalid operand value has been provided, e.g., HKID is out of range, HPA overlaps SEAMRR, GPA is not private, etc.
2	Resource Busy	Resource is busy, there is a concurrency conflict.
3	Page Metadata	Page metadata (in PAMT) are incorrect, e.g., page type is wrong.
4	Dependent Resources	The state of dependent resources is incorrect, e.g., there are TD pages while trying to reclaim a TDR page.
5	Intel TDX Module State	The Intel TDX module state is incorrect.
6	TD State	The state of the TD is incorrect, e.g., it has not been initialized yet.
7	TD VCPU State	The state of the TD VCPU is incorrect, e.g., it is corrupted.
8	Key Management	The status code is related to key management, e.g., keys are not configured.
9	Platform	The status code is related to platform configuration or state.
10	Physical Memory	The status code is related to physical memory.
11	Guest TD Memory	The status code is related to guest TD memory.

#### 17.1.2. Function Completion Status Codes

Table 17.2: Function Completion Status Codes Definition

Error and Recoverability Flags, Class and Name (Bits 63:32)			Details L2 (Bits 31:0)	Description
Value (Hex)	Status	Name		
0x00000000	Success	TDX_SUCCESS	TDH.VP.ENTER: Exit Reason Other : 0	Function completed successfully.
0x40000001	Non-Recover.	TDX_NON_RECOVERABLE_VCPU	TDH.VP.ENTER: Exit Reason	TD exit due to a non-recoverable VCPU state (e.g., triple fault) – VCPU is disabled
0x40000002	Non-Recover.	TDX_NON_RECOVERABLE_TD	TDH.VP.ENTER: Exit Reason	TD exit due to a non-recoverable TD state (e.g., machine check) – TD is disabled
0x80000003	Recover. Error	TDX_INTERRUPTED_RESUMABLE	0	Function operation has been interrupted by an external event, and it may be resumed from the point it was interrupted by calling it again.
0x80000004	Recover. Error	TDX_INTERRUPTED_RESTARTABLE	0	Function operation has been interrupted by an external event, and it may be restarted (from its beginning) by calling it again.
0xC0000100	Error	TDX_OPERAND_INVALID	Operand ID	Operand is invalid.
0xC0000101	Error	TDX_OPERAND_ADDR_RANGE_ERROR	Operand ID	Operand address is out of range (e.g., not in a TDMR).
0x80000200	Recover. Error	TDX_OPERAND_BUSY	Operand ID	The operand is busy (e.g., it is locked in Exclusive mode).

Error and Recoverability Flags, Class and Name (Bits 63:32)			Details L2 (Bits 31:0)	Description
Value (Hex)	Status	Name		
0x80000201	Recover. Error	TDX_PREVIOUS_TLB_EPOCH_BUSY	0	TDH.MEM.TRACK failed because one or more of the TD's VCPUs are running, and their VCPU epoch is the previous TD epoch.
0x80000202	Recover. Error	TDX_SYS_BUSY	0	Intel TDX module (as a whole) is busy.
0xC0000300	Error	TDX_OPERAND_PAGE_METADATA_INCORRECT	Operand ID	Physical page metadata (in PAMT) are incorrect for the requested operation.
0x00000301	Success	TDX_PAGE_ALREADY_FREE	Operand ID	Physical page is already marked as PT_FREE.
0xC0000400	Error	TDX_TD_ASSOCIATED_PAGES_EXIST	0	Physical pages associated with the TD exist in memory.
0xC0000500	Error	TDX_SYSINIT_NOT_PENDING	0	Attempting TDH.SYS.INIT when not expected.
0xC0000501	Error	TDX_SYSINIT_NOT_DONE	0	Attempting non-TDH.SYS.INIT SEAMCALL leaf before TDH.SYS.INIT was done.
0xC0000502	Error	TDX_SYSINITLP_NOT_DONE	0	Attempting non-TDH.SYS.LP.INIT SEAMCALL leaf before TDH.SYS.LP.INIT was done on this LP.
0xC0000503	Error	TDX_SYSINITLP_DONE	0	Attempting TDH.SYS.LP.INIT when already done on this LP.
0xC0000504	Error	RESERVED		
0xC0000505	Error	TDX_SYS_NOT_READY	0	Attempting to execute a non-initialization SEAMCALL function before initialization sequence completed.
0xC0000506	Error	TDX_SYS_SHUTDOWN	0	Attempting to execute SEAMCALL when the Intel TDX module is being shut down.
0xC0000507	Error	TDX_SYSCONFIG_NOT_DONE	0	Attempting TDH.SYS.KEY.CONFIG before TDH.SYS.CONFIG is done.
0xC0000600	Error	TDX_TD_NOT_INITIALIZED	0	TD has not been initialized (by TDH.MNG.INIT).
0xC0000601	Error	TDX_TD_INITIALIZED	0	TD has been initialized (by TDH.MNG.INIT).
0xC0000602	Error	TDX_TD_NOT_FINALIZED	0	TD measurement has not been finalized (by TDH.MR.FINALIZE).
0xC0000603	Error	TDX_TD_FINALIZED	0	TD measurement has been finalized (by TDH.MR.FINALIZE).
0xC0000604	Error	TDX_TD_FATAL	0	TD is in a FATAL error state.
0xC0000605	Error	TDX_TD_NON_DEBUG	0	TD's ATTRIBUTES.DEBUG bit is 0.
0xC0000610	Error	TDX_TDCX_NUM_INCORRECT	0	The number of TDCX pages is incorrect.
0xC0000700	Error	TDX_VCPU_STATE_INCORRECT	0	The VCPU state is incorrect for the requested operation.
0x80000701	Recover. Error	TDX_VCPU_ASSOCIATED	0	The VCPU is already associated with another LP.
0x80000702	Recover. Error	TDX_VCPU_NOT_ASSOCIATED	0	The VCPU is not associated with the current LP.
0xC0000703	Error	TDX_TDVPX_NUM_INCORRECT	0	The number of TDVPX pages is incorrect.
0xC0000704	Error	TDX_NO_VALID_VE_INFO	0	There is no valid #VE information.
0xC0000705	Error	TDX_MAX_VCPUS_EXCEEDED	0	TD's maximum number of VCPUs has been exceeded.
0xC0000706	Error	TDX_TSC_ROLLBACK	0	Time Stamp Counter value is lower than on last TD exit.
0xC0000720	Error	TDX_FIELD_NOT_WRITABLE	0	Field code and write mask are for a read-only field.
0xC0000721	Error	TDX_FIELD_NOT_READABLE	0	Field code is for an unreadable field.
0xC0000730	Error	TDX_TD_VMCS_FIELD_NOT_INITIALIZED	Bits 31:0: VMCS field code	The TD VMCS field has not been initialized.
0x80000800	Recover. Error	TDX_KEY_GENERATION_FAILED	0	Failed to generate a random key.
0x80000810	Recover. Error	TDX_TD_KEYS_NOT_CONFIGURED	0	TD keys have not been configured on the hardware.
0xC0000811	Error	TDX_KEY_STATE_INCORRECT	0	TDCS.KEY_STATE is incorrect for the required operation.
0x00000815	Success	TDX_KEY_CONFIGURED	0	The key is already configured on the current package.
0x80000817	Recover. Error	TDX_WBCACHE_NOT_COMPLETE	0	Attempting to execute TDH.MNG.KEY.FREEID when TDH.PHYMEM.CACHE.WB has not completed its operation.
0xC0000820	Error	TDX_HKID_NOT_FREE	0	A provided HKID cannot be assigned because it is not free.
0x00000821	Success	TDX_NO_HKID_READY_TO_WBCACHE	0	No private HKID is in the HKID_FLUSHED state, ready for TDH.PHYMEM.CACHE.WB.
0xC0000823	Error	TDX_WBCACHE_RESUME_ERROR	0	Resume of a previously-interrupted function has been aborted due to wrong HKID.
0x80000824	Recover. Error	TDX_FLUSHVP_NOT_DONE	0	TDH.VP.FLUSH was not done on all required VCPUs; some VCPUs are still associated with LPs.
0xC0000825	Error	TDX_NUM_ACTIVATED_HKIDS_NOT_SUPPORTED	Bits 31:0: Maximum supported HKIDs	The number of activated key IDs on the platform is not supported.
0xC0000900	Error	TDX_INCORRECT_CPUID_VALUE	0	A CPUID value is incorrect.
0xC0000901	Error	TDX_BOOT_NT4_SET	0	MSR IA32_MISC_ENABLES bit 22 (Boot NT4) is set.

Error and Recoverability Flags, Class and Name (Bits 63:32)			Details L2 (Bits 31:0)	Description
Value (Hex)	Status	Name		
0xC0000902	Error	TDX_INCONSISTENT_CPUID_FIELD	0	A field returned by CPUID is inconsistent between LPs.
0xC0000903	Error	RESERVED		
0xC0000904	Error	TDX_CPUID_LEAF_1F_FORMAT_UNRECOGNIZED	0	CPUID leaf 1F format is not recognized or sub-leaves are not in order.
0xC0000905	Error	TDX_INVALID_WBINVD_SCOPE	0	WBINVD scope is not supported.
0xC0000906	Error	TDX_INVALID_PKG_ID	Package ID	Package ID is larger than the maximum supported.
0xC0000907	Error	RESERVED		
0xC0000908	Error	TDX_CPUID_LEAF_NOT_SUPPORTED	CPUID leaf	
0xC0000910	Error	TDX_SMRR_NOT_LOCKED	0: SMRR, 1: SMRR2	SMRR* is not locked.
0xC0000911	Error	TDX_INVALID_SMRR_CONFIGURATION	0: SMRR, 1: SMRR2	SMRR* configuration is invalid.
0xC0000912	Error	TDX_SMRR_OVERLAPS_CMR	Bits 7:0: 0: SMRR, 1: SMRR2 Bits 15:8: Overlapping CMR index	SMRR* overlaps a CMR.
0xC0000913	Error	TDX_SMRR_LOCK_NOT_SUPPORTED	0	Platform does not support SMRR locking.
0xC0000914	Error	TDX_SMRR_NOT_SUPPORTED	0	Platform does not support SMRR.
0xC0000920	Error	TDX_INCONSISTENT_MSR	Bits 31:0: MSR index	MSR configuration is inconsistent between LPs.
0xC0000921	Error	TDX_INCORRECT_MSR_VALUE	Bits 31:0: MSR index	MSR value is incorrect.
0xC0000930	Error	TDX_SEAMREPORT_NOT_AVAILABLE	0	SEAMOPS(SEAMREPORT) instruction leaf is not available.
0x80000940	Recover. Error	TDX_PERF_COUNTERS_ARE_PEBBS_ENABLED	0	In System Profiling Mode, some enabled Perfmon counters are also enabled for PEBBS.
0xC0000A00	Error	TDX_INVALID_TDMR	Bits 7:0: TDMR index	TDMR base address is not aligned on 1GB, its HKID bits are not 0, TDMR size is not specified with 1GB granularity or TDMR is outside the platform's maximum PA.
0xC0000A01	Error	TDX_NON_ORDERED_TDMR	Bits 7:0: TDMR index	TDMR is not specified in an ascending, non-overlapping order.
0xC0000A02	Error	TDX_TDMR_OUTSIDE_CMRS	Bits 7:0: TDMR index	TDMR non-reserved parts are not fully contained in CMRs.
0x00000A03	Success	TDX_TDMR_ALREADY_INITIALIZED	0	TDMR is already fully initialized.
0xC0000A10	Error	TDX_INVALID_PAMT	Bits 7:0: TDMR index Bits 15:8: PAMT level (2: 1GB, 1: 2MB, 0: 4KB)	PAMT region base address is not aligned on 4KB, its HKID bits are not 0, PAMT region size is not specified with 4KB granularity, it is not large enough for the TDMR size or PAMT region is outside the platform's maximum PA.
0xC0000A11	Error	TDX_PAMT_OUTSIDE_CMRS	Bits 7:0: TDMR index Bits 15:8: PAMT level (2: 1GB, 1: 2MB, 0: 4KB)	PAMT is not fully contained in CMRs.
0xC0000A12	Error	TDX_PAMT_OVERLAP	Bits 7:0: TDMR index Bits 15:8: PAMT level (2: 1GB, 1: 2MB, 0: 4KB) Bits 23:16: Overlapping TDMR index	PAMT overlaps with TDMR non-reserved parts or with another PAMT.
0xC0000A20	Error	TDX_INVALID_RESERVED_IN_TDMR	Bits 7:0: TDMR index Bits 15:8: Reserved area index	Reserved area in TDMR's base offset is not aligned on 4KB, its size is not specified with 4KB granularity or it is not fully contained within the TDMR.
0xC0000A21	Error	TDX_NON_ORDERED_RESERVED_IN_TDMR	Bits 7:0: TDMR index Bits 15:8: Reserved area index	Reserved area in TDMR is not specified in an ascending, non-overlapping order.
0xC0000B00	Error	TDX_EPT_WALK_FAILED	Operand ID	
0xC0000B01	Error	TDX_EPT_ENTRY_FREE	Operand ID	
0xC0000B02	Error	TDX_EPT_ENTRY_NOT_FREE	Operand ID	
0xC0000B03	Error	TDX_EPT_ENTRY_NOT_PRESENT	Operand ID	
0xC0000B04	Error	TDX_EPT_ENTRY_NOT_LEAF	Operand ID	
0xC0000B05	Error	TDX_EPT_ENTRY_LEAF	Operand ID	
0xC0000B06	Error	TDX_GPA_RANGE_NOT_BLOCKED	Operand ID	
0x00000B07	Success	TDX_GPA_RANGE_ALREADY_BLOCKED	Operand ID	
0xC0000B08	Error	TDX_TLB_TRACKING_NOT_DONE	Operand ID	
0xC0000B09	Error	TDX_EPT_INVALID_PROMOTE_CONDITIONS	Operand ID	
0x00000B0A	Success	TDX_PAGE_ALREADY_ACCEPTED	Operand ID	

### 17.1.3. Function Completion Status Operand IDs

Table 17.3: Function Completion Operand IDs Definition

Operand ID	Explicit/Implicit	Class	Operand	Description
0	Explicit	GPR	RAX	Explicit input operand RAX

Operand ID	Explicit/Implicit	Class	Operand	Description
1	Explicit	GPR	RCX	Explicit input operand RCX
2	Explicit	GPR	RDX	Explicit input operand RDX
3	Explicit	GPR	RBX	Explicit input operand RBX
4	Explicit	GPR	Reserved_RSP	Reserved
5	Explicit	GPR	RBP	Explicit input operand RBP
6	Explicit	GPR	RSI	Explicit input operand RSI
7	Explicit	GPR	RDI	Explicit input operand RDI
8	Explicit	GPR	R8	Explicit input operand R8
9	Explicit	GPR	R9	Explicit input operand R9
10	Explicit	GPR	R10	Explicit input operand R10
11	Explicit	GPR	R11	Explicit input operand R11
12	Explicit	GPR	R12	Explicit input operand R12
13	Explicit	GPR	R13	Explicit input operand R13
14	Explicit	GPR	R14	Explicit input operand R14
15	Explicit	GPR	R15	Explicit input operand R15
63-16	Explicit	Reserved	Reserved	Reserved for additional explicit operands (e.g., XMM).
64	Explicit	Component of explicit input	ATTRIBUTES	TD_PARAMS.ATTRIBUTES
65	Explicit	Component of explicit input	XFAM	TD_PARAMS.XFAM
66	Explicit	Component of explicit input	EXEC_CONTROLS	TD_PARAMS.EXEC_CONTROLS
67	Explicit	Component of explicit input	EPTP_CONTROLS	TD_PARAMS.EPTP_CONTROLS
68	Explicit	Component of explicit input	MAX_VCPUS	TD_PARAMS.MAX_VCPUS
69	Explicit	Component of explicit input	CPUID_CONFIG	TD_PARAMS.CPUID_CONFIG
70	Explicit	Component of explicit input	TSC_FREQUENCY	TD_PARAMS.TSC_FREQUENCY
95-71	Explicit	Component of explicit input	Reserved	Reserved for additional components.
96	Explicit	Component of explicit input	TDMR_INFO_PA	TDMR_INFO_PA array entry
127-97	Explicit	Component of explicit input	Reserved	Reserved for additional components.
128	Implicit	Physical Page	TDR	TDR Page
129	Implicit	Physical Page	TDCX	TDCX Page
130	Implicit	Physical Page	TDVPR	TDVPR Page
131	Implicit	Physical Page	TDVPX	TDVPX Page
143-132	Implicit	Physical Page	Reserved	Reserved for additional implicit physical page types.
144	Implicit	Logical control structure	TDCS	TDCS Logical Structure
145	Implicit	Logical control structure	TDVPS	TDVPS Logical Structure
146	Implicit	Logical control structure	SEPT	Secure EPT Tree
167-147	Implicit	Logical control structure	Reserved	Reserved for additional implicit logical structure types.



Operand ID	Explicit/Implicit	Class	Operand	Description
168	Implicit	Component of logical control structure	RTMR	TDCS.RTMR
169	Implicit	Component of logical control structure	TD_EPOCH	TDCS.TD_EPOCH
183-170	Implicit	Component of logical control structure	Reserved	Reserved for additional components.
184	Implicit	Abstract item	SYS	Intel TDX Module
185	Implicit	Abstract item	TDMR	TDMR
186	Implicit	Abstract item	KOT	KOT
187	Implicit	Abstract item	KET	KET
188	Implicit	Abstract item	WBCACHE	TDH.PHYMEM.CACHE.WB State

## 18.ABI Reference: Data Types

This section describes data types that are designed to be used by the Intel TDX module.

### 18.1. Basic Crypto Types

Table 18.1: Basic Crypto Types

Name	Size (Bytes)	Description
SHA384_HASH	48	384-bit buffer containing the result of a SHA384 hash calculation
KEY128	16	128-bit key
KEY256	32	256-bit key

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### 18.2. TD Parameters Types

**Note:** This section describes TD parameter types, as defined. Implementation details may differ.

#### 18.2.1. ATTRIBUTES

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ATTRIBUTES is defined as a 64b field that specifies various guest TD attributes. ATTRIBUTES is provided by the host VMM as a guest TD initialization parameter as part of TD\_PARAMS. It is reported to the guest TD by TDG.VP.INFO and as part of TDREPORT\_STRUCT returned by TDG.MR.REPORT.

The ATTRIBUTES bits are divided into three groups, as shown in the table below. If any bit in the TUD group is set to 1, the guest TD is under off-TD debug and is untrusted. The SEC group indicates features that may impact TD security but are not considered as impacting TD trust.

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Table 18.2: ATTRIBUTES Definition

Bits	Group	Description	Bits	Field	Description	Reference
7:0	TUD	TD Under Debug If any of the bits in this group are set to 1, the guest TD is untrusted.	0	DEBUG	Guest TD runs in off-TD debug mode. Its VCPU state and private memory are accessible by the host VMM.	13.3
			1	SYSPROF	Indicates system profiling mode where the host VMM can monitor the guest TD using Perfmon counters	13.4
			7:2	RESERVED	Reserved for future TUD flags – must be 0	
31:8	SEC	Attributes that may impact TD security	29:8	RESERVED	Reserved for future SEC flags – must be 0	
			30	PKS	TD is allowed to use Supervisor Protection Keys.	9.13
			31	KL	TD is allowed to use Key Locker. Must be 0	
63:32	OTHER		62:32	RESERVED	Reserved for future OTHER flags – must be 0	

		Attributes that do not impact TD security	63	<b>PERFMON</b>	TD is allowed to use Perfmon and PERF_METRICS capabilities.	13.2
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**Notes:**

- The value of ATTRIBUTES.SYSPROF must be the same as the global SYSPROF value – it is provided as an input to TDH.SYS.CONFIG
- ATTRIBUTES.SYSPROF and ATTRIBUTES.PERFMON may not both be set at the same time.

**18.2.2. XFAM**

Intel SDM, Vol. 1, 13

Managing State Using the XSAVE Feature Set

Intel SDM, Vol. 3, 13

System Programming for Instruction Set Extensions and Processor Extended State

Intel TDX module extended state handling is described in 9.4.

XFAM (eXtended Features Available Mask) is defined as a 64b bitmap, which has the same format as XCR0 or IA32\_XSS MSR. XFAM determines the set of extended features available for use by the guest TD. XFAM is provided by the host VMM as a guest TD initialization parameter as part of TD\_PARAMS. It is reported to the guest TD by CPUID(0x0D, 0x01) and as part of TDREPORT\_STRUCT returned by TDG.MR.REPORT.

The Intel TDX module and the Intel® architecture impose some rules on how the bits of XFAM may be set. See Table 9.3 for details.

**18.2.3. CPUID\_VALUES**

CPUID\_VALUES is defined as a 128b structure composed of four 32b fields representing the values returned by CPUID in registers EAX, EBX, ECX and EDX. An array of CPUID\_RET is used during guest TD configuration by TDH.MNG.INIT.

**Table 18.3: CPUID\_VALUES Definition**

Field	Offset (Bytes)	Size (Bytes)	Description
EAX	0	4	Value returned by CPUID in EAX
EBX	4	4	Value returned by CPUID in EBX
ECX	8	4	Value returned by CPUID in ECX
EDX	12	4	Value returned by CPUID in EDX

**18.2.4. TD\_PARAMS**

TD\_PARAMS is provided as an input to TDH.MNG.INIT, and some of its fields are included in the TD report. The format of this structure is valid for a specific MAJOR\_VERSION of the Intel TDX module, as reported by TDH.SYS.INFO.

TD\_PARAMS' size is 1024B.

**Table 18.4: TD\_PARAMS Definition**

Field	Offset (Bytes)	Type	Size (Bytes)	Description	Included in TDG.MR.REPORT?
ATTRIBUTES	0	64b bitmap (see 18.2.1)	8	TD attributes: the value set in this field must comply with ATTRIBUTES_FIXED0 and ATTRIBUTES_FIXED1 enumerated by TDH.SYS.INFO.	Yes

Field	Offset (Bytes)	Type	Size (Bytes)	Description	Included in TDG.MR.REPORT?
<b>XFAM</b>	8	64b bitmap in XCRO format	8	Extended Features Available Mask: indicates the extended state features allowed for the TD. XFAM's format is the same as XCRO and IA32_XSS MSR. The value set in this field must satisfy the following conditions: <ul style="list-style-type: none"> <li>Natively valid value for XCRO and IA32_XSS (does not contain reserved bits, features not supported by the CPU, or illegal bit combinations)</li> <li>Complies with XFAM_FIXED0 and XFAM_FIXED1 as enumerated by TDH.SYS.INFO.</li> </ul>	Yes
<b>MAX_VCPUS</b>	16	Integer	4	Maximum number of VCPUs	No
<b>RESERVED</b>	20	N/A	4	Must be 0	No
<b>EPTP_CONTROLS</b>	24	EPTP	8	Control bits of EPTP – copied to each TD VMCS on TDH.VP.INIT: <p><b>Bits 2:0</b> Memory type – must be 110 (WB)</p> <p><b>Bits 5:3</b> EPT level – 1 less than the EPT page-walk length</p> <p><b>Bits 63:6</b> Reserved – must be 0</p>	No
<b>EXEC_CONTROLS</b>	32	64b bitmap (see Table 18.5)	8	Non-measured TD-scope execution controls	No
<b>TSC_FREQUENCY</b>	40	16b unsigned integer	2	TD-scope virtual TSC frequency in units of 25MHz – must be between 40 and 400.	No
<b>RESERVED</b>	42	N/A	38	Must be 0	No
<b>MRCONFIGID</b>	80	SHA384_HASH	48	Software-defined ID for non-owner-defined configuration of the guest TD – e.g., run-time or OS configuration	Yes
<b>MROWNER</b>	128	SHA384_HASH	48	Software-defined ID for the guest TD's owner	Yes
<b>MROWNERCONFIG</b>	176	SHA384_HASH	48	Software-defined ID for owner-defined configuration of the guest TD – e.g., specific to the workload rather than the run-time or OS	Yes
<b>RESERVED</b>	224	N/A	32	Must be 0	No
<b>CPUID_CONFIG[0]</b>	256	CPUID_VALUES	16		No

Field	Offset (Bytes)	Type	Size (Bytes)	Description	Included in TDG.MR.REPORT?
				Direct configuration of CPUID leaves/sub-leaves virtualization: the number and order of entries must be equal to the number and order of directly configurable or allowable CPUID leaves/sub-leaves reported by TDH.SYS.INFO. Note that the leaf and sub-leaf numbers are implicit.  Only bits that have been reported as 1 by TDH.SYS.INFO may be set to 1.	
<b>CPUID_CONFIG[n-1]</b>		CPUID_VALUES	16	Note that the virtualization of many CPUID bit fields not enumerated in this list is configurable indirectly, via the XFAM and ATTRIBUTES fields.	
<b>RESERVED</b>		N/A		Fills up to TD_PARAMS size (1024B) – must be 0	No

Table 18.5: TD\_PARAMS\_STRUCT.EXEC\_CONTROLS Definition

Bits	Name	Description
0	<b>GPAW</b>	TD-scope Guest Physical Address Width execution control: copied to each TD VMCS <b>GPAW</b> execution control on TDH.VP.INIT  0: GPA.SHARED bit is GPA[47] 1: GPA.SHARED bit is GPA[51]
63:1	<b>RESERVED</b>	Must be 0

### 18.3. Physical Memory Management Types

- 5 **Note:** This section describes physical memory types, as defined. Implementation may differ. PAMT entry and PT (page type) are defined in 6.3.

#### 18.3.1. Physical Page Size

Three physical page size levels (4KB, 2MB and 1GB) are defined.

Table 18.6: Page Size Definition

Page Size	Associated Physical Page Size	Value
<b>PS_1G</b>	1GB	2
<b>PS_2M</b>	2MB	1
<b>PS_4K</b>	4KB	0

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### 18.4. TD Private Memory Management Data Types: Secure EPT

Intel SDM, Vol. 3, 28.2.2 EPT Translation Mechanism

- Note:** This section describes private memory management types, as defined. Implementation may differ.

### 18.4.1. Secure EPT Entry Overview

From the CPU perspective, the Secure EPT entry format is defined to be identical to the legacy VMX EPT entry format. The text below describes how Secure EPT is used by the Intel TDX module.

The Secure EPT entry state (SEPT\_FREE, SEPT\_PRESENT, SEPT\_BLOCKED, SEPT\_PENDING and SEPT\_PENDING\_BLOCKED), as defined in 7.2, is encoded by bits 2:0 (RWX), bit 9 (used by the Intel TDX module to indicate the entry is blocked) and bit 11 (used by the Intel TDX module to indicate the entry is in a pending state).

**Note:** The Secure EPT entry state encoding is subject to change in future TDX versions; it is described here for the purpose of TD debug only. Software must not rely on this encoding.

In the SEPT\_FREE state, other bits are available for use by the host VMM via the TDH.MEM.SEPT.RD and TDH.MEM.SEPT.WR functions.

### 18.4.2. Secure EPT Levels

Secure EPT level definition is identical to legacy VMX EPT level definition. As a rule, an EPT entry at level L maps a GPA range whose size is  $2^{12+9*L}$ .

**Table 18.7: EPT Levels Definition**

Level	0	1	2	3	4	5 (5-Level EPT Only)
GPA Range Size	4KB	2MB	1GB	512GB	256TB	16PB <sup>9</sup>
Child Physical Page Size	4KB	2MB	1GB	N/A	N/A	N/A
EPT Page Type	N/A	EPT	EPD	EPDPT	EPML4	EPML5
Parent EPT Entry Type	EPTE	EPDE	EPDPTE	EPML4E	EPML5E (5-level EPT) or VMCS.EPTP (4-level EPT)	VMCS.EPTP
GPA Offset Bits	20:12	29:21	38:30	47:39	51:48 (5-level EPT only)	N/A

### 18.4.3. SEPT\_LEAF (Secure EPT Leaf Entry)

**Table 18.8: Secure EPT Leaf Entry Definition**

Bits	VMX Meaning and Usage		Intel TDX Module Usage per Secure EPT Entry State	
	Present	Not-Present	Non-SEPT_FREE	SEPT_FREE
2:0	RWX	000	SEPT_PRESENT: 111 SEPT_PENDING: 000 SEPT_BLOCKED: 000 SEPT_PENDING_BLOCKED: 000	000
5:3	Memory Type	Ignored	Set to 110 (WB)	Host VMM controlled
6	Ignore PAT		Set to 1	
7	Leaf <sup>10</sup>		Set to 1	
8	Accessed		Ignored	
9	Dirty		<b>TDX Blocked (TDB)</b> SEPT_PRESENT: 0 SEPT_PENDING: 0	0

<sup>9</sup> Only the lower half is available as TD private GPA space, because the SHARED bit must be 0

<sup>10</sup> Ignored for EPT entries (that map a 4KB leaf page)

Bits	VMX Meaning and Usage		Intel TDX Module Usage per Secure EPT Entry State	
	Present	Not-Present	Non-SEPT_FREE	SEPT_FREE
			SEPT_BLOCKED: 1 SEPT_PENDING_BLOCKED: 1	
10	Xu	If mode-based execute control is enabled, 0 Otherwise, ignored	Set to 0	Host VMM controlled
11	Ignored	Ignored	<b>TDX Pending (TDP)</b> SEPT_PRESENT: 0 SEPT_PENDING: 1 SEPT_BLOCKED: 0 SEPT_PENDING_BLOCKED: 1	0
51:12	HPA		HPA	Host VMM controlled
56:52	Ignored		Set to 0	
57	Check Paging-writability		Set to 0	
58	Paging-writable		Set to 0	
59	Ignored		Set to 0	
60	Supervisor Shadow Stack		Set to 0	
61	Check Sub-Page Permissions		Set to 0	
62	Ignored		Set to 0	
63	Suppress #VE	Suppress #VE	Set to 1	Set to 1

#### 18.4.4. SEPT\_NON\_LEAF (Secure EPT Non-Leaf Entry)

Table 18.9: Secure EPT Non-Leaf Entry Definition

Bits	VMX Meaning and Usage		Intel TDX Module Usage per Secure EPT Entry State	
	Present	Not-Present	Non-SEPT_FREE	SEPT_FREE
2:0	RWX	000	SEPT_PRESENT: 111 SEPT_BLOCKED: 000	000
6:3	Reserved: must be 0	Ignored	Set to 0000	Host VMM controlled
7	Leaf		Set to 0	
8	Accessed		Ignored	
9	Ignored		<b>TDX Blocked (TDB)</b> SEPT_PRESENT: 0 SEPT_BLOCKED: 1	
10	Xu	If mode-based execute control is enabled, 0 Otherwise, ignored	Set to 0	Host VMM controlled
11	Ignored	Ignored	<b>TDX Pending (TDP)</b> Set to 0	0

Bits	VMX Meaning and Usage		Intel TDX Module Usage per Secure EPT Entry State	
	Present	Not-Present	Non-SEPT_FREE	SEPT_FREE
51:12	HPA		HPA	Host VMM controlled
62:52	Ignored		Set to 0	
63	Ignored	Suppress #VE	Set to 1	1

## 18.5. Measurement and Attestation Types

**Note:** This section describes measurement and attestation types, as defined. Implementation may differ.

### 18.5.1. CPUSVN

5 CPUSVN is a 16B Security Version Number of the CPU.

- There is a single CPUSVN used for SGX and TDX.
- CPUSVN contents are considered micro-architectural. CPUSVN is composed of fields for PR\_RESET\_SVN, R\_LAST\_PATCH\_SVN, SINIT, BIOS ACM, Boot Guard ACM and BIOS Guard NP-PPPE module.

### 18.5.2. TDREPORT\_STRUCT

10 TDREPORT\_STRUCT is the output of the TDG.MR.REPORT function. TDREPORT\_STRUCT is composed of a generic MAC structure (REPORTMACSTRUCT, see 18.5.3 below), a SEAMINFO structure and a TDX-specific TEE info structure (TDINFO\_STRUCT, see 18.5.5 below).

The size of TDREPORT\_STRUCT is 1024B.

**Table 18.10: TDREPORT\_STRUCT Definition**

Name	Offset (Bytes)	Type	Size (Bytes)	Description
REPORTMACSTRUCT	0	REPORTMACSTRUCT	256	REPORTMACSTRUCT for the TDG.MR.REPORT
TEE_TCB_INFO	256	TEE_TCB_INFO_STRUCT	239	Additional attestable elements in the TD's TCB are not reflected in the REPORTMACSTRUCT.CPUSVN – includes the Intel TDX module measurements.
RESERVED	495	N/A	17	Reserved – contains 0
TDINFO	512	TDINFO_STRUCT	512	TD's attestable properties

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### 18.5.3. REPORTMACSTRUCT (Reference)

REPORTMACSTRUCT is common to Intel's Trusted Execution Environments (TEEs) – e.g., SGX and TDX. REPORTMACSTRUCT is the first field in the TEE report structure. In the TDX architecture, that is TDREPORT\_STRUCT. REPORTMACSTRUCT is MAC-protected and contains hashes of the remainder of the report structure which includes the TEE's measurements, and where applicable, the measurements of additional TCB elements not reflected in REPORTMACSTRUCT.CPUSVN – e.g., a SEAM's measurements.

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Software verifying a TEE report structure (for TDX, this includes TEE\_TCB\_INFO\_STRUCT and TDINFO\_STRUCT) should first confirm that its REPORTMACSTRUCT.TEE\_TCB\_INFO\_HASH equals the hash of the TEE\_TCB\_INFO\_STRUCT (if applicable) and that REPORTMACSTRUCT.TEE\_INFO\_HASH equals the hash of the TDINFO\_STRUCT. Then, software uses ENCLU(EVERIFYREPORT) to help check the integrity of the REPORTMACSTRUCT. If all checks pass, the measurements in the structure describe a TEE on this platform.

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The size of REPORTMACSTRUCT is 256B.



Table 18.11: REPORTMACSTRUCT Definition

Name	Offset (Bytes)	Type	Size (Bytes)	Description	MAC
REPORTTYPE	0	REPORTTYPE	4	Type Header Structure	Yes
RESERVED	4		12	Must be zero	Yes
CPUSVN	16	CPUSVN	16	CPU SVN	Yes
TEE_TCB_INFO_HASH	32	SHA384_HASH	48	SHA384 of TEE_TCB_INFO for TEEs implemented using Intel TDX	Yes
TEE_INFO_HASH	80	SHA384_HASH	48	SHA384 of TEE_INFO: a TEE-specific info structure (TDG.VP.INFO or SGXINFO) or 0 if no TEE is represented	Yes
REPORTDATA	128		64	A set of data used for communication between the caller and the target.	Yes
RESERVED	192		32	Must be zero	Yes
MAC	224		32	The MAC over the REPORTMACSTRUCT with model-specific MAC	No

#### 18.5.4. REPORTTYPE (Reference)

REPORTTYPE indicates the reported Trusted Execution Environment (TEE) type, sub-type and version.

- 5 The size of REPORTTYPE is 4B.

Table 18.12: REPORTTYPE Definition

Name	Offset (Bytes)	Size (Bytes)	Description
TYPE	0	1	Trusted Execution Environment (TEE) Type: 0x00: SGX 0x7F-0x01: Reserved (TEE implemented by CPU) 0x80: Reserved (TEE implemented by SEAM module) 0x81: TDX 0xFF-0x82: Reserved (TEE implemented by SEAM module)
SUBTYPE	1	1	TYPE-specific subtype Value is 0
VERSION	2	1	TYPE-specific version. Value is 0
RESERVED	3	1	Must be zero

#### 18.5.5. TDINFO\_STRUCT

TDINFO\_STRUCT is defined as the TDX-specific TEE\_INFO part of TDG.MR.REPORT. It contains the measurements and initial configuration of the TD that was locked at initialization and a set of measurement registers that are run-time extendable. These values are copied from the TDCS by the TDG.MR.REPORT function. Refer to 9.11 for additional details.

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The size of TDINFO\_STRUCT is 512B.

Table 18.13: TDINFO\_STRUCT Definition

Name	Offset (Bytes)	Type	Size (Bytes)	Description
ATTRIBUTES	0		8	TD's ATTRIBUTES
XFAM	8		8	TD's XFAM
MRTD	16	SHA384_HASH	48	Measurement of the initial contents of the TD
MRCONFIGID	64	SHA384_HASH	48	Software-defined ID for non-owner-defined configuration of the guest TD – e.g., run-time or OS configuration
MROWNER	112	SHA384_HASH	48	Software-defined ID for the guest TD's owner
MROWNERCONFIG	160	SHA384_HASH	48	Software-defined ID for owner-defined configuration of the guest TD – e.g., specific to the workload rather than the run-time or OS
RTMR	208	SHA384_HASH	NUM_RTMRs * 48	Array of NUM_RTMRs (4) run-time extendable measurement registers
RESERVED	400	N/A	112	Must be zero

## 18.6. Configuration, Enumeration and Initialization Types

**Note:** This section describes configuration, enumeration and initialization types, as defined. Implementation may differ.

### 18.6.1. CPUID\_CONFIG

CPUID\_CONFIG is designed to enumerate how the host VMM may configure the virtualization done by the Intel TDX module for a single CPUID leaf and sub-leaf. An array of CPUID\_CONFIG entries is used for the Intel TDX module enumeration by TDH.SYS.INFO.

Table 18.14: CPUID\_CONFIG Definition

Field	Offset (Bytes)	Size (Bytes)	Description
LEAF	0	4	EAX input value to CPUID
SUB_LEAF	4	4	ECX input value to CPUID A value of -1 indicates a CPUID leaf with no sub-leaves.
EAX	8	4	Enumeration of the configurable virtualization of the value returned by CPUID in EAX: a value of 1 in any of the bits indicates that the host VMM is allowed to configure that bit
EBX	12	4	Enumeration of the configurable virtualization of the value returned by CPUID in EBX: a value of 1 in any of the bits indicates that the host VMM is allowed to configure that bit
ECX	16	4	Enumeration of the configurable virtualization of the value returned by CPUID in ECX: a value of 1 in any of the bits indicates that the host VMM is allowed to configure that bit

Field	Offset (Bytes)	Size (Bytes)	Description
EDX	20	4	Enumeration of the configurable virtualization of the value returned by CPUID in EDX: a value of 1 in any of the bits indicates that the host VMM is allowed to configure that bit

### 18.6.2. TDSYSINFO\_STRUCT

TDSYSINFO\_STRUCT is designed to provide enumeration information about the Intel TDX module. It is an output of the TDH.SYS.INFO leaf function.

- 5 TDSYSINFO\_STRUCT's size is 1024B.

**Table 18.15: TDSYSINFO\_STRUCT Definition**

Section	Field Name	Offset (Bytes)	Type	Size (Bytes)	Description
Intel TDX Module Info	ATTRIBUTES	0	Bitmap	4	Module attributes <b>Bits 30:0</b> Reserved – set to 0 <b>Bit 31</b> 0 indicates a production module. 1 indicates a debug module.
	VENDOR_ID	4	Integer	4	0x8086 for Intel
	BUILD_DATE	8	BCD	4	Intel TDX module build data – in yyyyymmdd BCD format (each digit occupies 4 bits)
	BUILD_NUM	12	Integer	2	Build number of the Intel TDX module
	MINOR_VERSION	14	Integer	2	Minor version number of the Intel TDX module
	MAJOR_VERSION	16	Integer	2	Major version number of the Intel TDX module
	RESERVED	18	N/A	14	This field is reserved for enumerating future Intel TDX module capabilities. Set to 0
Memory Info	MAX_TDMRS	32	Integer	2	The maximum number of TDMRs supported
	MAX_RESERVED_PER_TDMR	34	Integer	2	The maximum number of reserved areas per TDMR
	PAMT_ENTRY_SIZE	36	Integer	2	The size of a PAMT entry – determines the number of bytes that need to be reserved for the three PAMT areas: <ul style="list-style-type: none"> <li>PAMT_1G (1 entry per 1GB of TDMR)</li> <li>PAMT_2M (1 entry per 2MB of TDMR)</li> <li>PAMT_4K (1 entry per 4KB of TDMR)</li> </ul>
	RESERVED	38	N/A	10	Set to 0
Control Struct Info	TDCS_BASE_SIZE	48	Integer	2	Base value for the number of bytes required to hold TDCS

Section	Field Name	Offset (Bytes)	Type	Size (Bytes)	Description
	RESERVED	50	N/A	2	Reserved for additional TDCS enumeration Set to 0
	TDVPS_BASE_SIZE	52	Integer	2	Base value for the number of bytes required to hold TDVPS
	RESERVED	54	N/A	10	Set to 0
TD Capabilities	ATTRIBUTES_FIXED0	64	Bitmap	8	If any certain bit is 0 in ATTRIBUTES_FIXED0, it must be 0 in any TD's ATTRIBUTES. The value of this field reflects the Intel TDX module capabilities and configuration and CPU capabilities.
	ATTRIBUTES_FIXED1	72	Bitmap	8	If any certain bit is 1 in ATTRIBUTES_FIXED1, it must be 1 in any TD's ATTRIBUTES. The value of this field reflects the Intel TDX module capabilities and configuration and CPU capabilities.
	XFAM_FIXED0	80	Bitmap	8	If any certain bit is 0 in XFAM_FIXED0, it must be 0 in any TD's XFAM.
	XFAM_FIXED1	88	Bitmap	8	If any certain bit is 1 in XFAM_FIXED1, it must be 1 in any TD's XFAM.
	RESERVED	96	N/A	32	Set to 0
	NUM_CPUID_CONFIG	128	Integer	4	Number of the following CPUID_CONFIG entries
	CPUID_CONFIG[0]	132	CPUID_CONFIG	24	Enumeration of the CPUID leaves/sub-leaves that contain bit fields whose virtualization by the Intel TDX module is either: <ul style="list-style-type: none"> <li>Directly configurable (CONFIG_DIRECT) by the host VMM</li> <li>Bits that the host VMM may allow to be 1 (ALLOW_DIRECT) and their native value, as returned by the CPU, is 1.</li> </ul> See 18.6.1 for details. Note that the virtualization of many CPUID bit fields not enumerated in this list is configurable indirectly via the XFAM and ATTRIBUTES assigned to a TD by the host VMM.
	CPUID_CONFIG[last]		CPUID_CONFIG	24	
Reserved	RESERVED		N/A		Fills up to the structure size (1024B) – set to 0

### 18.6.3. CMR\_INFO

CMR\_INFO is designed to provide information about a Convertible Memory Range (CMR), as configured by BIOS and checked and stored securely by MCHECK.

Table 18.16: CMR\_INFO Entry Definition

Name	Offset (Bytes)	Type	Size (Bytes)	Description
CMR_BASE	0	Physical Address	8	Base address of the CMR: since a CMR is aligned on 4KB, bits 11:0 are 0.
CMR_SIZE	8	Integer	8	Size of the CMR, in bytes: since a CMR is aligned on 4KB, bits 11:0 are 0. A value of 0 indicates a null entry.

TDH.SYS.INFO leaf function returns a MAX\_CMRS (32) entry array of CMR\_INFO entries. The CMRs are sorted from the lowest base address to the highest base address, and they are non-overlapping.

#### 5 18.6.4. TDMR\_INFO

TDMR\_INFO is designed to provide information about a single Trust Domain Memory Region (TDMR) and its associated PAMT.

Table 18.17: TDMR\_INFO Entry Definition

Name	Offset (Bytes)	Type	Size (Bytes)	Description
TDMR_BASE	0	Physical Address	8	Base address of the TDMR (HKID bits must be 0): since a TDMR is aligned on 1GB, bits 29:0 are always 0.
TDMR_SIZE	8	Integer	8	Size of the TDMR, in bytes: must be greater than 0 and a whole multiple of 1GB (i.e., bits 29:0 are always 0).
PAMT_1G_BASE	16	Physical Address	8	Base address of the PAMT_1G range associated with the above TDMR (HKID bits must be 0): since a PAMT range is aligned on 4KB, bits 11:0 are always 0.
PAMT_1G_SIZE	24	Integer	8	Size of the PAMT_1G range associated with the above TDMR: since a PAMT range is aligned on 4KB, bits 11:0 are always 0.
PAMT_2M_BASE	32	Physical Address	8	Base address of the PAMT_2M range associated with the above TDMR (HKID bits must be 0): since a PAMT range is aligned on 4KB, bits 11:0 are always 0.
PAMT_2M_SIZE	40	Integer	8	Size of the PAMT_2M range associated with the above TDMR: since a PAMT range is aligned on 4KB, bits 11:0 are always 0.
PAMT_4K_BASE	48	Physical Address	8	Base address of the PAMT_4K range associated with the above TDMR (HKID bits must be 0): since a PAMT range is aligned on 4KB, bits 11:0 are always 0.
PAMT_4K_SIZE	56	Integer	8	Size of the PAMT_4K range associated with the above TDMR: since a PAMT range is aligned on 4KB, bits 11:0 are always 0.
RESERVED_OFFSET[0]	64	Integer	8	<ul style="list-style-type: none"> <li>Offset of reserved range 0 within the TDMR: since a reserved range is aligned on 4KB, bits 11:0 are always 0.</li> </ul>
RESERVED_SIZE[0]	72	Integer	8	Size of reserved range 0 within the TDMR: <ul style="list-style-type: none"> <li>A size of 0 indicates a null entry. All following reserved range entries must also be null.</li> <li>Since a reserved range is aligned on 4KB, bits 11:0 are always 0.</li> </ul>

Name	Offset (Bytes)	Type	Size (Bytes)	Description
RESERVED_OFFSET[N-1]	64 + 16*(N-1)	Integer	8	Offset of the last reserved range within the TDMR.
RESERVED_SIZE[N-1]	72 + 16*(N-1)	Integer	8	Size of the last reserved range within the TDMR.

**Notes:**

- The number of reserved areas within a TDMR is enumerated by TDSYSINFO\_STRUCT.MAX\_RESREVED\_PER\_TDMR (see 18.6.2).
- Within each TDMR entry, all reserved areas must be sorted from the lowest offset to the highest offset, and they must not overlap with each other.
- All TDMRs and PAMTs must be contained within CMRs.
- A PAMT area must not overlap with another PAMT area (associated with any TDMR), and it must not overlap with non-reserved areas of any TDMR. PAMT areas may reside within reserved areas of TDMRs.

**18.7. Control Structure Field Access Code Types**

**Note:** This section describes control structure field access types, as defined. Implementation may differ.

**18.7.1. General Definition**

Field access codes are used with TDH.MNG.RD, TDH.MNG.WR, TDH.VP.RD and TDH.VP.WR functions. They have the following general structure:

**Table 18.18: Control Structure Field Access Codes Definition**

Bits	Name	Description
63	NON_ARCH	A value of 0 indicates that the field code and field definition will be maintained throughout Intel TDX module updates. A value of 1 indicates that the field code and field definition are non-architectural, and their meaning may change with Intel TDX module version. This is normally used for fields accessible only in debug mode.
62:56	CLASS_CODE	Identifies the field class – see the following sections for details
55:32	RESERVED	Must be 0
31:0	FIELD_CODE	Identifies the field – see the following sections for details

The TDH.MNG.RD, TDH.MNG.WR, TDH.VP.RD and TDH.VP.WR functions are designed to read and/or write up to eight bytes at a time. Thus, for those functions, fields that are larger than eight bytes are divided into multiple elements, each with its own field code. For example, SHA384 fields such as MRCONFIGID, whose size is 48B, are divided into six 8B elements, with six sequential field codes.

**18.7.2. TDR and TDCS Field Access Codes****Intel SDM, Vol. 3, 24.6.9 MSR-Bitmap Address**

TD-scope field access codes are used with TDH.MNG.RD and TDH.MNG.WR, as described in 20.2.20 and 20.2.21, respectively.

TD-scope field classes are defined as follows:

**Table 18.19: TD Scope (TDR and TDCS) Field Class Codes Definition**

Class Code	Control Structure	Field Class Name	Field Code Meaning
0	TDR	TD Management	Arbitrary field identifiers
1	TDR	Key Management	Arbitrary field identifiers
16	TDCS	TD Management	Arbitrary field identifiers
17	TDCS	Execution Controls	Arbitrary field identifiers
18	TDCS	TLB Epoch Tracking	Arbitrary field identifiers
19	TDCS	Measurement	Arbitrary field identifiers
32	TDCS	MSR Bitmaps	Offset (in 8B units) from the beginning of the architectural MSR bitmaps page structure, as specified by the [Intel SDM, Vol. 3, 24.6.9]
33	TDCS	Secure EPT Root	Offset (in 8B units) from the beginning of the page

### 18.7.3. TDVPS Field Access Codes

- 5
- Intel SDM, Vol. 1, 13.4 XSAVE Area
  - Intel SDM, Vol. 3, 24.11.2 VMREAD, VMWRITE, and Encodings of VMCS Fields
  - Intel SDM, Vol. 3, 29.1 Virtual APIC State
  - Intel SDM, Vol. 3, App. B Field Encoding in VMCS

TDVPS field access codes are used with TDH.VP.RD and TDH.VP.WR, as described in 20.2.43 and 20.2.44, respectively.

- 10 TDVPS field classes are defined as follows:

**Table 18.20: TD VCPU Scope (TDVPS) Field Class Codes Definition**

Class Code	Field Class Name	Field Code Meaning
0	TD VMCS	Architectural VMCS field code, as specified by [Intel SDM, Vol. 3, 24.11.2 and App. B]. The “HIGH” access type (for accessing the upper 32b of 64b fields) is not supported.
1	VAPIC	Offset (in 8B units) from the beginning of the architectural virtual APIC page structure, as specified by the [Intel SDM, Vol. 3, 29.1]
2	VE_INFO	Arbitrary field identifiers
16	Guest GPR State	Architectural GPR number
17	Other Guest State	Arbitrary field identifiers
18	Guest Extended State	Offset (in 8B units) from the beginning of the architectural XSAVE area structure, as specified by the [Intel SDM, Vol. 1, 13.4] and enumerated by CPUID(0x0A)
19	Guest MSR State	MSR index
32	Management	Arbitrary field identifiers

## 19.ABI Reference: Control Structures

This chapter describes the details of TDX control structures.

### 19.1. TD-Scope Control Structures

TD-scope control structures are described in 5.2.

#### 5 19.1.1. How to Read the TDR and TDCS Tables

The VMM access column describes whether this field is accessible to the host VMM, using TDH.MNG.RD and TDDBGWRV, in production mode (ATTRIBUTES.DEBUG == 0) and debug mode (ATTRIBUTES.DEBUG == 1). Possible values are shown in the table below.

**Table 19.1: VMM Access Definition**

VMM Access	Meaning
None	No host VMM access to the field
RO	Host VMM can only read the field (using TDDGBRD)
RW	Host VMM can read and write the field using TDH.MNG.RD and TDH.MNG.WR.

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#### 19.1.2. TDR

**Note:** This section describes TDR, as defined. Implementation may differ.

TDR is the root control structure of a guest TD. TDR is encrypted using the Intel TDX global private HKID. It contains the minimal set of fields that allow TD management operation when the guest TD's private ephemeral HKID is not known yet or when the TD's key state is such that memory encrypted with the guest TD's private ephemeral key is not accessible.

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TDR occupies a single 4KB naturally aligned page of memory. It is the first TD page to be allocated and the last to be removed.

TRD fields are divided into the following classes:

**Table 19.2: TDR Field Classes Definition**

Field Class	Description
TD Management	These fields are used to manage the TDR page, its descendent TD private memory pages and control structure pages.
Key Management	These fields are used by the Intel TDX module to manage memory encryption keys. See Chapter 4 for details.

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**Note:** The table below lists only TDR fields that may be accessed by the host VMM in either production or debug mode.

**Table 19.3: TDR Definition**

Class	Field	VMM Access		Type	Description	Field Code
		Prod.	Debug			
TD Management	INIT	None	RO	Boolean	Indicates that the TDCS has been initialized by TDH.MNG.INIT	0x8000000000000000
TD Management	FATAL	None	RO	Boolean	Indicates a fatal error – e.g., #MC during TD operation.	0x8000000000000001
TD Management	NUM_TDCX	None	RO	Unsigned Integer	Number of TDCX pages that have been added by TDH.MNG.ADDCX	0x8000000000000002
TD Management	TDCX_PA	None	RO	Array of Physical Address	Physical addresses of the TDCX pages (without HKID bits)	0x8000000000000010



Class	Field	VMM Access		Type	Description	Field Code
		Prod.	Debug			
TD Management	CHLDCNT	None	RO	64b Unsigned Integer	The number of 4KB child pages (including opaque control structure pages) associated with this TDR	0x8000000000000004
Key Management	KEY_STATE	None	RO	KEY_STATE	The key management state of this TD	0x8100000000000000
Key Management	HKID	None	RO	16b Unsigned Integer	Private HKID	0x8100000000000001
Key Management	PKG_CONFIG_BITMAP	None	RO	Bitmap	Bitmap that indicates on which package TDH.MNG.KEY.CONFIG was executed successfully using this private key entry	0x8100000000000002

### 19.1.3. TDCS

**Note:** This section describes TDCS, as defined. Implementation may differ.

TDCS complements TDR as the logical control structure of a guest TD. TDCS is encrypted with the guest TS's ephemeral private key. It controls the guest TD operation and holds the state that is global to all the TD's VCPUs.

TDCS fields are divided into the following classes:

**Table 19.4: TDCS Field Classes Definition**

Field Class	Description
<b>TD Management</b>	These fields are used to manage the TDCS, its descendent TD private memory pages and control structure pages.
<b>TD Execution Control</b>	Control the execution of the guest TD: some TD execution control fields are provided as an input to TDH.MNG.INIT, and some of those are included in the TDG.MR.REPORT.
<b>TLB Epoch Tracking</b>	Track the TLB epoch of the guest TD – see 7.6 for details
<b>Measurement</b>	TD measurement registers and associated fields – see Chapter 10 for details
<b>MSR Bitmaps</b>	MSR bitmaps that control VM exit from the guest TD on RDMSR/WRMSR are common to all TD VCPUs and thus are stored as part of TDCS.
<b>Secure EPT Root Page</b>	The root page (PML5 or PML4) of the secure EPT

**Note:** The table below lists only TDCS fields that may be accessed by the host VMM in either production or debug mode.

**Table 19.5: TDCS Definition**

Class	Field	VMM Access		Type	Description	Field Code
		Prod.	Debug			
TD Management	FINALIZED	None	RO	Boolean	Flags that TD build and measurement has been finalized	0x9000000000000000

Class	Field	VMM Access		Type	Description	Field Code
		Prod.	Debug			
TD Management	NUM_VCPUS	None	RO	32b Unsigned Integer	The number of VCPUs that are either in TDX non-root mode (TDVPS.STATE == VCPU_ACTIVE) or are ready to run (TDVPS.STATE == VCPU_READY): this includes VCPUs that have been successfully initialized (by TDH.VP.INIT) and have not since started teardown (due to a Triple Fault)	0x9000000000000001
TD Management	NUM_ASSOC_VCPUS	None	RO	32b Unsigned Integer	The number of VCPUS associated with LPs – i.e., the LPs might hold TLB translations and/or cached TD VMCS	0x9000000000000002
Execution Controls	ATTRIBUTES	None	RO	ATTRIBUTES	TD attributes	0x1100000000000000
Execution Controls	XFAM	None	RO	XCR0	Extended Features Available Mask: indicates the extended user and system features which are available for the TD.	0x1100000000000001
Execution Controls	MAX_VCPUS	None	RO	32b Unsigned Integer	Maximum number of VCPUs	0x1100000000000002
Execution Controls	GPAW	None	RO	Boolean	This bit has the same meaning as the VMCS GPAW execution control: 0: GPA.SHARED bit is GPA[47] 1: GPA.SHARED bit is GPA[51]	0x1100000000000003
Execution Controls	EPTP	None	RO	EPTP	TD-scope Secure EPT pointer: format is the same as the VMCS EPTP execution control; copied to each TD VMCS EPTP on TDVPINIT	0x1100000000000004
Execution Controls	TSC_OFFSET	None	RO	64b unsigned Integer	TD-scope TSC offset execution control: copied to each TD VMCS TSC-offset execution control on TDH.VP.INIT	0x110000000000000A
Execution Controls	TSC_MULTIPLIER	None	RO	64b Unsigned Integer	TD-scope TSC multiplier execution control: copied to each TD VMCS TSC-multiplier execution control on TDH.VP.INIT	0x110000000000000B
Execution Controls	TSC_FREQUENCY	None	RO	16b Unsigned Integer	Virtual TSC frequency – in units of 25MHz	0x110000000000000C
Execution Controls	CPUID_VALUES	None	RO	CPUID_RET	Values returned by configurable CPUID leaves/sub-leaves	0x1100000000000040
Execution Controls	XBUFF_OFFSETS	None	RO	Unsigned Integer	XSAVE buffer components offsets – calculated by TDH.MNG.INIT based on XFAM	0x1100000000000100
TLB Epoch Tracking	TD_EPOCH	None	RO	64b Integer	The TD epoch counter: incremented by the host VMM using the TDH.MEM.TRACK function	0x9200000000000000

Class	Field	VMM Access		Type	Description	Field Code
		Prod.	Debug			
TLB Epoch Tracking	REFCOUNT	None	RO	16b Unsigned Integer	Each REFCOUNT counts the number of LPs which may have TLB entries created during a specific TD_EPOCH and are currently executing in TDX non-root mode.	0x9200000000000001
Measurement	MRTD	None	RO	SHA384_HASH	Measurement of the initial contents of the TD	0x1300000000000000
Measurement	MRCONFIGID	None	RO	SHA384_HASH	Software-defined ID for non-owner-defined configuration of the guest TD – e.g., run-time or OS configuration	0x1300000000000010
Measurement	MROWNER	None	RO	SHA384_HASH	Software-defined ID for the guest TD's owner	0x1300000000000018
Measurement	MROWNERCONFIG	None	RO	SHA384_HASH	Software-defined ID for owner-defined configuration of the guest TD – e.g., specific to the workload rather than the run-time or OS	0x1300000000000020
Measurement	RTMR	None	RO	Array of SHA384_HASH	Array of NUM_RTMRs run-time extendable measurement registers	0x1300000000000040
Measurement	MRTD_CONTEXT	None	RO	N/A	Non-architectural context used during ongoing calculation of MRTD until TDFINELIZEMR	0x9300000000000080
MSR Bitmaps	MSR_BITMAPS	None	RO	64b bitmap	TD-scope RDMSR/WRMSR exit control bitmaps	0x2000000000000000
Secure EPT Root	SEPT_ROOT	None	RO	Secure EPT Entry	Secure EPT root page (PML5 or PML4)	0x2100000000000000

## 19.2. TDVPS: VCPU-Scope Control Structure

**Note:** This section describes TDVPS, as defined. Implementation may differ.

TDVPS is described in 5.3.1.

### 5 19.2.1. Overview

Logically, in the Intel TDX module's linear address space, TDVPS is a single structure that holds the state and control information for a single TD VCPU. The state is loaded to the LP on TD Entry and saved on TD exits.

Physically, TDVPS is composed of a root page (TDVPR) and multiple extension pages (TDVPX). The pages need not be contiguous in physical memory.

10 TDVPS fields are divided into the following classes:

**Table 19.6: TDVPS Field Classes Definition**

Field Class	Description
<b>VCPU Management</b>	These fields are used to manage the TDVPS and the TD VCPU.
<b>TD VMCS</b>	The TD VCPU's architectural VMCS
<b>VAPIC</b>	The TD VCPU's Virtual APIC page
<b>VE_INFO</b>	Holds Virtualization Exception (#VE) information
<b>Guest GPR State</b>	TD VCPU's general-purpose register state

Field Class	Description
Guest MSR State	TD VCPU's MSR state
Guest Extended State	TD VCPU's extended state

### 19.2.2. How to Read the TDVPS (including TD VMCS) Tables

#### 19.2.2.1. VMM Access using TDH.VP.RD and TDH.VP.WR

Describes whether this field is accessible to the host VMM, using TDH.VP.RD and TDH.VP.WR, in production mode (ATTRIBUTES.DEBUG == 0) and debug mode (ATTRIBUTES.DEBUG == 1). Possible values are shown in the table below.

**Table 19.7: VMM Access Column Definition**

VMM Access	Meaning
None	No host VMM access to the field
RO	Host VMM can only read the field (using TDH.VP.RD)
RW	Host VMM can read and write the field using TDH.VP.RD and TDH.VP.WR. TDH.VP.WR does not impose any limitations except for checking that the value fits in the field size.
RW*	Host VMM can read and write the field using TDH.VP.RD and TDH.VP.WR. Writing is subject to the same limitations as if the field was modified by the guest TD (for guest state fields) and/or other limitation as described per field.

#### 19.2.2.2. Text Highlighting

In the TD VMCS tables, text is highlighted to emphasize how the VMCS field value is determined and whether it can be modified during a TD VCPU life cycle, as shown in the table below.

**Table 19.8: Text Highlighting in the TD VMCS Tables**

Highlighting	Meaning
<b>Black Text</b>	Value is set by the Intel TDX module (based on a <b>constant</b> value) on TD VCPU initialization (TDH.VP.INIT), and it does not change afterwards.
<b>Purple Text</b>	On TD VCPU initialization (TDH.VP.INIT), value is <b>computed</b> by the Intel TDX module (e.g., based on TD parameters), and it does not change afterwards.
<b>Blue Text</b>	Value may be modified <b>by the Intel TDX module</b> during guest TD VCPU life cycle (possibly only in debug mode).
<b>Grey Background</b>	Reserved field: value is determined by the IA32_VMX_* MSRs

### 19.2.3. TDVPS (excluding TD VMCS)

**Note:** The table below lists only TDVPS fields that may be accessed by the host VMM in either production or debug mode.

**Table 19.9: TDVPS Definition**

Class	Field	VMM Access		Type	Description	Field Code
		Prod.	Debug			
Management	STATE	None	RO	VCPU_STATE	The activity state of the VCPU.	0xA000000000000000

Class	Field	VMM Access		Type	Description	Field Code
		Prod.	Debug			
Management	LAUNCHED	None	RO	Boolean	A Boolean flag, indicating whether the TD VCPU has been VMLAUNCH'ed on this LP since it has last been associated with this VCPU. If TRUE, VM entry should use VMRESUME. Else, VM entry should use VMLAUNCH.	0xA000000000000001
Management	VCPU_INDEX	None	RO	32b Unsigned Integer	Sequential index of the VCPU in the parent TD: VCPU_INDEX indicates the order of VCPU initialization (by TDH.VP.INIT) starting from 0, and it is made available to the TD via TDG.VP.INFO. VCPU_INDEX is in the range 0 to (TDCS.MAX_VCPUS - 1), up to 0xFFFFE.	0xA000000000000002
Management	NUM_TDVPX	None	RO	Unsigned Integer	A counter of the number of TDVPX child pages associated with this TDVPR	0xA000000000000003
Management	TDVPS_PAGE_PA	None	RO	Array of PA	An array of TDVPS_PAGES physical address pointers to the TDVPS physical pages <ul style="list-style-type: none"> <li>PA is without HKID bits</li> <li>Page 0 is the PA of the TDVPR page</li> <li>Pages 1,2... are PAs of the TDVPX pages</li> </ul>	0xA000000000000010
Management	ASSOC_HKID	None	RO	Integer	The TD's ephemeral private HKID at the last time this VCPU was associated (either by TDH.VP.ENTER or by other VCPU-specific SEAMCALL flow) with an LP: initialized by TDH.VP.INIT to the current TD ephemeral private HKID	0xA000000000000005
Management	VCPU_EPOCH	None	RO	Integer	The value of TDCS.TD_EPOCH at the time this VCPU entered TDX non-root mode	0xA000000000000006
Management	CPUID_SUPERVISOR_VE	None	RO	Boolean	When set, the Intel TDX module injects #VE on guest TD execution of CPUID in CPL = 0.	0xA000000000000007
Management	CPUID_USER_VE	None	RO	Boolean	When set, the Intel TDX module injects #VE on guest TD execution of CPUID in CPL > 0.	0xA000000000000008
Management	IS_SHARED_EPTP_VALID	None	RO	Boolean	Indicates that Shared EPTP is valid: set on successful TDH.VP.WR to Shared EPTP	0xA000000000000009
Management	LAST_EXIT_TSC	None	RO	Unsigned 64b Integer	Initialized to the value returned by rdtsc on TDH.VP.INIT	0xA00000000000000A

Class	Field	VMM Access		Type	Description	Field Code
		Prod.	Debug			
Management	PEND_NMI	RW	RW	Boolean	When set, the Intel TDX module injects an NMI to the guest TD at the next available opportunity (NMI window open after TDH.VP.ENTER). The Intel TDX module then clears PEND_NIM.	0x200000000000000B
VAPIC	VAPIC	None	RO	Page	Virtual APIC Page	0x0100000000000000
VE_INFO	EXIT_REASON	None	RO			0x0200000000000000
VE_INFO	VALID	None	RO		0xFFFFFFFF: valid 0x00000000: not valid	0x0200000000000001
VE_INFO	EXIT_QUALIFICATION	None	RO			0x0200000000000002
VE_INFO	GLA	None	RO			0x0200000000000003
VE_INFO	GPA	None	RO			0x0200000000000004
VE_INFO	EPTP_INDEX	None	RO			0x0200000000000005
VE_INFO	INSTRUCTION_LENGTH	None	RO			0x8200000000000010
VE_INFO	INSTRUCTION_INFORMATION	None	RO			0x8200000000000011
Guest GPR State	RAX	None	RW			0x1000000000000000
Guest GPR State	RCX	None	RW		Init value is provided as an input to TDH.VP.INIT (same value as R8)	0x1000000000000001
Guest GPR State	RDX	None	RW		Init Value: <ul style="list-style-type: none"> <li>Bits [31:00]: Same as RESET value, matches CPUID.1:EAX. CPU version information includes Family, Model and Stepping</li> <li>Bits [63:32]: Set to 0</li> </ul>	0x1000000000000002
Guest GPR State	RBX	None	RW		Init Value: <ul style="list-style-type: none"> <li>Bits [05:00]: GPAW is the effective GPA width (in bits) for this TD (do not confuse with MAXPA); SHARED bit is at GPA bit GPAW-1; only GPAW values 48 and 52 are possible</li> <li>Bits [63:06]: Reserved for future additional details, set to 0, must be ignored by vBIOS</li> </ul>	0x1000000000000003
Guest GPR State	RBP	None	RW			0x1000000000000005
Guest GPR State	RSI	None	RW		Init Value: <ul style="list-style-type: none"> <li>Bits [31:00]: Virtual CPU index, starting from 0 and allocated sequentially on each successful TDH.VP.INIT</li> <li>Bits [63:32]: Set to 0</li> </ul>	0x1000000000000006
Guest GPR State	RDI	None	RW			0x1000000000000007

Class	Field	VMM Access		Type	Description	Field Code
		Prod.	Debug			
Guest GPR State	R8	None	RW		Init value is provided as an input to TDH.VP.INIT (same value as RCX)	0x1000000000000008
Guest GPR State	R9	None	RW			0x1000000000000009
Guest GPR State	R10	None	RW			0x100000000000000A
Guest GPR State	R11	None	RW			0x100000000000000B
Guest GPR State	R12	None	RW			0x100000000000000C
Guest GPR State	R13	None	RW			0x100000000000000D
Guest GPR State	R14	None	RW			0x100000000000000E
Guest GPR State	R15	None	RW			0x100000000000000F
Guest State	DR0	None	RW			0x1100000000000000
Guest State	DR1	None	RW			0x1100000000000001
Guest State	DR2	None	RW			0x1100000000000002
Guest State	DR3	None	RW			0x1100000000000003
Guest State	DR6	None	RO			0x1100000000000006
Guest State	XCR0	None	RO			0x1100000000000020
Guest State	IWK.ENCKEY	None	RO		Last KeyLocker IWK loaded	0x1100000000000040
Guest State	IWK.INTKEY	None	RO			0x1100000000000044
Guest State	IWK.FLAGS	None	RW			0x1100000000000046
Guest MSR State	IA32_SPEC_CTRL	None	RW			0x1300000000000048
Guest MSR State	IA32_UMWAIT_CONTROL	None	RW			0x13000000000000E1
Guest MSR State	IA32_PERFEVTSELx	None	RW			0x1300000000000186
Guest MSR State	MSR_OFFCORE_RSPx	None	RW			0x13000000000001A6
Guest MSR State	IA32_XFD	None	RO			0x13000000000001C4
Guest MSR State	IA32_XFD_ERR	None	RO			0x13000000000001C5
Guest MSR State	IA32_FIXED_CTRx	None	RW			0x1300000000000309
Guest MSR State	IA32_PERF_METRICS	None	RW			0x1300000000000329
Guest MSR State	IA32_FIXED_CTR_CTRL	None	RW			0x130000000000038D
Guest MSR State	IA32_PERF_GLOBAL_STATUS	None	RO			0x130000000000038E
Guest MSR State	IA32_PEBS_ENABLE	None	RW			0x13000000000003F1
Guest MSR State	MSR_PEBS_DATA_CFG	None	RW			0x13000000000003F2
Guest MSR State	MSR_PEBS_LD_LAT	None	RW			0x13000000000003F6
Guest MSR State	MSR_PEBS_FRONTEND	None	RW			0x13000000000003F7
Guest MSR State	IA32_A_PMCx	None	RW			0x13000000000004C1
Guest MSR State	IA32_DS_AREA	None	RW			0x1300000000000600
Guest MSR State	IA32_XSS	None	RO			0x1300000000000DA0
Guest MSR State	IA32_LBR_DEPTH	None	RW			0x130000000000014CF
Guest MSR State	IA32_STAR	None	RO			0x13000000000002081
Guest MSR State	IA32_LSTAR	None	RO			0x13000000000002082
Guest MSR State	IA32_FMASK	None	RO			0x13000000000002084

Class	Field	VMM Access		Type	Description	Field Code
		Prod.	Debug			
Guest MSR State	IA32_KERNEL_GS_BASE	None	RO			0x1300000000002102
Guest MSR State	IA32_TSC_AUX	None	RW			0x1300000000002103
Guest Ext. State	XBUFF	None	RW	XSAVES buffer		0x1200000000000000

#### 19.2.4. TD VMCS

Intel SDM, 24 Virtual Machine Control Structures

**Note:** This section describes TD VMCS usage, as defined. Implementation may differ.

- 5 TD VMCS is a VMX format VMCS (with TDX ISA extensions) that is stored as part of TDVPS.

##### 19.2.4.1. TD VMCS Guest State Area

###### 19.2.4.1.1. TD VMCS Guest Register State Area

Intel SDM, Vol. 3, 9.1.1 Processor State after Reset  
Intel SDM, Vol. 3, 24.4.1 Guest Register State

10 Table 19.10: TD VMCS Guest Register State Area Fields

Field Name	VMM Access		Context Switched	Initial State	Reference
	Prod.	Debug			
<b>Guest CR0</b>	None	RO	Yes	0x0021 <ul style="list-style-type: none"> <li>Bits PE (0) and NE (5) are set to 1.</li> <li>All other bits are cleared to 0.</li> </ul> The initial value is checked for compatibility with fixed-0 and fixed-1 bits according to IA32_VMX_CR0_FIXED* MSRs.	9.5.1
<b>Guest CR3</b>	None	RO	Yes	0	
<b>Guest CR4</b>	None	RO	Yes	0x2040 <ul style="list-style-type: none"> <li>Bits MCE (6) and VMXE (13) are set to 1.</li> <li>All other bits are cleared to 0.</li> </ul> The initial value is checked for compatibility with fixed-0 and fixed-1 bits according to IA32_VMX_CR4_FIXED* MSRs.	9.5.2
<b>Guest DR7</b>	None	RW	Yes	0x00000400	
<b>Guest RSP</b>	None	RO	Yes	0	
<b>Guest RIP</b>	None	RO	Yes	0xFFFFFFFF0	
<b>Guest RFLAGS</b>	None	RO	Yes	0x00000002	
<b>Guest CS</b>	None	RO	Yes	Selector: 0 Base: 0 Limit: 0xFFFFFFFF AR: 0x0000C09B (Code, RX, Accessed, DPL=0, Present, 32b)	



Field Name	VMM Access		Context Switched	Initial State	Reference
	Prod.	Debug			
Guest DS, ES, FS, GS, SS	None	RO	Yes	Selector: 0 Base: 0 Limit: 0xFFFFFFFF AR: 0x0000C093 (Data, RW, Accessed, DPL=0, Present, 32b, 4KB granularity)	
Guest LDTR	None	RO	Yes	Selector: 0 Base: 0 Limit: 0x0000FFFF AR: 0x00010082 (LDT, Present, 32b, 1B granularity, Unusable)	
Guest TR	None	RO	Yes	Selector: 0 Base: 0 Limit: 0x0000FFFF AR: 0x0000008B (32b TSS, Busy, Present, 32b, 1B granularity)	
Guest GDTR	None	RO	Yes	Base: 0 Limit: 0x0000FFFF	
Guest IDTR	None	RO	Yes	Base: 0 Limit: 0x00000000	
Guest MSRs	See Table 19.11 below				
Guest SMBASE	None	None	Yes	0	

#### 19.2.4.1.2. TD VMCS Guest MSRs

See also the MSR virtualization tables in 16.1.

Table 19.11: TD VMCS Guest MSRs

MSR Name	VMM Access		Description	Initial State	Reference
	Prod.	Debug			
IA32_DEBUGCTL	None	RW*	<ul style="list-style-type: none"> <li>Reserved bits 63:16 and 5:2 must be 0</li> <li>Bit 13 must not be modified</li> </ul>	0	13.1.2.2
IA32_SYSENTER_CS	None	RO		0	
IA32_SYSENTER_ESP	None	RO		0	
IA32_SYSENTER_EIP	None	RO		0	
IA32_PERF_GLOBAL_CTRL	None	RW		0x000000FF <ul style="list-style-type: none"> <li>EN_PMCx (bits 0 to (NUM_PMC - 1)) are set to 1.</li> <li>All other bits are cleared to 0.</li> </ul>	
IA32_PAT	None	RO		0x0007040600070406	[Intel SDM, Vol. 3, Table 11-12]

MSR Name	VMM Access		Description	Initial State	Reference
	Prod.	Debug			
IA32_EFER	None	RO		0x901 <ul style="list-style-type: none"> <li>SCE (bit 0) is set to 1.</li> <li>LME (bit 8) is set to 1.</li> <li>NXE (bit 11) is set to 1.</li> <li>All other bits are cleared to 0.</li> </ul>	
VMX_GUEST_IA32_S_CET	None	RO		0	9.4
VMX_GUEST_SSP	None	RO		0	9.4
VMX_GUEST_IA32_INTERRUPT_SSP_TABLE_ADDR	None	RO		0	9.4
IA32_RTIT_CTL	None	RW		0	
IA32_LBR_CTL	None	RW		0	
IA32_BNDCFGS	None	RO		0	9.4
IA32_GUEST_PKRS	None	RO		0	9.13

#### 19.2.4.1.3. TD VMCS Guest Non-Register State Area

Intel SDM, 24.4.2 Guest Non-Register State

Table 19.12: TD VMCS Guest Non-Register State Area Fields

Field Name	VMM Access		Description	Initial State	Reference
	Prod.	Debug			
Activity State	None	RO	Saved/restored on VM exit/entry	Active (0)	
Interruptibility State	None	RO	Saved/restored on VM exit/entry	0	
Pending Debug Exceptions	None	RW	Saved/restored on VM exit/entry	0	
VMCS Link Pointer	None	None	Saved/restored on VM exit/entry	NULL_PA (-1)	
VMX-Preemption Timer Value	None	RO	N/A: VMX-preemption timer is not used by guest TDs.	0	
PDPTE0 – PDPTE3	None	None	N/A: PAE paging is not used by TD guests.	NULL_PA (-1)	
Guest Interrupt Status	None	RO	Includes RVI (lower byte) and SVI (upper byte): saved/restored on VM exit/entry	0	
PML Index	None	None	N/A: PML is not used by guest TDs.	0	
Guest UINV	None	RO		0	

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#### 19.2.4.2. TD VMCS Host State Area

Intel SDM, 24.5 Host-State Area

The host state area is not intended to be accessible outside the Intel TDX module.

## 19.2.4.3. TD VMCS VM-Execution Control Fields

Intel SDM, 24.6 VM-Execution Control Fields

## 19.2.4.3.1. TD VMCS Pin-Based VM-Execution Controls

Table 19.13: TD VMCS Pin-Based VM-Execution Controls

Bit(s)	Name	VMM Access		Description	Reference
		Prod.	Debug		
0	External-interrupt exiting	None	RO	Set to 1 – the Intel TDX module performs TD Exit	
2:1	Reserved	None	RO	Set based on IA32_VMX_TRUE_PINBASED_CTLMSR	[Intel SDM, Vol. 3, A.3.1]
3	NMI exiting	None	RO	Set to 1 – the Intel TDX module performs TD Exit	
4	Reserved	None	RO	Set based on IA32_VMX_TRUE_PINBASED_CTLMSR	[Intel SDM, Vol. 3, A.3.1]
5	Virtual NMIs	None	RO	Set to 1	9.8.4
6	Activate VMX-preemption timer	None	RO	Set to 0	
7	Process posted interrupts	RW*	RW*	Initial value is 0. Set to 1 by TDH.VP.WR only if a valid posted interrupt descriptor and a valid posted interrupt notification vector are set.	9.8, 19.2.4.3.6
31:8	Reserved	None	RO	Set based on IA32_VMX_TRUE_PINBASED_CTLMSR	[Intel SDM, Vol. 3, A.3.1]

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## 19.2.4.3.2. TD VMCS Processor-Based VM-Execution Controls

Table 19.14: TD VMCS Primary Processor-Based VM-Execution Controls

Bit	Name	VMM Access		Description	Reference
		Prod	Debug		
1:0	Reserved	None	RO	Set based on IA32_VMX_TRUE_PROCBASED_CTLMSR (fixed-0)	[Intel SDM, Vol. 3, A.3.2]
2	Interrupt-window exiting	None	RO	Set to 0	9.12
3	Use TSC offsetting	None	RO	Set to 1	9.12
6:4	Reserved	None	RO	Set based on IA32_VMX_TRUE_PROCBASED_CTLMSR	[Intel SDM, Vol. 3, A.3.2]
7	HLT exiting	None	RO	Set to 1 – the Intel TDX module injects a #VE into the guest TD	9.3
8	Reserved	None	RO	Set based on IA32_VMX_TRUE_PROCBASED_CTLMSR	[Intel SDM, Vol. 3, A.3.2]
9	INVLPG exiting	None	RO	Set to 0	
10	MWAIT exiting	None	RO	Set to 1 – the Intel TDX module injects a #VE into the guest TD	9.3
11	RDPMC exiting	None	RO	Set to ~TDCS.ATTRIBUTES.PERFMON	13.2

12	<b>RDTSK exiting</b>	None	RO	Set to 0	9.12
14:13	<b>Reserved</b>	None	RO	Set based on IA32_VMX_TRUE_PROCBASED_CTLMSR	[Intel SDM, Vol. 3, A.3.2]
15	<b>CR3-load exiting</b>	None	RO	Set to 0	
16	<b>CR3-store exiting</b>	None	RO	Set to 0	
17	<b>Activate tertiary controls</b>	None	RO	Set to 1	
18	<b>Reserved</b>	None	RO	Set based on IA32_VMX_TRUE_PROCBASED_CTLMSR	[Intel SDM, Vol. 3, A.3.2]
19	<b>CR8-load exiting</b>	None	RO	Set to 0	
20	<b>CR8-store exiting</b>	None	RO	Set to 0	
21	<b>Use TPR shadow</b>	None	RO	Set to 1	9.8
22	<b>NMI-window exiting</b>	None	RO	Initialized to 0 Set by the Intel TDX module before entering the guest TD – based on TDVPS.PEND_NMI	9.8.5
23	<b>MOV-DR exiting</b>	None	RO	Set to 0	
24	<b>Unconditional I/O exiting</b>	None	RO	Set to 1	9.3
25	<b>Use I/O bitmaps</b>	None	RO	Set to 0	
26	<b>Reserved</b>	None	RO	Set based on IA32_VMX_TRUE_PROCBASED_CTLMSR	[Intel SDM, Vol. 3, A.3.2]
27	<b>Monitor trap flag</b>	None	RO	Set to 0	
28	<b>Use MSR bitmaps</b>	None	RO	Set to 1	
29	<b>MONITOR exiting</b>	None	RO	Set to 1	9.3
30	<b>PAUSE exiting</b>	None	RO	Set to 0	
31	<b>Activate secondary controls</b>	None	RO	Set to 1	

Table 19.15: TD VMCS Secondary Processor-Based VM-Execution Controls

Bit	Name	VMM Access		Description	Reference
		Prod.	Debug		
0	<b>Virtualize APIC accesses</b>	None	RO	Set to 0	9.8
1	<b>Enable EPT</b>	None	RO	Set to 1	
2	<b>Descriptor-table exiting</b>	None	RO	Set to 0	
3	<b>Enable RDTSK</b>	None	RO	Set to 1	9.12
4	<b>Virtualize x2APIC mode</b>	None	RO	Set to 1	9.8
5	<b>Enable VPID</b>	None	RO	Set to 1	
6	<b>WBINVD exiting</b>	None	RO	Set to 1	9.3
7	<b>Unrestricted guest</b>	None	RO	Set to 1	
8	<b>APIC-register virtualization</b>	None	RO	Set to 1	9.8
9	<b>Virtual-interrupt delivery</b>	None	RO	Set to 1	9.8

10	<b>PAUSE-loop exiting</b>	RO	RW	Initialized to 0	9.15.2
11	<b>RDRAND exiting</b>	None	RO	Set to 0	
12	<b>Enable INVPCID</b>	None	RO	Set to 1	
13	<b>Enable VM functions</b>	None	RO	Set to 1	9.3
14	<b>VMCS shadowing</b>	None	RO	Set to 0	
15	<b>Enable ENCLS exiting</b>	None	RO	Set to 1	9.3
16	<b>RDSEED exiting</b>	None	RO	Set to 0	
17	<b>Enable PML</b>	None	RO	Set to 0	
18	<b>EPT-violation #VE</b>	None	RO	Set to 1	9.9
19	<b>Conceal VMX from PT</b>	None	RO	Set to 1	13.1.3
20	<b>Enable XSAVES/XRSTORS</b>	None	RO	Set to 1	
21	<b>PASID translation</b>	None	RO	Set to 1	
22	<b>Mode-based execute control for EPT</b>	None	RO	Set to 0	
23	<b>Enable SPP</b>	None	RO	Set to 0	
24	<b>PT uses guest physical addresses (PT2GPA)</b>	None	RO	Set to 1	13.1.3
25	<b>Use TSC scaling</b>	None	RO	Set to 1	9.12
26	<b>Enable user-level wait and pause</b>	None	RO	Set to the value of virtualized CPUID(0x7,0x0).ECX[5] on TDH.VP.INIT	
27	<b>Enable PCONFIG</b>	None	RO	Set to the value of virtualized CPUID(0x7,0x0).EDX[18] on TDH.VP.INIT	9.3, 9.14
28	<b>Enable ENCLV exiting</b>	None	RO	Set to 1	9.3
29	<b>Enable EPC Virtualization Extensions</b>	None	RO	Set to 0	
30	<b>Bus-lock detection</b>	RW	RW	Initialized to 0 If enabled by the host VMM (using TDH.VP.WR), then the Intel TDX module performs TD Exit on VM exit.	9.11
31	<b>Notification exiting</b>	RW	RW	Initialized to 0 If enabled by the host VMM (using TDH.VP.WR), then the Intel TDX module performs TD Exit on VM exit.	9.11

Table 19.16: TD VMCS Tertiary Processor-Based VM-Execution Controls

Bit	Name	VMM Access		Description	Reference
		Prod.	Debug		
0	<b>LOADIWKEY exiting</b>	None	RO	Set to 0	
1	<b>Enable HLAT</b>	None	RO	Set to 0	
2	<b>EPT paging-write control</b>	None	RO	Set to 0	
3	<b>Guest paging verification</b>	None	RO	Set to 0	

4	<b>IPI virtualization</b>	None	RO	Set to 0	
5	<b>GPAW</b>	None	RO	Copied from TDCS.GPAW on TDH.VP.INIT 0: GPA.SHARED bit is GPA[47] 1: GPA.SHARED bit is GPA[51]	
63:6	<b>Reserved</b>	None	RO	Set based on IA32_VMX_PROCBASED_CTL33 MSR	

### 19.2.4.3.3. TD VMCS Controls for APIC Virtualization

Table 19.17: TD VMCS Controls for APIC Virtualization

Field Name	VMM Access		Description	Reference
	Prod.	Debug		
<b>APIC-access address</b>	None	RO	Set to NULL_PA (-1)	9.8
<b>Virtual-APIC address</b>	None	None	On VCPU-to-LP association, set by the Intel TDX module to the address of the VAPIC page in TDVPS, including the TD's ephemeral HKID	9.8
<b>TPR threshold</b>	None	RO	Set to 0 (do not cause any exits on TPR below threshold)	9.8
<b>EOI-exit bitmap</b>	None	RO	4 fields, all set to 0	9.8
<b>Posted-interrupt notification vector</b>	RW*	RW*	Initialized to 0xFFFF TDH.VP.WR checks the value to be in the range 0 to 255. See process posted interrupt pin-based execution control.	9.8.3, 19.2.4.3.1
<b>Posted-interrupt descriptor address</b>	RW*	RW*	Initialized to NULL_PA (-1) TDH.VP.WR checks the value as follows: <ul style="list-style-type: none"> <li>It must be a valid shared physical address (HKID bits encode a shared HKID).</li> <li>It must be aligned on 64B.</li> </ul> See process posted interrupt pin-based execution control.	9.8.3, 19.2.4.3.1, [Intel SDM, Vol. 3, 24.6.8]

### 5 19.2.4.3.4. EPTP and Shared EPTP

Table 19.18: EPTP (Copied from TDCS.EPTP on TDH.VP.INIT)

Bits	Field Name	VMM Access		Description	Reference
		Prod.	Debug		
2:0	EPT Memory Type	RO	RO	Set to 110 (WB)	
5:3	EPT Level	RO	RO	1 less than the EPT page-walk length – copied on TDH.VP.INIT from TDCS.EPTP	
6	Enable A/D Bits	RO	RO	Set to 0	
7	Enable supervisor shadow stack control	RO	RO	Set to 0	9.4
11:8	Reserved	RO	RO	Set to 0	
51:12	EPML5/4 PA	RO	RO	Copied on TDH.VP.INIT from TDCS.EPTP – HKID bits are cleared to 0	
63:52	Reserved	RO	RO	Set to 0	

Table 19.19: Shared EPTP

Bits	Field Name	VMM Access		Description	Reference
		Prod.	Debug		
11:0	Reserved	RO	RO	Set to 0 For Shared EPT walks, the CPU uses the values of bits [11:0] from the EPTP field above.	
51:12	EPML5/4 PA	RW*	RW*	A guest TD attempt to access a Shared GPA before this field is updated by the host VMM results in an EPT Misconfiguration TD exit. TDH.VP.WR checks that this is a valid shared physical address (HKID bits encode a shared HKID) aligned on 4KB.	
63:52	Reserved	RO	RO	Set to 0	

## 19.2.4.3.5. CR-Related TD VMCS VM-Execution Control Fields

Table 19.20: CR-Related VMCS VM-Execution Control Fields

Field Name	VMM Access		Description	Reference
	Prod.	Debug		
<b>CRO Guest/Host Mask</b>	None	RO	The following bits are set to 1, indicating they are owned by the Intel TDX module: <ul style="list-style-type: none"> <li>PE (0)</li> <li>NE (5)</li> <li>NW (29)</li> <li>CD (30)</li> <li>Any bit set to 1 in IA32_VMX_CRO_FIXED0 (i.e., a bit whose value must be 1)</li> <li>Any bit set to 0 in IA32_VMX_CRO_FIXED1 (i.e., a bit whose value must be 0)</li> <li>Bits known to the Intel TDX module as reserved (bits 63-32, 28-19, 17 and 15-6)</li> </ul> All other bits are cleared to 0, indicating they are owned by the guest TD.	9.5.1
<b>CRO Read Shadow</b>	None	RO	The following bits are set to 1: <ul style="list-style-type: none"> <li>PE (0)</li> <li>NE (5)</li> <li>Any bit set to 1 in IA32_VMX_CRO_FIXED0 (i.e., a bit whose value must be 1)</li> </ul> All other bits are cleared to 0.	9.5.1

Field Name	VMM Access		Description	Reference
	Prod.	Debug		
<b>CR4 Guest/Host Mask</b>	None	RO	<ul style="list-style-type: none"> <li>Bits MCE (6), VMXE (13) and SMXE (14) are set to 1, indicating they are owned by the Intel TDX module.</li> <li>If PK is not enabled, then bit PKE (22) is set to ~TDCS.XFAM[9] to intercept writes to CR4.</li> <li>If TDCS.XFAM[12:11] is 11, then bit CET (23) is cleared to 0. Otherwise, if CET is not enabled, then bit CET (23) is set to 1 to intercept writes to CR4.</li> <li>If ULI is not enabled, then bit UINT (25) is set to ~TDCS.XFAM[14] to intercept writes to CR4.</li> <li>If KeyLocker is not enabled, then bit KL (19) is set to ~TDCS.ATTRIBUTES.KL to intercept writes to CR4.</li> <li>If PKS is not enabled, then bit PKS (24) is set to ~TDCS.ATTRIBUTES.PKS to intercept writes to CR4.</li> <li>If Perfmon is not enabled, then bit PCE (8) is set to ~TDCS.ATTRIBUTES.PERFMON to intercept writes to CR4.</li> <li>Any bit set to 1 in IA32_VMX_CR4_FIXED0 (i.e., a bit whose value must be 1) is set to 1.</li> <li>Any bit set to 0 in IA32_VMX_CR4_FIXED1 (i.e., a bit whose value must be 0) is set to 1.</li> <li>Bits known to the Intel TDX module as reserved (bits 63-26 and bit 15) are set to 1.</li> <li>All other bits are cleared to 0.</li> </ul>	9.5.2, 9.13
<b>CR4 Read Shadow</b>	None	RO	<ul style="list-style-type: none"> <li>Bit MCE (6) is set to 1.</li> <li>Bit VMXE (13) is cleared to 0.</li> <li>Any other bit whose value is set to 1 in IA32_VMX_CR4_FIXED0 (i.e., a bit whose value must be 1) is set to 1.</li> <li>All other bits are cleared to 0.</li> </ul>	9.5.2, 9.13
<b>CR3-Target Values</b>	None	RO	N/A: The Intel TDX module does not control guest CR3	
<b>CR3-Target Count</b>	None	RO	Set to 0: Intel TDX module does not control guest CR3	

#### 19.2.4.3.6. Other TD VMCS VM-Execution Control Fields

Table 19.21: Other TD VMCS VM-Execution Control Fields

Field Name	VMM Access		Description	Reference
	Prod.	Debug		
<b>Exception Bitmap</b>	None	RW*	<ul style="list-style-type: none"> <li>Bit 18 (MCE) is set to 1, even in debug mode.</li> <li>Other bits are cleared to 0. They may be modified in debug mode.</li> </ul>	
<b>Page-fault error-code mask</b>	None	None		
<b>Page-fault error-code match</b>	None	None		
<b>I/O-Bitmap Addresses</b>	None	RO	Set to NULL_PA (-1): I/O bitmaps execution control is set to 0	



Field Name	VMM Access		Description	Reference
	Prod.	Debug		
<b>Time-Stamp Counter Offset</b>	None	RW	Copied from TDCS.TSC_OFFSET on TDH.VP.INIT	9.12
<b>Time-Stamp Counter Multiplier</b>	None	RW	Copied from TDCS.TSC_MULTIPLIER on TDH.VP.INIT	9.12
<b>MSR-Bitmap Address</b>	None	None	A single MSR bitmap page is held per TD as part of TDCS. This field is set to the PA of that MSR bitmap.	
<b>Executive-VMCS Pointer</b>	None	None	N/A	
<b>TD HKID</b>	None	RO		
<b>VPID</b>	None	RO	Set by the Intel TDX module on TDH.VP.INIT to 1 + the sequential index of the VCPU (TDVPS.VCPU_INDEX + 1)	
<b>PLE_GAP</b>	RO	RW	Initial value is 0	9.15.2
<b>PLE_Window</b>	RO	RW	Initial value is 0	9.15.2
<b>VM-Function Controls</b>	None	RO	Set to all 0s – the Intel TDX module injects a #UD into the TD.	9.3
<b>EPTP-list address</b>	None	RO	Set to NULL_PA (-1) – VMFUNC is not supported.	
<b>VMREAD-bitmap address</b>	None	RO	Set to NULL_PA (-1) – VMCS shadowing is not supported.	
<b>VMWRITE-bitmap address</b>	None	RO	Set to NULL_PA (-1) – VMCS shadowing is not supported.	
<b>ENCLS-Exiting Bitmap</b>	None	RO	Set to all 1s – the Intel TDX module injects a #UD into the guest TD.	9.3
<b>ENCLV-Exiting Bitmap</b>	None	RO	Set to all 1s – the Intel TDX module injects a #UD into the guest TD.	9.3
<b>PML address</b>	None	RO	Set to NULL_PA (-1) – PML is not used for TD.	
<b>Virtualization-exception information address</b>	None	None		9.9
<b>EPTP index</b>	None	RO	Set to 0	
<b>XSS-Exiting Bitmap</b>	None	RO	Set to 0	9.4
<b>low PASID directory address</b>	None	None		9.4
<b>high PASID directory address</b>	None	None		9.4
<b>notify window</b>	RW	RW	Initialized to 0	9.11
<b>PCONFIG-Exiting Bitmap</b>	None	RO	Set to all 1s	9.3, 9.14

## 19.2.4.4. TD VMCS VM-Exit Control Fields

Intel SDM, 24.7

VM-Exit Control Fields

Table 19.22: TD VMCS VM-Exit Controls

Bit	Name	VMM Access		Description	Reference
		Prod.	Debug		
1:0	Reserved	None	RO	Set based on IA32_VMX_TRUE_EXIT_CTL5 MSR	[Intel SDM, Vol. 3, A.4]
2	Save debug controls	None	RO	Set to 1	
8:3	Reserved	None	RO	Set based on IA32_VMX_TRUE_EXIT_CTL5 MSR	[Intel SDM, Vol. 3, A.4]
9	Host address-space size	None	RO	Set to 1	
11:10	Reserved	None	RO	Set based on IA32_VMX_TRUE_EXIT_CTL5 MSR	[Intel SDM, Vol. 3, A.4]
12	Load IA32_PERF_GLOBAL_CTRL	None	RO	Set to TDCS.ATTRIBUTES.PERFMON	13.2
14:13	Reserved	None	RO	Set based on IA32_VMX_TRUE_EXIT_CTL5 MSR	[Intel SDM, Vol. 3, A.4]
15	Acknowledge interrupt on exit	None	RO	Set to 1	9.8
17:16	Reserved	None	RO	Set based on IA32_VMX_TRUE_EXIT_CTL5 MSR	[Intel SDM, Vol. 3, A.4]
18	Save IA32_PAT	None	RO	Set to 1	
19	Load IA32_PAT	None	RO	Set to 1	
20	Save IA32_EFER	None	RO	Set to 1	
21	Load IA32_EFER	None	RO	Set to 1	
22	Save VMX-preemption time value	None	RO	Set to 0	
23	Clear IA32_BNDCFGS	None	RO	Set to 1	
24	Conceal VMX from PT	None	RO	Set to 1	13.1.3
25	Clear IA32_RTIT_CTL	None	RO	Set to 1	
26	Clear IA32_LBR_CTL	None	RO	Set to 1	
27	Clear UINV	None	RO	Set to 1	
28	Load host CET state	None	RO	Set to 1	
29	Load host PKRS	None	RO	Set to 0	9.13
30	Save IA32_PERF_GLOBAL_CTRL	None	RO	Set to TDCS.ATTRIBUTES.PERFMON	13.2
31	Reserved	None	RO	Set based on IA32_VMX_TRUE_EXIT_CTL5 MSR	[Intel SDM, Vol. 3, A.4]

Table 19.23: TD VMCS VM-Exit Controls for MSRs

Field Name	VMM Access		Description	Reference
	Prod.	Debug		
VM-exit MSR-store count	None	RO	Not used – set to 0	
VM-exit MSR-store address	None	RO	Not used – set to NULL_PA (-1)	
VM-exit MSR-load count	None	None	Not used – set to 0	
VM-exit MSR-load address	None	None	Not used – set to NULL_PA (-1)	

## 19.2.4.5. TD VMCS VM-Entry Control Fields

Intel SDM, 24.8

VM-Entry Control Fields

5 Table 19.24: TD VMCS VM-Entry Controls

Bit	Name	VMM Access		Description	Reference
		Prod.	Debug		
1:0	Reserved	None	RO	Set based on IA32_VMX_ENTRY_CTL5 MSR	[Intel SDM, Vol. 3, A.5]
2	Load debug controls	None	RO	Set to 1	
8:3	Reserved	None	RO	Set based on IA32_VMX_ENTRY_CTL5 MSR	[Intel SDM, Vol. 3, A.5]
9	IA-32e mode guest	None	RO	Initialized to 0 – written by the CPU on VM exit	[Intel SDM, Vol. 3, 24.8.1]
10	Entry to SMM	None	RO	Set to 0	
11	Deactivate dual-monitor treatment	None	RO	Set to 0	
12	Reserved	None	RO	Set based on IA32_VMX_ENTRY_CTL5 MSR	[Intel SDM, Vol. 3, A.5]
13	Load IA32_PERF_GLOBAL_CTRL	None	RO	Set to TDCS.ATTRIBUTES.PERFMON	13.2
14	Load IA32_PAT	None	RO	Set to 1	
15	Load IA32_EFER	None	RO	Set to 1	
16	Load IA32_BNDCFGS	None	RO	Set to 0	
17	Conceal VMX from PT	None	RO	Set to 1	13.1.3
18	Load IA32_RTIT_CTL	None	RO	Set to 1	?
19	Load UINV	None	RO	Set to 1	?
20	Load CET state	None	RO	Set to 1	9.4
21	Load IA32_LBR_CTL	None	RO	Set to 1	
22	Load guest PKRS	None	RO	Set to TDCS.ATTRIBUTES.PKRS	9.13
31:23	Reserved	None	RO	Set based on IA32_VMX_ENTRY_CTL5 MSR	[Intel SDM, Vol. 3, A.5]

Table 19.25: TD VMCS VM-Entry Controls for MSRs

Field Name	VMM Access		Description	Reference
	Prod.	Debug		
VM-entry MSR-load count	None	RO	Not used – set to 0	
VM-entry MSR-load address	None	RO	Not used – set to NULL_PA (-1)	

Table 19.26: TD VMCS VM-Entry Controls for Event Injection

Field Name	VMM Access		Description	Reference
	Prod.	Debug		
VM-entry interruption information	None	RO		
VM-entry exception error code	None	RO		
VM-entry instruction length	None	RO		

## 5 19.2.4.6. TD VMCS VM-Exit Information Fields

Intel SDM, 24.9

VM-Exit Information Fields

Table 19.27: TD VMCS Basic VM-Exit Information

Field Name	VMM Access		Description	Reference
	Prod.	Debug		
Exit reason	Indirectly via RAX	RO	If the Intel TDX module decides to perform a TD exit, it returns this in RAX bits 31:0. Bit 27 (enclave mode) is not set. Bit 28 (Pending MTF VM exit) is not set. Bit 29 (VM exit from VMX root operation) is not set. Bit 31 (VM-entry failure) is not set.	20.2.31
Exit qualification	Indirectly, via RCX	RO	If the Intel TDX module decides to perform a TD exit, it returns this in RCX. If the exit is due to EPT violation, bits 12-7 of the exit qualification are cleared to 0.	20.2.31
Guest-Linear Address	None	RO		
Guest-physical Address	Indirectly, via R8	RO	If the Intel TDX module decides to perform a TD exit, it returns this in R8. If the EPT fault was caused by an access attempt to a private page, the Intel TDX module clears bits 11:0 to 0.	20.2.31

Table 19.28: TD VMCS Information for VM Exits Due to Vectored Events

Field Name	VMM Access		Description	Reference
	Prod.	Debug		
VM-exit interruption information	Indirectly, via R9	RO	On asynchronous TD exit, the Intel TDX module returns this in R9. Bits 63:32 are cleared to 0.	20.2.31
VM-exit interruption error code	None	RO		

Table 19.29: TD VMCS Information for VM Exits That Occur During Event Delivery

Field Name	VMM Access		Description	Reference
	Prod.	Debug		
IDT-vectoring information	None	RO		
IDT-vectoring error code	None	RO		

5

Table 19.30: TD VMCS Information for VM Exits Due to Instruction Execution

Field Name	VMM Access		Description	Reference
	Prod.	Debug		
VM-exit instruction length	None	RO		
VM-exit instruction information	None	RO		
I/O RCX	None	RO	N/A	
I/O RSI	None	RO	N/A	
I/O RDI	None	RO	N/A	
I/O RIP	None	RO	N/A	

Table 19.31: TD VMCS VM-Instruction Error Field

Field Name	VMM Access		Description	Reference
	Prod.	Debug		
VM-instruction error	None	RO		

## 20.ABI Reference: Interface Functions

### 20.1. How to Read the Interface Function Definitions

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 5 A table of operands is provided for any function that has explicit and/or implicit memory operands or implicit resources. Table 20.1 below describes how to read it. Most of the background is detailed in Chapter 15.

**Table 20.1: How to Read the Operands Information Tables**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Alignment Check	Concurrency Restrictions		
								Resource	Contain. 2MB	Contain. 1GB
The operand may be specified explicitly or may be implicit, see 15.2 0	Register used as a pointer to the operand	HPA or GPA, see 15.2	Resource (memory or CPU internal) for this operand	Data type of the resource, as defined in Chapter 18 or Chapter 19	Type of memory or resource access: R, RW, or Ref,0 see 15.2	Shared, Private, Opaque or Hidden, see 15.2	Required alignment of the operand	<p>Concurrency restrictions are described in 15.1.</p> <p>For explicit memory accesses using HPA, there are additional concurrency restrictions on the 1GB and 2MB blocks that contain the accessed HPA. For other types of accesses, only the operand concurrency is applicable.</p> <p>Shared(i) and Exclusive(i) indicate that the resource is implicitly restricted.</p>		

### 20.2. Host-Side (SEAMCALL) Interface Functions

- 10 The SEAMCALL instruction enters the Intel TDX module. It is designed to call host-side Intel TDX functions, either local or a TD entry to a guest TD, as selected by RAX.

#### 20.2.1. SEAMCALL Instruction (Common)

This section describes the common functionality of SEAMCALL. Leaf functions are described in the following sections.

**Table 20.2: SEAMCALL Input Operands Definition**

Parameter	Description
RAX	Leaf number: see Table 20.4 below.
Other	See individual SEAMCALL leaf functions.

15

**Table 20.3: SEAMCALL Output Operands Definition**

Parameter	Description
RAX	Instruction return code, indicating the outcome of execution of the instruction. See 15.3.2 for details.
Other	See individual SEAMCALL leaf functions.

**Table 20.4: SEAMCALL Instruction Leaf Numbers Definition**

Leaf Number	Interface Function Name
0	TDH.VP.ENTER
1	TDH.MNG.ADDCX
2	TDH.MEM.PAGE.ADD
3	TDH.MEM.SEPT.ADD
4	TDH.VP.ADDCX
5	
6	TDH.MEM.PAGE.AUG
7	TDH.MEM.RANGE.BLOCK
8	TDH.MNG.KEY.CONFIG
9	TDH.MNG.CREATE
10	TDH.VP.CREATE
11	TDH.MNG.RD
12	TDH.PHYMEM.PAGE.RD
13	TDH.MNG.WR
14	TDH.PHYMEM.PAGE.WR
15	TDH.MEM.PAGE.DEMOTE
16	TDH.MR.EXTEND
17	TDH.MR.FINALIZE
18	TDH.VP.FLUSH
19	TDH.MNG.VPFLUSHDONE
20	TDH.MNG.KEY.FREEID
21	TDH.MNG.INIT
22	TDH.VP.INIT
23	TDH.MEM.PAGE.PROMOTE
24	TDH.PHYMEM.PAGE.RDMD
25	TDH.MEM.SEPT.RD
26	TDH.VP.RD
27	TDH.MNG.KEY.RECLAIMID
28	TDH.PHYMEM.PAGE.RECLAIM
29	TDH.MEM.PAGE.REMOVE
30	TDH.MEM.SEPT.REMOVE
31	TDH.SYS.KEY.CONFIG
32	TDH.SYS.INFO
33	TDH.SYS.INIT
35	TDH.SYS.LP.INIT
36	TDH.SYS.TDMR.INIT
38	TDH.MEM.TRACK

Leaf Number	Interface Function Name
39	TDH.MEM.RANGE.UNBLOCK
40	TDH.PHYMEM.CACHE.WB
41	TDH.PHYMEM.PAGE.WBINVD
42	TDH.MEM.SEPT.WR
43	TDH.VP.WR
44	TDH.SYS.LP.SHUTDOWN
45	TDH.SYS.CONFIG

### Instruction Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 5 On entry, the Intel TDX module performs the checks listed below at a high level. Errors cause a SEAMRET with RAX set to the proper completion status code.
1. The leaf number in RAX is supported by the Intel TDX module.
  2. If the Intel TDX module's state is not SYS\_READY (see 12.1.2), only TDH.SYS.INFO, TDH.SYS.INIT, TDH.SYS.LP.INIT, TDH.SYS.CONFIG, TDH.SYS.KEY.CONFIG and TDH.SYS.SHUTDOWN leaf functions are allowed. Those leaf functions then perform other initialization state checks.
- 10

If all checks pass, the Intel TDX module calls the leaf function according to the leaf number in RAX. See the following sections for individual leaf function details.

### Completion Status Codes

**Table 20.5: SEAMCALL Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_SUCCESS	SEAMCALL is successful.
TDX_SYS_SHUTDOWN	
Other	See individual leaf functions.

15



### 20.2.2. TDH.MEM.PAGE.ADD Leaf

Add a 4KB private page to a TD, mapped to the specified GPA, filled with the given page image and encrypted using the TD ephemeral key, and update the TD measurement with the page properties.

**Table 20.6: TDH.MEM.PAGE.ADD Input Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction leaf number – see 20.2.1		
RCX	EPT mapping information:		
	Bits	Name	Description
	2:0	Level	Level of the EPT entry that will map the new page – see 18.4.2: must be 0
	11:3	Reserved	Reserved: must be 0
	51:12	GPA	Bits 51:12 of the guest physical address to be mapped for the new Secure EPT page
63:52	Reserved	Reserved: must be 0	
RDX	Host physical address of the parent TDR page		
R8	Host physical address of the target page to be added to the TD		
R9	Host physical address of the source page image		

5

**Table 20.7: TDH.MEM.PAGE.ADD Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
RCX	Extended error information part 1 In case of EPT walk error, Secure EPT entry where the error was detected In other cases, RCX returns 0
RDX	Extended error information part 2 In case of EPT walk error, EPT level where the error was detected In other cases, RDX returns 0
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

TDH.MEM.PAGE.ADD adds a 4KB private page to a TD and maps it to the provided GPA. It copies the provided source page image to specified physical page using the TD's ephemeral private key and updates the TD measurement with the page properties. TDH.MEM.PAGE.ADD is used during TD build before the TD is initialized.

10

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.8: TDH.MEM.PAGE.ADD Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	GPA	TD private page (GPA) <sup>11</sup>	Blob	RW	Private	4KB	N/A	N/A	N/A
Explicit	RDX	HPA	TDR page	Blob	RW	Opaque	4KB	Exclusive	Shared	Shared
Explicit	R8	HPA	TD private page (HPA) <sup>11</sup>	Blob	RW	Private	4KB	Exclusive	Shared	Shared
Explicit	R9	HPA	Source page	Blob	R	Shared	4KB	None	None	None
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Exclusive(i)	N/A	N/A
Implicit	N/A	GPA	Secure EPT tree	N/A	RW	Private	N/A	Exclusive	N/A	N/A

- 5 TDH.MEM.PAGE.ADD checks the memory operands per the table above when applicable during its flow. The text below does not explicitly mention those checks, except when necessary.

The function checks the following conditions:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
- 10 3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
4. TDCS must have been initialized (TDR.INIT is TRUE).
5. The TD build and measurement must not have been finalized (by TDH.MR.FINALIZE).
6. The target page metadata in PAMT must be correct (PT must be PT\_NDA).

If successful, the function does the following:

- 15 7. Walk the Secure EPT based on the GPA operand, and find the leaf EPT entry for the 4KB page.

If the Secure EPT entry is marked as SEPT\_FREE, the function does the following:

8. Copy the source image to the target TD page using the TD's ephemeral private HKID, and direct write (MOVDIR64B).
9. Update the parent Secure EPT entry with the target page HPA and SEPT\_PRESENT state.
10. Extend TDCS.MRTD with the target page GPA. Extension is done using SHA384 with a 128B extension buffer
- 20 composed as follows:
  - o Bytes 0 through 8 contain the ASCII string "TDH.MEM.PAGE.ADD".
  - o Bytes 16 through 23 contain the GPA (in little-endian format).
  - o All the other bytes contain 0.
11. Increment TDR.CHLCNT.
- 25 12. Update the PAMT entry with the PT\_REG page type and the TDR physical address as the OWNER.

<sup>11</sup> RCX and R8 denote the same TD private page operand, using HPA and GPA respectively

## Completion Status Codes

Table 20.9: TDH.MEM.PAGE.ADD Completion Status Codes (Returned in RAX) Definition

Completion Status Code	Description
TDX_EPT_ENTRY_NOT_FREE	
TDX_EPT_WALK_FAILED	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.MEM.PAGE.ADD is successful
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_FINALIZED	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_INITIALIZED	

### 20.2.3. TDH.MEM.PAGE.AUG Leaf

Dynamically add a 4KB private page to an initialized TD, mapped to the specified GPAs.

**Table 20.10: TDH.MEM.PAGE.AUG Input Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction leaf number – see 20.2.1		
RCX	EPT mapping information:		
	Bits	Name	Description
	2:0	Level	Level of the EPT entry that will map the new page – see 18.4.2: must be 0
	11:3	Reserved	Reserved: must be 0
	51:12	GPA	Bits 51:12 of the guest physical address to be mapped for the new Secure EPT page
63:52	Reserved	Reserved: must be 0	
RDX	Host physical address of the parent TDR page		
R8	Host physical address of the target page to be added to the TD		

5

**Table 20.11: TDH.MEM.PAGE.AUG Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
RCX	Extended error information part 1 In case of EPT walk error, Secure EPT entry where the error was detected In other cases, RCX returns 0.
RDX	Extended error information part 2 In case of EPT walk error, EPT level where the error was detected In other cases, RDX returns 0.
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.MEM.PAGE.AUG adds a 4KB private page to a TD and maps it to the provided GPA. The new page is mapped in a pending state and can be accessed only by the guest TD after it accepts it using TDCALL(TDG.MEM.PAGE.ACCEPT). TDH.MEM.PAGE.AUG does not initialize the new page and does not update the TD measurement. TDH.MEM.PAGE.AUG can be used during TD run time after the TD is initialized.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.12: TDH.MEM.PAGE.AUG Memory Operands Information Definition**

Explicit/ Implicit	Register	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	GPA	TD private page (GPA) <sup>12</sup>	Blob	None	Private	4KB	N/A	N/A	N/A
Explicit	RDX	HPA	TDR page	TDR	RW	Opaque	4KB	Shared	Shared	Shared
Explicit	R8	HPA	TD private page (HPA) <sup>12</sup>	Blob	None	Private	4KB	Exclusive	Shared	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Shared(i)	N/A	N/A
Implicit	N/A	GPA	Secure EPT tree	N/A	RW	Private	N/A	Exclusive	N/A	N/A

- 5 TDH.MEM.PAGE.AUG checks the memory operands per the table above when applicable during its flow. The text below does not explicitly mention those checks, except when necessary.

The function checks the following conditions:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
- 10 3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
4. TDCS must have been initialized (TDR.INIT is TRUE).
5. The TD build and measurement must have been finalized (by TDH.MR.FINALIZE).
6. The target page metadata in PAMT must be correct (PT must be PT\_NDA).

If successful, the function does the following:

- 15 7. Walk the Secure EPT based on the GPA operand, and find the leaf EPT entry for the 4KB page.

If the Secure EPT entry is marked as SEPT\_FREE, the function does the following:

8. Update the parent Secure EPT entry with the target page HPA and SEPT\_PENDING state.
9. Increment TDR.CHLCNT.
10. Update the PAMT entry with the PT\_REG page type and the TDR physical address as the OWNER.

## 20 Completion Status Codes

**Table 20.13: TDH.MEM.PAGE.AUG Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_EPT_ENTRY_NOT_FREE	
TDX_EPT_WALK_FAILED	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	

<sup>12</sup> RCX and R8 denote the same TD private page operand, using HPA and GPA respectively

Completion Status Code	Description
TDX_SUCCESS	TDH.MEM.PAGE.AUG is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_FINALIZED	
TDX_TD_NOT_INITIALIZED	

### 20.2.4. TDH.MEM.PAGE.DEMOTE Leaf

Split a large private TD page (2MB or 1GB) into 512 small pages (4KB or 2MB, respectively).

**Table 20.14: TDH.MEM.PAGE.DEMOTE Input Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction leaf number – see 20.2.1		
RCX	EPT mapping information:		
	Bits	Name	Description
	2:0	Level	Level of the Secure EPT entry that maps the large page to be split: either 1 (2MB) or 2 (1GB) – see 18.4.2
	11:3	Reserved	Reserved: must be 0
	51:12	GPA	Bits 51:12 of the guest physical address of the large page to be split Depending on the level, the following least significant bits must be 0: Level 1 (2MB): Bits 20:12 Level 2 (1GB): Bits 29:12
63:52	Reserved	Reserved: must be 0	
RDX	Host physical address of the parent TDR page		
R8	Host physical address of the new Secure EPT page to be added to the TD		

5

**Table 20.15: TDH.MEM.PAGE.DEMOTE Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
RCX	Extended error information part 1 In case of EPT walk error, Secure EPT entry where the error was detected In other cases, RCX returns 0.
RDX	Extended error information part 2 In case of EPT walk error, EPT level where the error was detected In other cases, RDX returns 0.
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.MEM.PAGE.DEMOTE splits a large TD private page (2MB or 1GB) into 512 small pages (4KB or 2MB, respectively) and adds a new Secure EPT page to map those small pages.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.16: TDH.MEM.PAGE.DEMOTE Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource Name	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	GPA and Level	TD private page to split	Blob	None	Private	$2^{12+9*\text{level}}$ bytes	Exclusive	None	None
Explicit	RDX	HPA	TDR page	TDR	RW	Opaque	4KB	Shared	Shared	Shared
Explicit	R8	HPA	New Secure EPT page	SEPT_PAGE	RW	Private	4KB	Exclusive	Shared	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Shared(i)	N/A	N/A
Implicit	N/A	GPA	Secure EPT Tree	N/A	RW	Private	N/A	Exclusive	N/A	N/A

- 5 TDH.MEM.PAGE.DEMOTE checks the memory operands per the table above when applicable during its flow. The text below does not explicitly mention those checks, except when necessary.

The function checks the following conditions:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
- 10 3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
4. TDCS must have been initialized (TDR.INIT is TRUE).
5. The specified page level is either 1 (2MB) or 2 (1GB). See 18.4.2 for a definition of EPT level.

If successful, the function does the following:

6. Walk the Secure EPT based on the GPA operand and locate the large TD private page to be demoted.
- 15 7. Check the page is blocked (its parent Secure EPT entry is a leaf entry, and its state is SEPT\_BLOCKED).
8. Check that TLB tracking has been done, based on the large TD private page's PAMT.BEPOCH.

If successful, the function does the following:

9. Split the large TD private page PAMT entry into 512 PAMT entries at the lower level:
  - 9.1. Set the parent PAMT\_2M or PAMT\_1G entry state to PT\_NDA.
  - 20 9.2. Set the 512 child PAMT4K or PAMT\_2M entries respectively to PT\_REG.
10. Initialize the new Secure EPT page's 512 entries to SEPT\_PRESENT state pointing to the 512 consecutive small pages above. Use the TD's ephemeral private HKID and direct write (MOVDIR64B).
11. Atomically set the demoted Secure EPT entry to SEPT\_PRESENT leaf entry pointing to the new Secure EPT page.
12. Atomically increment TDR.CHLDCNT by 1.
  - 25 12.1. Note that CHLDCNT counts the number of 4KB pages. The change is due only to the addition of the new Secure EPT page.
13. Update the PAMT entry of the new Secure-EPT page with the PT\_EPT page type and the TDR physical address as the OWNER.



## Completion Status Codes

Table 20.17: TDH.MEM.PAGE.DEMOTE Completion Status Codes (Returned in RAX) Definition

Completion Status Code	Description
TDX_EPT_ENTRY_NOT_LEAF	
TDX_EPT_WALK_FAILED	
TDX_GPA_RANGE_NOT_BLOCKED	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.MEM.PAGE.DEMOTE is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_INITIALIZED	
TDX_TLB_TRACKING_NOT_DONE	

### 20.2.5. TDH.MEM.PAGE.PROMOTE Leaf

Merge 512 consecutive small private TD pages (4KB or 2MB) into one large page (2MB or 1GB, respectively).

**Table 20.18: TDH.MEM.PAGE.PROMOTE Input Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction leaf number – see 20.2.1		
RCX	EPT mapping information:		
	Bits	Name	Description
	2:0	Level	Level of the Secure EPT entry that will map the merged large page: either 1 (2MB) or 2 (1GB) (see 18.4.2)
	11:3	Reserved	Reserved: must be 0
	51:12	GPA	Bits 51:12 of the guest physical address of the merged large page Depending on the level, the following least significant bits must be 0: Level 1 (2MB): Bits 20:12 Level 2 (1GB): Bits 29:12
63:52	Reserved	Reserved: must be 0	
RDX	Host physical address of the parent TDR page		

5

**Table 20.19: TDH.MEM.PAGE.PROMOTE Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
RCX	In case of successful operation, HPA of the removed Secure EPT page In case of EPT walk error, Secure EPT entry where the error was detected In other cases, RCX returns 0.
RDX	In case of EPT walk error, EPT level where the error was detected In other cases, RDX returns 0.
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.MEM.PAGE.PROMOTE merges 512 private pages, which are consecutive both in the HPA space and in the GPA space. It removes the Secure EPT leaf page that formerly mapped those pages.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.20: TDH.MEM.PAGE.PROMOTE Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	GPA and Level	Removed Secure EPT page	SEPT_PAGE	R	Private	$2^{12+9*\text{Level}}$ Bytes	Exclusive	None	None
Explicit	RDX	HPA	TDR page	TDR	RW	Opaque	4KB	Shared	Shared	Shared
Implicit	N/A	HPA	Merged HPA range	Blob	None	Private	N/A	Exclusive	None	None
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Shared(i)	N/A	N/A
Implicit	N/A	GPA	Secure EPT Tree	N/A	RW	Private	N/A	Exclusive	N/A	N/A

- 5 TDH.MEM.PAGE.PROMOTE checks the memory operands per the table above when applicable during its flow. The text below does not explicitly mention those checks, except when necessary.

The function checks the following conditions:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
- 10 3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
4. TDCS must have been initialized (TDR.INIT is TRUE).
5. The specified merged page level is either 1 (2MB) or 2 (1GB) – see 18.4.2 for a definition of EPT level.

If successful, the function does the following:

6. Walk the Secure EPT based on the GPA operand, and locate the Secure EPT parent entry of the GPA range to be promoted to a merged large page.
7. Check the Secure EPT entry:
  - 7.1. It must be a non-leaf entry.
  - 7.2. It must be blocked (SEPT\_BLOCKED).
8. Get the HPA of the Secure EPT page, which currently maps the GPA range to be promoted, from the Secure EPT above. Get its PAMT entry.
- 20 9. Check that TLB tracking has been done, based on the above Secure EPT page's PAMT.BEPOCH.
10. Scan the content of the above Secure EPT page and check all 512 entries:
  - 10.1. They are leaf entries (this also implies that the corresponding pages are PT\_REG).
  - 10.2. Their state is SEPT\_PRESENT.
  - 25 10.3. Have contiguous HPA mapping aligned to the promoted range size.

If successful, the above checks imply that:

- The 2MB or 1GB GPA range to be promoted has a corresponding single HPA range and a single PAMT entry (PAMT\_2M or PAMT\_1G, respectively) owned by the current guest TD, and its current PAMT.PT is PAMT\_NDA.
- The 512 child PAMT entries (PAMT\_2M or PAMT\_4K, respectively) of the above are owned by the current guest TD, and their PAMT.PT is PAMT\_REG.

The function then does the following:

11. Merge the corresponding 512 physical pages into a single larger physical page:
  - 11.1. Set the small page (PAMT\_4K or PAMT\_2M) entries state to PT\_NDA.
  - 11.2. Set the parent (PAMT\_2M or PAMT\_1G respectively) entry to PT\_REG.
- 35 12. Atomically set the promoted Secure EPT entry to SEPT\_PRESENT leaf entry pointing to the merged HPA range.

13. Remove the Secure EPT page that previously mapped the 512 physical pages:

13.1. Atomically decrement TDR.CHLDCNT by 1.

13.1.1. Note that CHLDCNT counts the number of 4KB pages. The change is due only to the removal of the Secure EPT page.

5 13.2. Update the PAMT entry of the removed Secure EPT page to PT\_NDA.

### Completion Status Codes

**Table 20.21: TDH.MEM.PAGE.PROMOTE Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_EPT_ENTRY_FREE	
TDX_EPT_ENTRY_LEAF	
TDX_EPT_INVALID_PROMOTE_CONDITIONS	
TDX_EPT_WALK_FAILED	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.MEM.PAGE.PROMOTE is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_INITIALIZED	
TDX_TLB_TRACKING_NOT_DONE	

## 20.2.6. TDH.MEM.PAGE.REMOVE Leaf

Remove a GPA-mapped 4KB, 2MB or 1GB private page from a TD.

**Table 20.22: TDH.MEM.PAGE.REMOVE Input Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction leaf number – see 20.2.1		
RCX	EPT mapping information:		
	Bits	Name	Description
	2:0	Level	Level of the Secure EPT entry that maps the private page to be removed: either 0 (4KB), 1 (2MB) or 2 (1GB) – see 18.4.2.
	11:3	Reserved	Reserved: must be 0
	51:12	GPA	Bits 51:12 of the guest physical address of the private page to be removed
63:52	Reserved	Reserved: must be 0	
RDX	Host physical address of the parent TDR page		

5

**Table 20.23: TDH.MEM.PAGE.REMOVE Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
RCX	In case of successful operation, HPA of the removed page In case of EPT walk error, Secure EPT entry where the error was detected In other cases, RCX returns 0.
RDX	In case of EPT walk error, EPT level where the error was detected In other cases, RDX returns 0.
Other	Unmodified

### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.MEM.PAGE.REMOVE removes a 4KB, 2MB or 1GB private page from the TD's Secure EPT tree. On successful operation, it marks the physical page as free in PAMT.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.24: TDH.MEM.PAGE.REMOVE Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	GPA and Level	TD private page	Blob	R	Private	$2^{12+9*Level}$ Bytes	Exclusive	None	None

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RDX	HPA	TDR page	TDR	RW	Opaque	4KB	Shared	Shared	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Shared(i)	N/A	N/A
Implicit	N/A	GPA	Secure EPT tree	N/A	RW	Private	N/A	Exclusive	N/A	N/A

TDH.MEM.PAGE.REMOVE checks the memory operands per the table above when applicable during its flow. The text below does not explicitly mention those checks, except when necessary.

The function checks the following conditions:

- 5 1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
4. TDCS must have been initialized (TDR.INIT is TRUE).
5. The TD build and measurement must have been finalized (by TDH.MR.FINALIZE).
- 10 6. The specified level is either 0 (4KB), 1 (2MB) or 2 (1GB) – see 18.4.2 for a definition of EPT level.

If successful, the function does the following:

7. Walk the Secure EPT based on the GPA operand, and find the page to be removed.
8. Check the page's parent Secure EPT entry is a blocked leaf entry (SEPT\_BLOCKED or SEPT\_PENDING\_BLOCKED).
9. Check that TLB tracking was done.
- 15 If successful, the function does the following:
  10. Atomically decrement TDR.CHLD CNT by 1, 512 or 512<sup>2</sup> depending on the removed TD private page size (4KB, 2MB or 1GB, respectively).
  11. Free the physical page:
    - 11.1. If the level is 0 (4KB), set the PAMT entry of the removed TD private page to PT\_NDA.
    - 20 11.2. Else (levels 1 or 2, 2MB or 1GB respectively), set the PAMT entry of the removed TD private page to PT\_NDA.
  12. Set the parent Secure EPT entry to SEPT\_FREE.

### Completion Status Codes

**Table 20.25: TDH.MEM.PAGE.REMOVE Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_EPT_WALK_FAILED	
TDX_GPA_RANGE_NOT_BLOCKED	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.MEM.PAGE.REMOVE is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	

Completion Status Code	Description
TDX_TD_NOT_FINALIZED	
TDX_TD_NOT_INITIALIZED	
TDX_TLB_TRACKING_NOT_DONE	

### 20.2.7. TDH.MEM.RANGE.BLOCK Leaf

Block a TD private GPA range (i.e., a Secure EPT page or a TD private page) at any level (4KB, 2MB, 1GB, 512GB, 256TB, etc.) from creating new GPA-to-HPA address translations.

**Table 20.26: TDH.MEM.RANGE.BLOCK Input Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction leaf number – see 20.2.1		
RCX	EPT mapping information:		
	Bits	Name	Description
	2:0	Level	Level of the Secure EPT entry that maps the GPA range to be blocked – see 18.4.2 Level must be between 0 and 3 for a 4-level EPT or between 0 and 4 for a 5-level EPT.
	11:3	Reserved	Reserved: must be 0
	51:12	GPA	Bits 51:12 of the GPA range to be blocked Depending on the level, the following least significant bits must be 0: Level 0 (EPTE): None Level 1 (EPDE): Bits 20:12 Level 2 (EPDPTE): Bits 29:12 Level 3 (EPML4E): Bits 38:12 Level 4 (EPML5E): Bits 47:12
63:52	Reserved	Reserved: must be 0	
RDX	Host physical address of the parent TDR page		

5

**Table 20.27: TDH.MEM.RANGE.BLOCK Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
RCX	Extended error information part 1 In case of EPT walk error, Secure EPT entry where the error was detected In other cases, RCX returns 0.
RDX	Extended error information part 2 In case of EPT walk error, EPT level where the error was detected In other cases, RDX returns 0.
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

TDH.MEM.RANGE.BLOCK finds the Secure EPT entry for the given GPA and level, and it marks it as blocked (SEPT\_BLOCKED or SEPT\_PENDING\_BLOCKED as appropriate). It records the current TD's TLB epoch in the PAMT entry of the physical Secure EPT page or TD private page mapped by the blocked Secure EPT entry.

10



To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.28: TDH.MEM.RANGE.BLOCK Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	GPA and Level	Secure EPT page or TD private page	Blob	None	Private	$2^{12+9*\text{Level}}$ Bytes	None	None	None
Explicit	RDX	HPA	TDR page	TDR	R	Opaque	4KB	Shared	Shared	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Shared(i)	N/A	N/A
Implicit	N/A	GPA	Secure EPT tree	N/A	RW	Private	N/A	Exclusive	N/A	N/A

- 5 TDH.MEM.RANGE.BLOCK checks the memory operands per the table above when applicable during its flow. The text below does not explicitly mention those checks, except when necessary.

The function checks the following conditions:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
- 10 3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
4. TDCS must have been initialized (TDR.INIT is TRUE).
5. The specified level is of an EPT entry – i.e., 0 to 3 for 4-level EPT or 0 to 4 for 5-level EPT. See 18.4.2 for a definition of EPT level.

If successful, the function does the following:

- 15 6. Walk the Secure EPT based on the GPA operand, and find the Secure EPT entry to be blocked.
7. Check the Secure EPT entry is not free and not blocked (its state should be SEPT\_PRESENT or SEPT\_PENDING).

If successful, the function does the following:

8. Block the Secure EPT entry. Atomically set its state to SEPT\_BLOCKED (if it was SEPT\_PRESENT) or SEPT\_PENDING\_BLOCKED (if it was SEPT\_PENDING).
- 20 9. Read the TD's epoch (TDCS.TD\_EPOCH), and write it to the PAMT entry of the blocked Secure EPT page or TD private page (PAMT.BEPOCH).

### Completion Status Codes

**Table 20.29: TDH.MEM.RANGE.BLOCK Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_EPT_ENTRY_FREE	
TDX_EPT_WALK_FAILED	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	

Completion Status Code	Description
TDX_SUCCESS	TDH.MEM.RANGE.BLOCK is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_INITIALIZED	

### 20.2.8. TDH.MEM.RANGE.UNBLOCK Leaf

Remove the blocking of a TD private GPA range (i.e., a Secure EPT page or a TD private page), at any level (4KB, 2MB, 1GB, 512GB, 256TB etc.) previously blocked by TDH.MEM.RANGE.BLOCK.

**Table 20.30: TDH.MEM.RANGE.UNBLOCK Input Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction leaf number – see 20.2.1		
RCX	EPT mapping information:		
	Bits	Name	Description
	2:0	Level	Level of the Secure EPT entry that maps the GPA range to be unblocked – see 18.4.2 Level must be between 0 and 3 for a 4-level EPT or between 0 and 4 for a 5-level EPT.
	11:3	Reserved	Reserved: must be 0
	51:12	GPA	Bits 51:12 of the guest physical address range to be unblocked Depending on the level, the following least significant bits must be 0: Level 0 (EPTE): None Level 1 (EPDE): Bits 20:12 Level 2 (EPDPTE): Bits 29:12 Level 3 (EPML4E): Bits 38:12 Level 4 (EPML5E): Bits 47:12
63:52	Reserved	Reserved: must be 0	
RDX	Host physical address of the parent TDR page		

5

**Table 20.31: TDH.MEM.RANGE.UNBLOCK Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
RCX	Extended error information part 1 In case of EPT walk error, Secure EPT entry where the error was detected In other cases, RCX returns 0.
RDX	Extended error information part 2 In case of EPT walk error, EPT level where the error was detected In other cases, RDX returns 0.
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

TDH.MEM.RANGE.UNBLOCK finds the blocked Secure EPT entry for the given GPA and level. It checks that the entry has been blocked and TLB tracking has been done, and then it marks the entry as non-blocked (SEPT\_PRESENT or SEPT\_PENDING as appropriate).

10

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.32: TDH.MEM.RANGE.UNBLOCK Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	GPA and Level	Secure EPT page or TD private page	Blob	None	Private	$2^{12+9*\text{Level}}$ Bytes	None	None	None
Explicit	RDX	HPA	TDR page	TDR	R	Opaque	4KB	Shared	Shared	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Shared(i)	N/A	N/A
Implicit	N/A	GPA	Secure EPT tree	N/A	RW	Private	N/A	Exclusive	N/A	N/A

- 5 TDH.MEM.RANGE.UNBLOCK checks the memory operands per the table above when applicable during its flow. The text below does not explicitly mention those checks, except when necessary.

The function checks the following conditions:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
- 10 3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
4. TDCS must have been initialized (TDR.INIT is TRUE).
5. The specified level is of an EPT entry (i.e., 0 to 3 for 4-level EPT or 0 to 4 for 5-level EPT) – see 18.4.2 for a definition of EPT level.

If successful, the function does the following:

- 15 6. Walk the Secure EPT based on the GPA operand, and find the Secure EPT page or TD private page to be unblocked.
7. Check the page's parent Secure EPT entry is blocked (SEPT\_BLOCKED or SEPT\_PENDING\_BLOCKED).
8. Check that TLB tracking was done.

If successful, the function does the following:

- 20 9. Unblock the Secure EPT entry. Atomically set its state to SEPT\_PRESENT (if it was SEPT\_BLOCKED) or SEPT\_PENDING (if it was SEPT\_PENDING\_BLOCKED).

### Completion Status Codes

**Table 20.33: TDH.MEM.RANGE.UNBLOCK Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_EPT_WALK_FAILED	
TDX_GPA_RANGE_NOT_BLOCKED	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	

Completion Status Code	Description
TDX_SUCCESS	TDH.MEM.RANGE.UNBLOCK is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_INITIALIZED	
TDX_TLB_TRACKING_NOT_DONE	

### 20.2.9. TDH.MEM.SEPT.ADD Leaf

Add and map a 4KB Secure EPT page to a TD.

**Table 20.34: TDH.MEM.SEPT.ADD Input Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction leaf number – see 20.2.1		
RCX	EPT mapping information:		
	Bits	Name	Description
	2:0	Level	Level of the non-leaf Secure EPT entry that will map the new Secure EPT page – see 18.4.2 Level must be between 1 and 3 for a 4-level EPT or between 1 and 4 for a 5-level EPT.
	11:3	Reserved	Reserved: must be 0
	51:12	GPA	Bits 51:12 of the guest physical address of to be mapped for the new Secure EPT page Depending on the level, the following least significant bits must be 0: Level 1 (EPT): Bits 20:12 Level 2 (EPD): Bits 29:12 Level 3 (EPDPT): Bits 38:12 Level 4 (EPML4): Bits 47:12
63:52	Reserved	Reserved: must be 0	
RDX	Host physical address of the parent TDR page		
R8	Host physical address of the new Secure EPT page to be added to the TD		
Other	Unmodified		

5

**Table 20.35: TDH.MEM.SEPT.ADD Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
RCX	Extended error information part 1 In case of EPT walk error, Secure EPT entry where the error was detected In other cases, RCX returns 0
RDX	Extended error information part 2 In case of EPT walk error, EPT level where the error was detected In other cases, RDX returns 0
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

TDH.MEM.SEPT.ADD adds a 4KB Secure EPT page to a TD and maps it to the provided GPA. It initializes the page to hold 512 free entries using the TD's ephemeral private key.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

5

**Table 20.36: TDH.MEM.SEPT.ADD Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	GPA and Level	Secure EPT page (GPA) <sup>13</sup>	SEPT_PAGE	RW	Private	2 <sup>12+9*Level</sup> Bytes	N/A	N/A	N/A
Explicit	RDX	HPA	TDR page	TDR	RW	Opaque	4KB	Shared	Shared	Shared
Explicit	R8	HPA	Secure EPT page (HPA) <sup>13</sup>	SEPT_PAGE	RW	Private	4KB	Exclusive	Shared	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Shared(i)	N/A	N/A
Implicit	N/A	GPA	Secure EPT tree	N/A	RW	Private	N/A	Exclusive	N/A	N/A

TDH.MEM.SEPT.ADD checks the memory operands per the table above when applicable during its flow. The text below does not explicitly mention those checks, except when necessary.

The function checks the following conditions:

- 10 1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
4. TDCS must have been initialized (TDR.INIT is TRUE).
- 15 5. The specified level is of an EPT non-leaf entry – i.e., 1 to 3 for 4-level EPT or 1 to 4 for 5-level EPT. See 18.4.2 for a definition of EPT level.
6. The target page metadata in PAMT must be correct (PT must be PT\_NDA).

If successful, the function does the following:

7. Walk the Secure EPT based on the GPA operand, and find the parent EPT entry for the new Secure EPT page.

If the Secure EPT entry is marked as SEPT\_FREE:

- 20 8. Initialize the new Secure EPT page to 0, indicating 512 entries in the SEPT\_FREE state, using the TD's ephemeral private HKID and direct writes (MOVDIR64B).
9. Update the parent Secure EPT entry with the new Secure EPT page HPA and SEPT\_PRESENT state.
10. Increment TDR.CHLDCNT.
- 25 11. Update the new Secure EPT page's PAMT entry with the PT\_EPT page type and the TDR physical address as the OWNER.

### Completion Status Codes

**Table 20.37: TDH.MEM.SEPT.ADD Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_EPT_ENTRY_NOT_FREE	

<sup>13</sup> RCX and R8 denote the same Secure EPT page operand, using HPA and GPA respectively

Completion Status Code	Description
TDX_EPT_WALK_FAILED	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.MEM.SEPT.ADD is successful
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_INITIALIZED	



**20.2.10. TDH.MEM.SEPT.RD Leaf**

Read a Secure EPT entry.

**Table 20.38: TDH.MEM.SEPT.RD Input Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction leaf number – see 20.2.1		
RCX	EPT mapping information:		
	Bits	Name	Description
	2:0	Level	Level of the Secure EPT entry to read – see 18.4.2 Level must be between 0 and 3 for a 4-level EPT or between 0 and 4 for a 5-level EPT.
	11:3	Reserved	Reserved: must be 0
	51:12	GPA	Bits 51:12 of the guest physical address for the Secure EPT entry to read Depending on the level, the following least significant bits must be 0: Level 0 (EPTE): None Level 1 (EPDE): Bits 20:12 Level 2 (EPDPTE): Bits 29:12 Level 3 (EPML4E): Bits 38:12 Level 4 (EPML5E): Bits 47:12
63:52	Reserved	Reserved: must be 0	
RDX	Host physical address of the parent TDR page		

5

**Table 20.39: TDH.MEM.SEPT.RD Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
RCX	In case of successful operation, EPTP or Secure EPT entry contents In case of EPT walk error, Secure EPT entry where the error was detected In other cases, RCX returns 0.
RDX	In case of EPT walk error, EPT level where the error was detected In other cases, RDX returns 0.
Other	Unmodified

**Leaf Function Description**

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

10 TDH.MEM.SEPT.RD reads a Secure EPT entry.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.40: TDH.MEM.SEPT.RDSEPT Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	GPA and Level	Secure EPT entry	SEPT_ENTRY	R	Private	$2^{12+9*\text{Level}}$ Bytes	None	None	None
Explicit	RDX	HPA	TDR page	TDR	R	Opaque	4KB	Shared	Shared	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Shared(i)	N/A	N/A
Implicit	N/A	GPA	Secure EPT Tree	N/A	R	Private	N/A	Shared	N/A	N/A

- 5 TDH.MEM.SEPT.RD checks the memory operands per the table above when applicable during its flow. The text below does not explicitly mention those checks, except when necessary.

The function checks the following conditions:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
- 10 3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
4. TDCS must have been initialized (TDR.INIT is TRUE).
5. The specified level is of an EPT entry (i.e., 0 to 3 for 4-level EPT or 0 to 4 for 5-level EPT) – see 18.4.2 for a definition of EPT level.

If successful, the function does the following:

- 15 6. Walk the Secure EPT based on the GPA operand, and find the Secure EPT entry.
7. Read the Secure EPT entry contents.

### Completion Status Codes

**Table 20.41: TDH.MEM.SEPT.RD Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_EPT_WALK_FAILED	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.MEM.SEPT.RD is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	

---

Completion Status Code	Description
TDX_TD_NOT_INITIALIZED	

**20.2.11. TDH.MEM.SEPT.REMOVE Leaf**

Remove an empty 4KB Secure EPT page from a TD.

**Table 20.42: TDH.MEM.SEPT.REMOVE Input Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction leaf number – see 20.2.1		
RCX	EPT mapping information:		
	Bits	Name	Description
	2:0	Level	Level of the non-leaf Secure EPT entry that maps the Secure EPT page to be removed – see 18.4.2 Level must be between 1 and 3 for a 4-level EPT or between 1 and 4 for a 5-level EPT.
	11:3	Reserved	Reserved: must be 0
	51:12	GPA	Bits 51:12 of the guest physical address for the Secure EPT page to be removed Depending on the level, the following least significant bits must be 0: Level 1 (EPT): Bits 20:12 Level 2 (EPD): Bits 29:12 Level 3 (EPDPT): Bits 38:12 Level 4 (EPML4): Bits 47:12
63:52	Reserved	Reserved: must be 0	
RDX	Host physical address of the parent TDR page		

5

**Table 20.43: TDH.MEM.SEPT.REMOVE Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
RCX	In case of successful operation, HPA of the removed page In case of EPT walk error, Secure EPT entry where the error was detected In other cases, RCX returns 0.
RDX	In case of EPT walk error, EPT level where the error was detected In other cases, RDX returns 0.
Other	Unmodified

**Leaf Function Description**

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.MEM.SEPT.REMOVE removes an empty Secure EPT page, with all 512 marked as SEPT\_FREE, from the TD's Secure EPT tree. On successful operation, it marks the 4KB physical page as free in PAMT.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.44: TDH.MEM.SEPT.REMOVE Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	GPA and Level	Secure EPT page	SEPT_PAGE	R	Private	$2^{12+9*\text{Level}}$ Bytes	Exclusive	None	None
Explicit	RDX	HPA	TDR page	TDR	RW	Opaque	4KB	Shared	Shared	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Shared(i)	N/A	N/A
Implicit	N/A	GPA	Secure EPT Tree	N/A	RW	Private	N/A	Exclusive	N/A	N/A

- 5 TDH.MEM.SEPT.REMOVE checks the memory operands per the table above when applicable during its flow. The text below does not explicitly mention those checks, except when necessary.

The function checks the following conditions:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
- 10 3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
4. TDCS must have been initialized (TDR.INIT is TRUE).
5. The specified level is of a non-leaf EPT entry (i.e., 1 to 3 for 4-level EPT or 1 to 4 for 5-level EPT) – see 18.4.2 for a definition of EPT level.

If successful, the function does the following:

- 15 6. Walk the Secure EPT based on the GPA operand, and find the Secure EPT page to be removed.
7. Check the page's parent Secure EPT entry is a blocked (SEPT\_BLOCKED) non-leaf entry.
8. Check that TLB tracking was done.
9. Scan the Secure EPT page content and check all 512 entries are SEPT\_FREE.

If successful, the function does the following:

- 20 10. Atomically decrement TDR.CHLDCNT.
11. Set the PAMT entry of the removed Secure EPT page to PT\_NDA.
12. Set the parent Secure EPT entry to SEPT\_FREE.

### Completion Status Codes

**Table 20.45: TDH.MEM.SEPT.REMOVE Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_EPT_ENTRY_NOT_FREE	
TDX_EPT_WALK_FAILED	
TDX_GPA_RANGE_NOT_BLOCKED	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	

Completion Status Code	Description
TDX_SUCCESS	TDH.MEM.SEPT.REMOVE is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_INITIALIZED	
TDX_TLB_TRACKING_NOT_DONE	

**20.2.12. TDH.MEM.SEPT.WR Leaf**

Write a free Secure EPT entry.

**Table 20.46: TDH.MEM.SEPT.WR Input Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction leaf number – see 20.2.1		
RCX	EPT mapping information:		
	Bits	Name	Description
	2:0	Level	Level of the Secure EPT entry to write – see 18.4.2
	11:3	Reserved	Reserved: must be 0
	51:12	GPA	Bits 51:12 of the guest physical address for the Secure EPT entry to write Depending on the level, the following least significant bits must be 0: Level 0 (EPTE): None Level 1 (EPDE): Bits 20:12 Level 2 (EPDPTE): Bits 29:12 Level 3 (EPML4E): Bits 38:12 Level 4 (EPML5E): Bits 47:12
63:52	Reserved	Reserved: must be 0	
RDX	Host physical address of the parent TDR page		
R8	Value to write into the secure EPT entry		

5

**Table 20.47: TDH.MEM.SEPT.WR Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
RCX	In case of successful operation, previous Secure EPT entry contents In case of EPT walk error, Secure EPT entry where the error was detected In other cases, RCX returns 0.
RDX	In case of EPT walk error, EPT level where the error was detected In other cases, RDX returns 0.
Other	Unmodified

**Leaf Function Description**

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.MEM.SEPT.WR writes a Secure EPT entry that is not being used by the Intel TDX module – i.e., its state is SEPT\_FREE. Only the bits available to host VMM are written.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.48: TDH.MEM.SEPT.WR Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	GPA and Level	Secure EPT entry	SEPT_ENTRY	RW	Private	$2^{12+9*Level}$ Bytes	None	None	None
Explicit	RDX	HPA	TDR page	TDR	R	Opaque	4KB	Shared	Shared	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Shared(i)	N/A	N/A
Implicit	N/A	GPA	Secure EPT tree	N/A	R	Private	N/A	Shared	N/A	N/A

- 5 TDH.MEM.SEPT.WR checks the memory operands per the table above when applicable during its flow. The text below does not explicitly mention those checks, except when necessary.

The function checks the following conditions:

1. Only the VMM-controlled Secure EPT entry bits (see 18.4) may be set in the new value to be written.
2. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
- 10 3. The TD is not in a FATAL state (TDR.FATAL is FALSE).
4. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
5. TDCS must have been initialized (TDR.INIT is TRUE).
6. The specified level is of an EPT entry (i.e., 0 to 3 for 4-level EPT or 0 to 4 for 5-level EPT) – see 18.4.2 for a definition of EPT level.

- 15 If successful, the function does the following:

7. Walk the Secure EPT based on the GPA operand, and find the Secure EPT entry.
8. Read the Secure EPT entry contents.
9. If the Secure EPT entry is marked as SEPT\_FREE, update the entry's bits available to software (see 18.4) with the input value.

- 20 **Note:** It is the host VMM's responsibility to serialize TDH.MEM.SEPT.WR to the same Secure EPT entry.

### Completion Status Codes

**Table 20.49: TDH.MEM.SEPT.WR Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_EPT_ENTRY_NOT_FREE	
TDX_EPT_WALK_FAILED	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	



Completion Status Code	Description
TDX_SUCCESS	TDH.MEM.SEPT.WR is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_INITIALIZED	

### 20.2.13. TDH.MEM.TRACK Leaf

Increment the TD's TLB epoch counter.

**Table 20.50: TDH.MEM.TRACK Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of the parent TDR page

5

**Table 20.51: TDH.MEM.TRACK Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.MEM.TRACK increments the TD's TLB epoch counter.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.52: TDH.MEM.TRACK Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDR page	TDR	R	Opaque	4KB	Shared	Shared	Shared
Implicit	N/A	N/A	TDCS structure	TDR	RW	Opaque	4KB	Shared(i)	N/A	N/A
Implicit	N/A	N/A	TDCS Epoch Tracking Fields	N/A	RW	Opaque	N/A	Exclusive	N/A	N/A

- 15 In addition to the memory operand checks per the table above, the function checks the following:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
4. TDCS must have been initialized (TDR.INIT is TRUE).
5. The TD build and measurement must have been finalized (by TDH.MR.FINALIZE).

20

If successful, the function does the following as a critical section, protected by exclusively locking the TDCS epoch tracking fields TD\_EPOCH and REFCOUNT. A concurrent TDH.VP.ENTER may cause this locking to fail with a TDX\_OPERAND\_BUSY status code; in this case the caller is expected to retry TDH.MEM.TRACK.

6. Lock the TDCS epoch tracking fields in exclusive mode.
7. Check that the TD's previous epoch's REFCOUNT is 0. This guarantees that no REFCOUNT information will be lost when TD\_EPOCH is incremented in the next step.
8. If successful, increment the TD's epoch counter (TDCS.TD\_EPOCH).
9. Release the exclusive mode locking of the epoch tracking fields.

**Completion Status Codes****Table 20.53: TDH.MEM.TRACK Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_PREVIOUS_TLB_EPOCH_BUSY	
TDX_SUCCESS	TDH.MEM.TRACK is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_FINALIZED	
TDX_TD_NOT_INITIALIZED	

### 20.2.14. TDH.MNG.ADDCX Leaf

Add a TDCX page to a guest TD.

**Table 20.54: TDH.MNG.ADDCX Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a page where TDCX will be added
RDX	The physical address of the owner TDR page

5

**Table 20.55: TDH.MNG.ADDCX Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

10 TDH.MNG.ADDCX adds a TDCX page, which is a child of the specified TDR.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX Interface functions.

**Table 20.56: TDH.MNG.ADDCX Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDCX page	Blob	RW	Opaque	4KB	Exclusive	Shared	Shared
Explicit	RDX	HPA	TDR page	TDR	RW	Opaque	4KB	Exclusive	Shared	Shared

15 In addition to the explicit memory operand checks per the table above, the function checks the following conditions:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
3. The TD must not have been initialized (TDR.INIT is FALSE).
4. The number of TDCX pages (TDR.NUM\_TDCX) is smaller than the required number.
- 20 5. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
6. The new TDCX page metadata in PAMT must be correct (PT must be PT\_NDA).

If successful, the function does the following:

7. Initialize the TDCX page contents using direct writes (MOVDIR64B).
8. Set the TDCX pointer entry in the TDR.TDCX\_PA array.
- 25 9. Increment TDR.NUM\_TDCX.

## Completion Status Codes

Table 20.57: TDH.MNG.ADDCX Completion Status Codes (Returned in RAX) Definition

Completion Status Code	Description
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.MNG.ADDCX is successful
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_INITIALIZED	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TDCX_NUM_INCORRECT	

### 20.2.15. TDH.MNG.CREATE Leaf

Create a new guest TD and its TDR root page.

**Table 20.58: TDH.MNG.CREATE Input Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction leaf number – see 20.2.1		
RCX	The physical address of a page where TDR will be created		
RDX	Bits	Name	Description
	15:0	HKID	The TD's ephemeral private HKID
	63:16	Reserved	Reserved: must be 0

5

**Table 20.59: TDH.MNG.CREATE Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

10 TDH.MNG.CREATE creates a TDR page which is the root page of a new guest TD.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.60: TDH.MNG.CREATE Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDR page	TDR	RW	Opaque	4KB	Exclusive	Shared	Shared
Implicit	N/A	N/A	KOT	KOT	N/A	Hidden	N/A	Exclusive	N/A	N/A

15 In addition to the explicit memory operand checks per the table above, the function checks the following conditions:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_NDA).
2. The value of the specified HKID must be in the range configured for TDX.
3. The KOT entry for the specified HKID must be marked as HKID\_FREE.

If successful, the function does the following:

4. Zero out the TDR page contents using direct write (MOVDIR64B).
  5. Initialize the key management fields.
  6. Initialize the state variables.
  7. Initialize the TD management fields.
  8. Mark the KOT entry for the specified HKID as HKID\_ASSIGNED.
  9. Initialize the TDR page metadata in PAMT.
- 25

**Completion Status Codes****Table 20.61: TDH.MNG.CREATE Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_HKID_NOT_FREE	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.MNG.CREATE is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	

### 20.2.16. TDH.MNG.INIT Leaf

Initialize TD-scope control structures TDR and TDCS.

**Table 20.62: TDH.MNG.INIT Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a TDR page
RDX	The physical address of an input TD_PARAMS_STRUCT

5

**Table 20.63: TDH.MNG.INIT Output Operands Definition**

Operand	Description									
RAX	SEAMCALL instruction return code – see 20.2.1									
RCX	Extended error information In case of a TD_PARAMS_STRUCT.CPUID_CONFIG error, RCX returns the applicable CPUID information as shown below. In all other cases, RCX returns 0.									
	<table border="1"> <thead> <tr> <th>Bits</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>31:0</td> <td>LEAF</td> <td>CPUID leaf number</td> </tr> <tr> <td>63:32</td> <td>SUBLEAF</td> <td>CPUID sub-leaf number: if sub-leaf is not applicable, value is -1 (0xFFFFFFFF).</td> </tr> </tbody> </table>	Bits	Name	Description	31:0	LEAF	CPUID leaf number	63:32	SUBLEAF	CPUID sub-leaf number: if sub-leaf is not applicable, value is -1 (0xFFFFFFFF).
	Bits	Name	Description							
31:0	LEAF	CPUID leaf number								
63:32	SUBLEAF	CPUID sub-leaf number: if sub-leaf is not applicable, value is -1 (0xFFFFFFFF).								
Other	Unmodified									

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.MNG.INIT initializes the TD-scope control structures TDR and TDCS based on a set of TD parameters provided as input.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.64: TDH.MNG.INIT Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDR page	TDR	RW	Opaque	4KB	Exclusive	Shared	Shared
Explicit	RDX	HPA	TD Parameters	TD_PARAMS	R	Shared	1024B	None	N/A	N/A
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Exclusive(i)	N/A	N/A

15

In addition to the explicit memory operand checks per the table above, the function checks the following conditions:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).



3. The TD must not have been initialized (TDR.INIT is FALSE).
4. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
5. All the TDCX pages have been added (by TDH.MNG.ADDCX).

If successful, the function does the following:

- 5
  6. Set the TDCS TD management fields to their initial values.
  7. Read the input parameters structure fields.
  8. Check the input parameters and initialize the TDCS logical structure.
    - 8.1. Check that ATTRIBUTES and XFAM bits that must be fixed-0 or fixed-1 are set correctly.
    - 8.2. Check XFAM bit groups that must have certain values (e.g., AVX bits 7:5).
- 10 If passed:
  9. Initialize EPTP to point to TDCS.SEPT\_ROOT.
  10. Initialize the MSR bitmaps based on ATTRIBUTES and XFAM.
  11. Initialize the TDCS measurement fields.
  12. Mark the TD as initialized (set TDR.INIT to TRUE).

## 15 Completion Status Codes

**Table 20.65: TDH.MNG.INIT Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.MNG.INIT is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_INITIALIZED	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TDCX_NUM_INCORRECT	

### 20.2.17. TDH.MNG.KEY.CONFIG Leaf

Configure the TD ephemeral private key on a single package.

**Table 20.66: TDH.MNG.KEY.CONFIG Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a TDR page

5

**Table 20.67: TDH.MNG.KEY.CONFIG Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

10 TDH.MNG.KEY.CONFIG configures the TD’s ephemeral private key on a single package.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.68: TDH.MNG.KEY.CONFIG Operands Information**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDR page	TDR	RW	Opaque	4KB	Exclusive	Shared	Shared
Implicit	N/A	N/A	KETs on current package	N/A	N/A	Hidden	N/A	Exclusive	N/A	N/A

15 In addition to the memory operand checks per the table above, the function checks the following conditions:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
3. All HKIDs must be assigned to the TD; the TDR key management state must be TD\_HKID\_ASSIGNED.

If successful, the function does the following:

- 20
4. Configure the TD ephemeral private key on the package.
    - 4.1. This operation may fail due to a conflict with a concurrent TDH.MNG.KEY.CONFIG or PCONFIG running on the same package.
    - 4.2. A CPU-generated random key is used. The operation may fail due to lack of entropy.
  5. If the key has been configured on all the packages, set the TDR key management state to TD\_KEYS\_CONFIGURED.

25 **Completion Status Codes**

**Table 20.69: TDH.MNG.KEY.CONFIG Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_KEY_CONFIGURED	

Completion Status Code	Description
TDX_KEY_GENERATION_FAILED	
TDX_KEY_STATE_INCORRECT	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.MNG.KEY.CONFIG is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	

**20.2.18. TDH.MNG.KEY.FREEID Leaf**

End the platform cache flush sequence, and mark applicable HKIDs in KOT as free.

**Table 20.70: TDH.MNG.KEY.FREEID Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a TDR page

5

**Table 20.71: TDH.MNG.KEY.FREEID Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

**Leaf Function Description**

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.MNG.KEY.FREEID ends the platform cache flush sequence for the HKIDs associated with the specified TD after TDH.PHYMEM.CACHE.WB has been executed on all the required packages. It marks the TD's HKIDs in KOT as free, and the TD itself as being torn down.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

15

**Table 20.72: TDH.MNG.KEY.FREEID Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDR page	TDR	RW	Opaque	4KB	Exclusive	Shared	Shared
Implicit	N/A	N/A	KOT	KOT	N/A	Hidden	N/A	Exclusive	N/A	N/A

In addition to the memory operand checks per the table above, the function checks the following conditions:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
  2. There should be no VCPUs associated with any LP (all cached VCPU state must have been flushed to TDVPS).
- 20 For each KOT entry associated with the specified TD, the function checks the following conditions:
3. The KOT entry is marked as HKID\_RECLAIMED – having been reclaimed earlier by TDH.MNG.KEY.RECLAIMID.
  4. The KOT entry indicates that TDH.PHYMEM.CACHE.WB has been executed on all applicable packages or cores.

If successful, the function does the following:

5. Marks the KOT entry as HKID\_FREE.
  6. Set the TD's key management state to TD\_TEARDOWN.
- 25

**Completion Status Codes****Table 20.73: TDH.MNG.KEY.FREEID Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_KEY_STATE_INCORRECT	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.MNG.KEY.FREEID is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_WBCACHE_NOT_COMPLETE	

### 20.2.19. TDH.MNG.KEY.RECLAIMID Leaf

Reclaim all the HKIDs assigned to a TD.

**Table 20.74: TDH.MNG.KEY.RECLAIMID Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a TDR page

5

**Table 20.75: TDH.MNG.KEY.RECLAIMID Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.MNG.KEY.RECLAIMID reclaims the HKID assigned to the TD and marks the applicable KOT entries as HKID\_RECLAIMED.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.76: TDH.MNG.KEY.RECLAIMID Operands Information**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDR page	TDR	RW	Opaque	4KB	Exclusive	Shared	Shared
Implicit	N/A	N/A	KOT	KOT	N/A	Hidden	N/A	Exclusive	N/A	N/A

15

In addition to the memory operand checks per the table above, the function checks the following conditions:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. HKIDs are assigned to the TD; the TDR key management state must be either TD\_HKID\_ASSIGNED or TD\_KEYS\_CONFIGURED.
- 20 3. The KOT entry for the TD's assigned HKID in the list must be marked as HKID\_ASSIGNED.

If successful, the function does the following:

4. Mark the KOT entry for the TD's HKID as HKID\_RECLAIMED.
5. Set the TDR key management state to TD\_BLOCKED.

#### Completion Status Codes

25

**Table 20.77: TDH.MNG.KEY.RECLAIMID Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_KEY_STATE_INCORRECT	
TDX_OPERAND_ADDR_RANGE_ERROR	

Completion Status Code	Description
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.MNG.KEY.RECLAIMID is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	

### 20.2.20. TDH.MNG.RD Leaf

Read a TD-scope control structure field of a debuggable TD.

**Table 20.78: TDH.MNG.RD Operands**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a TDR page
RDX	Field code – see 0

5 **Table 20.79: TDH.MNG.RD Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
R8	Contents of the field
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

10 TDH.MNG.RD writes a TD-scope control structure field of a debuggable TD.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.80: TDH.MNG.RD Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDR page	TDR	R	Opaque	4KB	Shared	Shared	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	R	Opaque	N/A	Shared(i)	N/A	N/A

15 In addition to the memory operand checks per the table above, the function checks the following conditions:

1. The provided field code is valid and indicates a readable field.
2. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
3. The TD is not in a FATAL state (TDR.FATAL is FALSE).
4. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
- 20 5. TDCS must have been initialized (TDR.INIT is TRUE).
6. The TD is debuggable (TDCS.ATTRIBUTES.DEBUG is 1).

If the above checks pass, the function does the following:

7. Read the TD field.



**Completion Status Codes****Table 20.81: TDH.MNG.RD Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.MNG.RD is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NON_DEBUG	
TDX_TD_NOT_INITIALIZED	

### 20.2.21. TDH.MNG.VPFLUSHDONE Leaf

Check that none of the TD's VCPUs are associated with an LP.

**Table 20.82: TDH.MNG.VPFLUSHDONE Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a TDR page

5

**Table 20.83: TDH.MNG.VPFLUSHDONE Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.MNG.VPFLUSHDONE checks that none of the TD's VCPUs are associated with an LP, and it then prepares for cache flushing by TDH.PHYMEM.CACHE.WB.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.84: TDH.MNG.VPFLUSHDONE Operands Information**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDR page	TDR	RW	Opaque	4KB	Exclusive	Shared	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	R	Opaque	N/A	Exclusive(i)	N/A	N/A
Implicit	N/A	N/A	KOT	KOT	N/A	Hidden	N/A	Exclusive	N/A	N/A

15

In addition to the memory operand checks per the table above, the function checks the following conditions:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
  2. The KOT entry for the TD's assigned HKID in the list must be marked as HKID\_RECLAIMED.
  3. None of the TD's VCPUs are associated with an LP (either the TD has not been initialized by TDH.MNG.INIT, or TDCS.NUM\_ASSOC\_VCPUS is 0).
- 20

If successful, the function does the following:

4. Set a bitmap in the KOT entry to track the required subsequent TDH.PHYMEM.CACHE.WB operations.
5. Mark the KOT entry as HKID\_FLUSHED.

#### Completion Status Codes

25

**Table 20.85: TDH.MNG.VPFLUSHDONE Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_FLUSHVP_NOT_DONE	

Completion Status Code	Description
TDX_KEY_STATE_INCORRECT	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.MNG.VPFLUSHDONE is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	

**20.2.22. TDH.MNG.WR Leaf**

Write a TD-scope control structure field of a debuggable TD.

There are no writable fields. TDH.MNG.WR is a placeholder and returns a constant value of TDX\_OPERAND\_INVALID, see below.

5 **Table 20.86: TDH.MNG.WR Operands**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a TDR page
RDX	Field code – see 0
R8	Data to write to the field
R9	64b mask to indicate which bits of the value in R8 are to be written to the field

**Table 20.87: TDRDGWR Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
R8	Previous content of the field
Other	Unmodified

**Leaf Function Description**

10 **Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

TDH.MNG.WR writes a TD-scope control structure field of a debuggable TD. The specific bits of the value (R8) are written as specified by the write mask (R9). Writing is subject to the field's writability.

15 To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.88: TDH.MNG.WR Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDR page	TDR	RW	Opaque	4KB	Shared	Shared	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	R	Opaque	N/A	Shared(i)	N/A	N/A

There are no writable fields. TDH.MNG.WR returns a constant value of TDX\_OPERAND\_INVALID indicating an invalid field code.

20 **Completion Status Codes**

**Table 20.89: TDH.MNG.WR Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_INVALID	



**20.2.23. TDH.MR.EXTEND Leaf**

Extend the MRTD measurement register in the TDCS with the measurement of the indicated chunk of a TD page.

**Table 20.90: TDH.MR.EXTEND Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The GPA of the TD page chunk to be measured
RDX	The TDR page of the target TD

5

**Table 20.91: TDH.MR.EXTEND Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
RCX	Extended error information part 1 In case of EPT walk error, Secure EPT entry where the error was detected In other cases, RCX returns 0.
RDX	Extended error information part 2 In case of EPT walk error, EPT level where the error was detected In other cases, RDX returns 0.
Other	Unmodified

**Leaf Function Description**

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.MR.EXTEND updates the MRTD measurement register in the TDCS with the measurement of the indicated chunk of a TD private page. For pages whose contents need to be measured, once the page is copied into the TD memory area, the host VMM will call TDH.MR.EXTEND multiple times to measure the pages contents into MRTD. TDEXEND can be executed only before TDH.MR.FINALIZE.

**Note:** TDH.MR.EXTEND works on a 256B chunk of a page, not on a full page, due to instruction latency considerations.

- 15 To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.92: TDH.MR.EXTEND Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	GPA	TD private page chunk	Blob	RW	Private	256B	None	None	None
Explicit	RDX	HPA	TDR page	TDR	R	Opaque	4KB	Exclusive	Shared	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	4KB	Exclusive(i)	N/A	N/A
Implicit	N/A	GPA	Secure EPT tree	N/A	R	Private	N/A	Shared	N/A	N/A

In addition to the memory operand checks per the table above, the function checks the following:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
- 5 4. TDCS must have been initialized (TDR.INIT is TRUE).
5. The TD build and measurement must not have been finalized (by TDH.MR.FINALIZE).
6. The page must be mapped and accessible in the Secure EPT.

If successful, the function does the following:

7. Update the TD measurement in TDCS based on the chunk's GPA and contents.
- 10 8. Extend TDCS.MRTD with the chunk's GPA and contents. Extension is done using SHA384, with three 128B extension buffers. The first extension buffer is composed as follows:
  - o Bytes 0 through 9 contain the ASCII string "TDH.MR.EXTEND".
  - o Bytes 16 through 23 contain the GPA (in little-endian format).
  - o All the other bytes contain 0.
- 15 The other two extension buffers contain the chunk's contents.

### Completion Status Codes

**Table 20.93: TDH.MR.EXTEND Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_EPT_ENTRY_NOT_PRESENT	
TDX_EPT_WALK_FAILED	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.MR.EXTEND is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_FINALIZED	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_INITIALIZED	

### 20.2.24. TDH.MR.FINALIZE Leaf

- 20 TDH.MR.FINALIZE completes measurement of the initial TD contents and marks the TD as ready to run.

**Table 20.94: TDH.MR.FINALIZE Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of the parent TDR page

**Table 20.95: TDH.MR.FINALIZE Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

**Leaf Function Description**

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

TDH.MR.FINALIZE completes the measurement of the initial TD contents and marks the TD as finalized.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.96: TDH.MR.FINALIZE Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDR page	TDR	R	Opaque	4KB	Exclusive	Shared	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	4KB	Exclusive(i)	N/A	N/A

In addition to the memory operand checks per the table above, the function checks the following:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
4. TDCS must have been initialized (TDR.INIT is TRUE).
5. The TD build and measurement must not have been finalized (by TDH.MR.FINALIZE).

If successful, the function does the following:

6. Finalize the TD measurement.
7. Mark the TD as finalized.

**Completion Status Codes****Table 20.97: TDH.MR.FINALIZE Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.MR.FINALIZE is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_FINALIZED	



Completion Status Code	Description
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_INITIALIZED	

### 20.2.25. TDH.PHYMEM.CACHE.WB Leaf

TDH.PHYMEM.CACHE.WB is an interruptible and restartable function to write back the cache hierarchy on a package or a core.

**Table 20.98: TDH.PHYMEM.CACHE.WB Input Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction leaf number – see 20.2.1		
RCX	Command, as described below:		
	Value	Name	Description
	0	TDH.PHYMEM.CACHE.WB_START_CMD	Start a new TDH.PHYMEM.CACHE.WB cycle with no cache invalidation.
	1	TDH.PHYMEM.CACHE.WB_RESUME_CMD	Resume a previously-interrupted TDH.PHYMEM.CACHE.WB cycle with no cache invalidation.
Other		Reserved	

5

**Table 20.99: TDH.PHYMEM.CACHE.WB Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

TDH.PHYMEM.CACHE.WB writes back the cache hierarchy to memory and updates the KOT state to allow reuse of HKIDs.

- TDH.PHYMEM.CACHE.WB does not invalidate cache lines.
- The function is interruptible by external events and is restartable. In case it is interrupted by an external event, information is stored in an Intel TDX module internal table which allows the instruction to be restarted.
- The function operates on cache lines associated with any HKID.
- The function guarantees write back of at least those cache lines where the state of that HKID (in the KOT) was HKID\_FLUSHED at the time of the first invocation (RCX == TDH.PHYMEM.CACHE.WB\_START\_CMD (0)).
- Depending on the implementation, the instruction may write back additional cache lines.
- The scope at which TDH.PHYMEM.CACHE.WB operates (e.g., package or core) is determined at Intel TDX module initialization time.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.100: TDH.PHYMEM.CACHE.WB (Implicit) Operands Information**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Implicit	N/A	N/A	KOT	KOT	N/A	Hidden	N/A	Shared	N/A	N/A
Implicit	N/A	N/A	WBT entry for current scope	WBT_ENTRY	N/A	Hidden	N/A	Exclusive	N/A	N/A

In addition to the memory operand checks per the table above, the function checks the following conditions:

1. The command value is one of the supported ones.
2. If the command is to start a new TDH.PHYMEM.CACHE.WB cycle (RCX == 0), then:
  - 2.1. Clear the internally saved interruption state.
  - 2.2. Scan the KOT: mark those HKIDs whose state is HKID\_FLUSHED in an internal table; only those HKIDs will be later marked as written back and invalidated upon successful completion of TDH.PHYMEM.CACHE.WB.
  - 2.3. If none of the KOT entries for the requested set of HKIDs (either single or all) is in HKID\_FLUSHED state, then abort with an informational code (it achieved its goal: write back and invalidate at least the HKIDs that are in the HKID\_FLUSHED state).
3. Run cache write back operation on the cache hierarchy of the current package or core. This operation is long and may be interrupted by external events.
  - 3.1. If a previous TDH.PHYMEM.CACHE.WB has been interrupted, the operation resumes from the interruption point which has been recorded.
  - 3.2. In case of interruption, the current point in the write back and invalidation flow and the current HKID are recorded.
4. If the operation has not been interrupted, update the KOT as follows:
  - 4.1. For each KOT entry, if the entry was marked as HKID\_FLUSHED at the start of the TDH.PHYMEM.CACHE.WB cycle as discussed above, use the KOT entry's bitmap to indicate that TDH.PHYMEM.CACHE.WB has been executed on this package or core.

### Error and Informational Codes

**Table 20.101: TDH.PHYMEM.CACHE.WB Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_INTERRUPTED_RESUMABLE	
TDX_NO_HKID_READY_TO_WBCACHE	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_SUCCESS	TDH.PHYMEM.CACHE.WB is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	

**20.2.26. TDH.PHYMEM.PAGE.RD Leaf**

Read a 64b chunk from a debuggable guest TD private memory.

**Table 20.102: TDH.VP.RDBGWRMEM Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a naturally-aligned 8-byte chunk of a guest TD private page

5

**Table 20.103: TDH.PHYMEM.PAGE.RD Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
RDX	Content of the memory chunk
Other	Unmodified

**Leaf Function Description**

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.PHYMEM.PAGE.RD reads a 64b chunk from a debuggable guest TD private memory.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.104: TDH.PHYMEM.PAGE.RD Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TD private page chunk	Blob	R	Private	8B	Shared	Shared	Shared
Implicit	N/A	HPA	TDR page	TDR	R	Opaque	N/A	Shared	N/A	N/A
Implicit	N/A	N/A	TDCS structure	TDCS	R	Opaque	N/A	Shared(i)	N/A	N/A

- 15 In addition to the memory operand checks per the table above, the function checks the following conditions:

1. The TD private page metadata in PAMT must be correct (PT must be PT\_REG).
2. No fatal error has occurred (TDR.FATAL is FALSE).
3. The TD keys be configured on the hardware (TDR.KEYT\_STATE is TD\_KEYS\_CONFIGURED).
4. TDCS must have been initialized (TDR.INIT is TRUE).
5. The TD is a debuggable TD (TDCS.ATTRIBUTES.DEBUG is 1).

20

If the above checks pass, the function does the following:

6. Read the content of the memory chunk.

**Completion Status Codes****Table 20.105: TDH.PHYMEM.PAGE.RD Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDDBGREDMEM is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NON_DEBUG	
TDX_TD_NOT_INITIALIZED	

**20.2.27. TDH.PHYMEM.PAGE.RDMD Leaf**

Read the metadata of a page (or the metadata of the containing large page) in TDMR.

**Table 20.106: TDH.PHYMEM.PAGE.RDMD Operands**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	A physical address of a 4KB page in TDMR

5

**Table 20.107: TDH.PHYMEM.PAGE.RDMD Output Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction return code – see 20.2.1		
RCX	Page Type (PT):		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0	PT_NDA	The physical page is <b>Not Directly Assigned</b> to the Intel TDX module.
	1	PT_RSVD	The physical page is reserved for non-TDX usage.
	3	PT_REG	The physical page holds TD private memory.
	4	PT_TDR	The physical page holds the TD Root (TDR) control structure.
	8:5		The physical page holds a TD control structure.
Other		Reserved	
RDX	OWNER: the HPA of the TD's TDR control structure page (if applicable)		
R8	<b>Bits</b>	<b>Name</b>	<b>Description</b>
	2:0	Size	Size of the containing 4KB, 2MB or 1GB page – see 18.3.1
	63:3	Reserved	Set to 0
R9	BEPOCH		
R10	Reserved: set to 0		
R11	Reserved: set to 0		
Other	Unmodified		

**Leaf Function Description**

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.PHYMEM.PAGE.RDMD finds the containing page (4KB, 2MB or 2GB) of the given page in TDMR and reads its metadata from its PAMT entry.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.108: TDH.PHYMEM.PAGE.RDMD Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	Target page	Blob	None	Opaque/ Private	4KB	Shared	Shared	Shared

5 If the memory operand checks per the table above pass, the function does the following:

1. Do a PAMT walk, and find the containing page and its size.

If passed:

2. Read the PAMT entry.

#### Completion Status Codes

10

**Table 20.109: TDH.PHYMEM.PAGE.RDMD Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_SUCCESS	TDH.PHYMEM.PAGE.RDMD is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	

**20.2.28. TDH.PHYMEM.PAGE.RECLAIM Leaf**

Reclaim a physical 4KB, 2MB or 1GB TD-owned page (i.e., TD private page, Secure EPT page or a control structure page) from a TD, given its HPA.

**Table 20.110: TDH.PHYMEM.PAGE.RECLAIM Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a 4KB, 2MB or 1GB page to be reclaimed

5

**Table 20.111: TDH.PHYMEM.PAGE.RECLAIM Output Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction return code – see 20.2.1		
RCX	PT		
RDX	OWNER		
R8	<b>Bits</b>	<b>Name</b>	<b>Description</b>
	2:0	Size	Size of the containing 4KB, 2MB or 1GB page – see 18.3.1
	63:3	Reserved	Set to 0
R9	Reserved: set to 0		
R10	Reserved: set to 0		
R11	Reserved: set to 0		
Other	Unmodified		

**Leaf Function Description**

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

10

TDH.PHYMEM.PAGE.RECLAIM reclaims a TD-owned physical page from the TD.

TDH.PHYMEM.PAGE.RECLAIM can reclaim pages only if the owner TD is in the TD\_TEARDOWN state.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

15

**Table 20.112: TDH.PHYMEM.PAGE.RECLAIM Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	Target page	Blob	RW	Opaque/ Private	4KB, 2MB or 1GB	Exclusive	Shared	Shared



Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Implicit	N/A	N/A	TDR page <sup>14</sup>	TDR	RW	Opaque	4KB	Shared	N/A	N/A

TDH.PHYMEM.PAGE.RECLAIM checks the memory operands per the table above when applicable during its flow. The text below does not explicitly mention those checks, except when necessary.

The function works as follows:

- 5 1. Check that the target page metadata in PAMT are correct (PT must not be PT\_NDA nor PT\_RSVD).
2. If the target page is not a TDR (PT is not PT\_TDR):
  - 2.1. Get the TDR page (pointed by the target page's PAMT.OWNER).
  - 2.2. Check that the TD is in teardown state (TDR.KEY\_STATE is TD\_TEARDOWN).
  - 2.3. Atomically decrement TDR.CHLDLCNT.
- 10 3. Else (target page is a TDR):
  - 3.1. Check that the TD is in teardown state (TDR.KEY\_STATE is TD\_TEARDOWN).
  - 3.2. Check that TDR.CHLDLCNT is 0.
4. Update the PAMT entry of the reclaimed page to PT\_NDA.
5. Return the page metadata (as they were before PAMT update above).

#### 15 Completion Status Codes

**Table 20.113: TDH.PHYMEM.PAGE.RECLAIM Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_KEY_STATE_INCORRECT	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.PHYMEM.PAGE.RECLAIM is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_ASSOCIATED_PAGES_EXIST	

<sup>14</sup> Except when TDR is the target page

**20.2.29. TDH.PHYMEM.PAGE.WBINVD Leaf**

Write back and invalidate all cache lines associated with the specified memory page and HKID.

**Table 20.114: TDH.PHYMEM.PAGE.WBINVD Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	Physical address of a 4KB page in TDMR, including HKID bits

5

**Table 20.115: TDH.PHYMEM.PAGE.WBINVD Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

**Leaf Function Description**

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.PHYMEM.PAGE.WBINVD performs cache write back and invalidation on all the cache lines associated with the specified page and HKID. The page must not be in use by the Intel TDX module (i.e., not assigned to a TD as a private page or a Secure EPT page), nor used as a control structure page.

It is the responsibility of the host VMM to track which HKID is associated with the target page; the function does not check it.

- 15 To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.116: TDH.PHYMEM.PAGE.WBINVD Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	Target page	Blob	R	Private/ Opaque	4KB	Shared	Shared	Shared

In addition to the memory operand checks per the table above, the function checks the following conditions:

- 20 1. The target page must be marked in PAMT as not controlled by the Intel TDX module (PT must be PT\_NDA).

If successful, the function performs the following:

2. Write back and invalidate all the cache lines for the given target HPA and HKID.

**Completion Status Codes****Table 20.117: TDH.PHYMEM.PAGE.WBINVD Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	

Completion Status Code	Description
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.PHYMEM.PAGE.WBINVD is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	

### 20.2.30. TDH.PHYMEM.PAGE.WR Leaf

Write a 64b chunk to a debuggable guest TD private memory.

**Table 20.118: TDH.PHYMEM.PAGE.WR Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a naturally-aligned 8-byte chunk of a guest TD private page
RDX	Data to write to memory

5

**Table 20.119: TDH.PHYMEM.PAGE.WR Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
RDX	Previous content of the memory chunk
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

10 TDH.PHYMEM.PAGE.WR writes a 64b chunk to a debuggable guest TD private memory.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.120: TDH.PHYMEM.PAGE.WR Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TD private page chunk	Blob	RW	Private	8B	Shared	Shared	Shared
Implicit	N/A	HPA	TDR page	TDR	R	Opaque	N/A	Shared	N/A	N/A
Implicit	N/A	N/A	TDCS structure	TDCS	R	Opaque	N/A	Shared(i)	N/A	N/A

15 In addition to the memory operand checks per the table above, the function checks the following conditions:

1. The TD private page metadata in PAMT must be correct (PT must be PT\_REG).
2. No fatal error has occurred (TDR.FATAL is FALSE).
3. The TD keys be configured on the hardware (TDR.KEYT\_STATE is TD\_KEYS\_CONFIGURED).
4. TDCS must have been initialized (TDR.INIT is TRUE).
5. The TD is a debuggable TD (TDCS.ATTRIBUTES.DEBUG is 1).

20

If the above checks pass, the function does the following:

6. Read the previous content of the memory chunk, and write the new value.

**Completion Status Codes****Table 20.121: TDH.PHYMEM.PAGE.WR Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.PHYMEM.PAGE.WR is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NON_DEBUG	
TDX_TD_NOT_INITIALIZED	

### 20.2.31. TDH.SYS.CONFIG Leaf

Globally configure the Intel TDX module.

**Table 20.122: TDH.SYS.CONFIG Input Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction leaf number – see 20.2.1		
RCX	The physical address of an array of pointers, each containing the physical address of a single TDMR_INFO entry (see 18.6.4). The pointer array must be sorted such that TDMR base addresses (TDMR_INFO.TDMR_BASE) are sorted from the lowest to the highest base address, and TDMRs do not overlap with each other.		
RDX	The number of pointers in the above buffer, up to 64		
R8	Bits	Name	Description
	15:0	HKID	Intel TDX global private HKID value
	63:16	Reserved	Reserved: must be 0

5

**Table 20.123: TDH.SYS.CONFIG Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.SYS.CONFIG performs global (platform-scope) configuration of the Intel TDX module. This function is intended to be executed during OS/VMM boot, and thus it has relaxed latency requirements.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.124: TDH.SYS.CONFIG Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDMR Info Pointers	Array of HPA	R	Shared	512B	None	N/A	N/A
Explicit	N/A	HPA	TDMR Info	TDMR_INFO	R	Shared	512B	None	N/A	N/A
Implicit	N/A	N/A	All Intel TDX module internal variables	N/A	RW	Hidden	N/A	Exclusive	N/A	N/A

15

In addition to the memory operand checks per the table above, the function checks the following conditions:

1. Global and LP-scope initialization has been done:
  - 1.1. PL.SYS\_STATE is SYSINIT\_DONE.
  - 1.2. TDH.SYS.LP.INIT has been executed on all LPs.
2. The number of TDMR\_INFO entries does not exceed the supported number of TDMRs.
3. Check each pointer to TDMR\_INFO; read the applicable TDMR\_INFO entry; check and update the internal TDMR\_TABLE with TDMR, reserved areas and PAMT setup:
  - 3.1. TDMRs must be sorted in an ascending base address order.
  - 3.2. For each TDMR:
    - 3.2.1. TDMR base address must be aligned on 1GB.
    - 3.2.2. TDMR size must be greater than 0 and a whole multiple of 1GB.
    - 3.2.3. TDMR base address must comply with the platform's maximum PA, and their HKID bits must be 0.
    - 3.2.4. For each PAMT region (1G, 2M and 4K) of each TDMR:
      - 3.2.4.1. PAMT base address must comply with the alignment requirements.
      - 3.2.4.2. PAMT base address must comply with the platform's maximum PA, and the HKID bits must be 0.
      - 3.2.4.3. The size of each PAMT region must be large enough to contain the PAMT for its associated TDMR.
    - 3.2.5. Reserved areas within TDMR must be sorted in an ascending offset order.
    - 3.2.6. A null reserved area (indicated by a size of 0) may be followed only by other null reserved areas.
    - 3.2.7. For each reserved area within TDMR:
      - 3.2.7.1. Offset and size must comply with the alignment and granularity requirements.
      - 3.2.7.2. Reserved areas must not overlap.
      - 3.2.7.3. Reserved areas must be fully contained within their TDMR.
  - 3.3. TDMRs must not overlap with other TDMRs.
  - 3.4. PAMTs must not overlap with other PAMTs.
  - 3.5. TDMRs' non-reserved parts and PAMTs must not overlap (PAMTs may reside within TDMR reserved areas).
  - 3.6. TDMRs' non-reserved parts must be contained in convertible memory – i.e., in CMRs.
  - 3.7. PAMTs must be contained in convertible memory – i.e., in CMRs.
4. Check and set the Intel TDX global private HKID. The provided HKID must be in the TDX HKID range.

If successful, the function does the following:

5. Complete the initialization of the Intel TDX module at platform scope.
6. Set PL.SYS\_STATE to SYSCONFIG\_DONE.

### Completion Status Codes

**Table 20.125: TDH.SYS.CONFIG Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_INVALID_PAMT	
TDX_INVALID_RESERVED_IN_TDMR	
TDX_INVALID_TDMR	
TDX_NON_ORDERED_RESERVED_IN_TDMR	
TDX_NON_ORDERED_TDMR	
TDX_OPERAND_INVALID	
TDX_PAMT_OUTSIDE_CMRS	
TDX_PAMT_OVERLAP	
TDX_SUCCESS	TDH.SYS.CONFIG is successful.
TDX_SYS_BUSY	
TDX_SYS_SHUTDOWN	

Completion Status Code	Description
TDX_SYSINIT_NOT_DONE	
TDX_SYSINITLP_NOT_DONE	
TDX_TDMR_ALREADY_INITIALIZED	
TDX_TDMR_OUTSIDE_CMRS	



### 20.2.32. TDH.SYS.INFO Leaf

Provide information about the Intel TDX module and the convertible memory.

**Table 20.126: TDH.SYS.INFO Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a buffer where the output TDSYSINFO_STRUCT will be written
RDX	The number of bytes in the above buffer
R8	The physical address of a buffer where an array of CMR_INFO will be written
R9	The number of CMR_INFO entries in the above buffer

5

**Table 20.127: TDH.SYS.INFO Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
RDX	The actual number of bytes written to the above buffer
R9	The number of CMR_INFO entries actually written to the above buffer
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.SYS.INFO provides information about the Intel TDX module and about the memory configuration.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.128: TDH.SYS.INFO Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDX system information structure	TDSYSINFO_STRUCT	RW	Shared	1024B	None	N/A	N/A
Explicit	R8	HPA	CMR table	CMR_INFO_ARRAY	RW	Shared	512B	None	N/A	N/A

- 15 In addition to the memory operand checks per the table above, the function checks the following conditions:

1. Global and LP-scope initialization has been done:
  - 1.1. TDH.SYS.INIT has been executed.
  - 1.2. TDH.SYS.LP.INIT has been executed on the current LP.
2. The number of bytes provided for returning TDSYSINFO\_STRUCT (in RDX) must be at least the size of that structure.
- 20 3. The number of entries provided for returning CMR\_INFO\_ARRAY (in R9) must be at least the actual number of CMRs.

If successful, the function does the following:

4. Write the TDSYSINFO\_STRUCT, and set RDX to the actual number of bytes written.

5. Write the `CMR_INFO_ARRAY` based on the CMR information in `SEAMCFG`, and set `R9` to the actual number of CMRs.

#### Completion Status Codes

**Table 20.129: TDH.SYS.INFO Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
<code>TDX_OPERAND_INVALID</code>	
<code>TDX_SUCCESS</code>	TDH.SYS.INFO is successful.
<code>TDX_SYS_SHUTDOWN</code>	
<code>TDX_SYSINITLP_NOT_DONE</code>	

### 20.2.33. TDH.SYS.INIT Leaf

Globally initialize the Intel TDX module.

**Table 20.130: TDH.SYS.INIT Input Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction leaf number – see 20.2.1		
RCX	Intel TDX module attributes		
	Bits	Name	Description
	0	SYSPROF	Indicates system profiling mode where the host VMM can monitor the guest TDs using Perfmon counters
	63:1	RESERVED	Reserved: must be 0

5

**Table 20.131: TDH.SYS.INIT Output Operands Definition**

Operand	Description		
RAX	SEAMCALL instruction return code – see 20.2.1		
RCX	Extended error information part 1 In case of an incorrect CPUID value, RCX returns the applicable CPUID information as shown below. In all other cases, RCX returns 0.		
	Bits	Name	Description
	31:0	LEAF	CPUID leaf number
	63:32	SUBLEAF	CPUID sub-leaf number: if sub-leaf is not applicable, value is -1 (0xFFFFFFFF).
RDX	Extended error information part 2 In case of an incorrect CPUID value, RDX returns the value masks as shown below. A bit value of 1 indicates a bit position that was checked against the required value. In all other cases, RDX returns 0.		
	Bits	Name	Description
	31:0	MASK_EAX	Mask of the value returned by CPUID in EAX
	63:32	MASK_EBX	Mask of the value returned by CPUID in EBX
R8	Extended error information part 3 In case of an incorrect CPUID value, R8 returns the value masks as shown below. A bit value of 1 indicates a bit position that was checked against the required value. In all other cases, R8 returns 0.		
	Bits	Name	Description
	31:0	MASK_ECX	Mask of the value returned by CPUID in ECX
	63:32	MASK_EDX	Mask of the value returned by CPUID in EDX
R9	Extended error information part 4 In case of an incorrect CPUID value, R9 returns the expected values as shown below. In all other cases, R9 returns 0.		

	Bits	Name	Description
	31:0	VALUE_EAX	Value expected to be returned by CPUID in EAX
	63:32	VALUE_EBX	Value expected to be returned by CPUID in EBX
R10	Extended error information part 5 In case of an incorrect CPUID value, R10 returns the expected values as shown below. In all other cases, R10 returns 0.		
	Bits	Name	Description
	31:0	VALUE_ECX	Value expected to be returned by CPUID in ECX
	63:32	VALUE_EDX	Value expected to be returned by CPUID in EDX
Other	Unmodified		

### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 5 TDH.SYS.INIT performs global (platform-scope) initialization of the Intel TDX module. This function is intended to be executed during OS/VMM boot and thus it has relaxed latency requirements.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.132: TDH.SYS.INIT Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Implicit	N/A	N/A	All Intel TDX module internal variables	N/A	RW	Hidden	N/A	Exclusive	N/A	N/A

10

In addition to the memory operand checks per the table above, the function checks the following conditions:

1. Check that PL.SYS\_STATE is SYSINIT\_PENDING.
2. Do any global Intel TDX module initializations required for running this flow.
3. Check the memory operands per the table above.
- 15 4. Check the following conditions (no specific order is implied):
  - Enumerate CPU and platform information, and check Intel TDX module compatibility. If the Intel TDX module is compatible with multiple variants of CPU and platform features, sample the current LP's features enumeration – to be later checked to be the same on all LPs by TDH.SYS.LP.INIT. Examples of compatibility checks are:
    - The CPU must support any ISA that the Intel TDX module relies upon, such as SHA-NI.
    - The CPU must support the WBINVD scope for which the Intel TDX module was built.
  - 20 • Sample and check the platform configuration on the current LP – to be later checked to be the same on all LPs by TDH.SYS.LP.INIT. For example:
    - Sample SMRR and SMRR2, check they are locked and do not overlap any CMR, and store their values to be checked later on each LP.
- 25 If successful, the function does the following:
  5. Complete the initialization of the Intel TDX module at platform scope.
  6. Set PL.SYS\_STATE to SYSINIT\_DONE.

## Completion Status Codes

Table 20.133: TDH.SYS.INIT Completion Status Codes (Returned in RAX) Definition

Completion Status Code	Description
TDX_BOOT_NT4_SET	
TDX_CPUID_LEAF_1F_FORMAT_UNRECOGNIZED	
TDX_CPUID_LEAF_1F_NOT_SUPPORTED	
TDX_CPUID_LEAF_0D_INCONSISTENT	
TDX_INCORRECT_CPUID_VALUE	
TDX_INCORRECT_MSR_VALUE	
TDX_INVALID_WBINVD_SCOPE	
TDX_SMRR_LOCK_NOT_SUPPORTED	
TDX_SMRR_NOT_LOCKED	
TDX_SMRR_NOT_SUPPORTED	
TDX_SMRR_OVERLAPS_CMR	
TDX_SUCCESS	TDH.SYS.INIT is successful.
TDX_SYS_BUSY	
TDX_SYS_SHUTDOWN	
TDX_SYSINIT_NOT_PENDING	

### 20.2.34. TDH.SYS.KEY.CONFIG Leaf

Configure the Intel TDX global private key on the current package.

**Table 20.134: TDH.SYS.KEY.CONFIG Input Operands Definition**

Operand	In/Out	Description
RAX	In	SEAMCALL instruction leaf number – see 20.2.1

5

**Table 20.135: TDH.SYS.KEY.CONFIG Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

10 TDH.SYS.KEY.CONFIG performs package-scope Intel TDX global private key configuration.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.136: TDH.SYS.KEY.CONFIG Operands Information**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Implicit	N/A	N/A	All Intel TDX module internal variables	N/A	RW	Hidden	N/A	Exclusive	N/A	N/A

15 In addition to the memory operand checks per the table above, the function checks the following conditions:

1. Check that TDH.SYS.CONFIG has completed successfully (PL.SYS\_STATE is SYSCONFIG\_DONE).

If successful, the function does the following:

2. Do the following as an atomic operation (e.g., LOCK BTS) on PL.PKG\_CONFIG\_BITMAP:
  - 2.1. Check the package has not yet been configured.
  - 2.2. Mark it as configured.
3. Execute PCONFIG to configure the Intel TDX global private HKID on the package with a CPU-generated random key.

20

PCONFIG may fail due to an entropy error or a device busy error. In these cases, the VMM should retry TDH.SYS.KEY.CONFIG.

If successful:

4. If this was the last package on which TDH.SYS.KEY.CONFIG has executed, set PL.STATE to SYS\_READY.

25

#### Completion Status Codes

**Table 20.137: TDH.SYS.KEY.CONFIG Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_KEY_CONFIGURED	

Completion Status Code	Description
TDX_KEY_GENERATION_FAILED	
TDX_OPERAND_BUSY	
TDX_SUCCESS	TDH.SYS.KEY.CONFIG is successful.
TDX_SYS_BUSY	
TDX_SYS_SHUTDOWN	
TDX_SYSINIT_NOT_DONE	

### 20.2.35. TDH.SYS.LP.INIT Leaf

Initialize the Intel TDX module at the current logical processor scope.

**Table 20.138: TDH.SYS.LP.INIT Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1

5

**Table 20.139: TDH.SYS.LP.INIT Output Operands Definition**

Operand	Description									
RAX	SEAMCALL instruction return code – see 20.2.1									
RCX	Extended error information part 1 In case of an inconsistent CPUID field error, RCX returns the applicable CPUID information as shown below. In all other cases, RCX returns 0.									
	<table border="1"> <thead> <tr> <th>Bits</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>31:0</td> <td>LEAF</td> <td>CPUID leaf number</td> </tr> <tr> <td>63:32</td> <td>SUBLEAF</td> <td>CPUID sub-leaf number: if sub-leaf is not applicable, value is -1 (0xFFFFFFFF).</td> </tr> </tbody> </table>	Bits	Name	Description	31:0	LEAF	CPUID leaf number	63:32	SUBLEAF	CPUID sub-leaf number: if sub-leaf is not applicable, value is -1 (0xFFFFFFFF).
	Bits	Name	Description							
31:0	LEAF	CPUID leaf number								
63:32	SUBLEAF	CPUID sub-leaf number: if sub-leaf is not applicable, value is -1 (0xFFFFFFFF).								
63:32	SUBLEAF	CPUID sub-leaf number: if sub-leaf is not applicable, value is -1 (0xFFFFFFFF).								
RDX	Extended error information part 2 In case of an inconsistent CPUID field error, RDX returns the value masks as shown below. A bit value of 1 indicates a bit position that was checked against the same CPUID leaf value checked during TDH.SYS.INIT. In all other cases, RDX returns 0.									
	<table border="1"> <thead> <tr> <th>Bits</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>31:0</td> <td>MASK_EAX</td> <td>Mask of the value returned by CPUID in EAX</td> </tr> <tr> <td>63:32</td> <td>MASK_EBX</td> <td>Mask of the value returned by CPUID in EBX</td> </tr> </tbody> </table>	Bits	Name	Description	31:0	MASK_EAX	Mask of the value returned by CPUID in EAX	63:32	MASK_EBX	Mask of the value returned by CPUID in EBX
	Bits	Name	Description							
31:0	MASK_EAX	Mask of the value returned by CPUID in EAX								
63:32	MASK_EBX	Mask of the value returned by CPUID in EBX								
63:32	MASK_EBX	Mask of the value returned by CPUID in EBX								
R8	Extended error information part 3 In case of an inconsistent CPUID field error, R8 returns the value masks as shown below. A bit value of 1 indicates a bit position that was checked against the same CPUID leaf value checked during TDH.SYS.INIT. In all other cases, R8 returns 0.									
	<table border="1"> <thead> <tr> <th>Bits</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>31:0</td> <td>MASK_ECX</td> <td>Mask of the value returned by CPUID in ECX</td> </tr> <tr> <td>63:32</td> <td>MASK_EDX</td> <td>Mask of the value returned by CPUID in EDX</td> </tr> </tbody> </table>	Bits	Name	Description	31:0	MASK_ECX	Mask of the value returned by CPUID in ECX	63:32	MASK_EDX	Mask of the value returned by CPUID in EDX
	Bits	Name	Description							
31:0	MASK_ECX	Mask of the value returned by CPUID in ECX								
63:32	MASK_EDX	Mask of the value returned by CPUID in EDX								
63:32	MASK_EDX	Mask of the value returned by CPUID in EDX								
Other	Unmodified									

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.SYS.LP.INIT performs LP-scope initialization of the Intel TDX module. This function is intended to be executed during OS/VMM boot, and thus it has relaxed latency requirements.



To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.140: TDH.SYS.LP.INIT Operands Information**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Implicit	N/A	N/A	All Intel TDX module internal variables	N/A	RW	Hidden	N/A	Shared	N/A	N/A

5 In addition to the memory operand checks per the table above, the function checks the following conditions:

1. TDH.SYS.INIT has completed successfully (PL.SYS\_STATE is SYSINIT\_DONE).
2. This is the first invocation of TDH.SYS.LP.INIT on the current LP.

If successful, the function does the following:

3. Do a global EPT flush (INVEPT type 2).
- 10 4. Initialize the Intel TDX module's LP-scope variables.
5. Check the compatibility and uniformity of features and configuration. Once per LP, core or package, depending on the scope of the checked feature or configuration:
  - 15 5.1. Check features compatibility with the Intel TDX module. For example, the WBINVD scope must be the same as the scope the Intel TDX module was built to handle. In cases where the Intel TDX module supports several options, check that the features on the current LP are the same as sampled during TDH.SYS.INIT.
  - 5.2. Check configuration uniformity. For example, the SMRR and SMRR2 must be locked and configured in the same way as sampled during TDH.SYS.INIT.
6. Mark the current LP as initialized.

### Completion Status Codes

**Table 20.141: TDH.SYS.LP.INIT Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_INCONSISTENT_CPUID_FIELD	
TDX_INCONSISTENT_MSR	
TDX_INCORRECT_MSR_VALUE	
TDX_INVALID_PKG_ID	
TDX_SUCCESS	TDH.SYS.LP.INIT is successful.
TDX_SYS_BUSY	
TDX_SYS_SHUTDOWN	
TDX_SYSINIT_NOT_DONE	
TDX_SYSINITLP_DONE	

### 20.2.36. TDH.SYS.LP.SHUTDOWN Leaf

Initiate Intel TDX module shutdown, and prevent further SEAMCALLs on the current logical processor.

Table 20.142: TDH.SYS.SHUTDOWNLP Input Operands Definition

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1

Table 20.143: TDH.SYS.LP.SHUTDOWN Output Operands Definition

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

## 5 Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

TDH.SYS.SHUTDOWNLP marks the Intel TDX module as being shut down (if not already in this state) and prevents further SEAMCALLs on the current LP.

- 10 To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

Table 20.144: TDH.SYS.LP.SHUTDOWN Operands Information

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Implicit	N/A	N/A	All Intel TDX module internal variables	N/A	RW	Hidden	N/A	Shared	N/A	N/A

In addition to the memory operand checks per the table above, the function checks the following conditions:

- 15
1. Mark the Intel TDX module as being shut down by setting PL.SYS\_STATE to SYS\_SHUTDOWN.
  2. Prevent further SEAMCALLs on the current LP by setting the SEAM VMCS's HOST RIP field to the value of SYS\_INFO\_TABLE.SHUTDOWN\_HOST\_RIP (originally configured by the SEAMLDR).
  3. Do a global EPT flush (INVEPT type 2).
    - 3.1. This is a defense-in-depth. In case of an Intel TDX module update, TDH.SYS.LP.INIT will do a global EPT flush.

## 20 Completion Status Codes

Table 20.145: TDH.SYS.LP.SHUTDOWN Completion Status Codes (Returned in RAX) Definition

Completion Status Code	Description
TDX_SUCCESS	TDH.SYS.LP.SHUTDOWN is successful.
TDX_SYS_BUSY	
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	

### 20.2.37. TDH.SYS.TDMR.INIT Leaf

Partially initialize a Trust Domain Memory Region (TDMR) and its associated PAMT.

**Table 20.146: TDH.SYS.TDMR.INIT Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical base address of a TDMR

5

**Table 20.147: TDH.SYS.TDMR.INIT Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
RDX	On successful completion, RDX returns the TDMR next-to-initialize address. This is the physical address of the last byte that has been initialized so far, rounded down to 1GB. In all other cases, RDX returns 0.
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.SYS.TDMR.INIT partially initializes the metadata (PAMT) associated with a Trust Domain Memory Region (TDMR), while adhering to latency considerations. It can run concurrently on multiple LPs as long as each concurrent flow initializes a different TDMR. After each 1GB range of a TDMR has been initialized, that 1GB range becomes available for use by any Intel TDX function that creates a private TD page or a control structure page – e.g., TDH.MEM.PAGE.ADD, TDH.VP.ADDCX, etc.
- 15 To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.148: TDH.SYS.TDMR.INIT Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDMR	Blob	None	None	1GB	Exclusive	N/A	N/A
Implicit	N/A	HPA	PAMT region associated with TDMR	Blob	RW	Hidden	N/A	Exclusive	N/A	N/A

In addition to the memory operand checks per the table above, the function checks the following conditions:

- 20
1. The provided TDMR start address belongs to one of the TDMRs set during TDH.SYS.INIT.
  2. The TDMR has not been completely initialized yet.

If successful, the function does the following:

3. If the TDMR has been completely initialized, there is nothing to do.

Else, the function does the following:

4. Initialize the next implementation defined un-initialized number of PAMT entries. The maximum number of PAMT entries to be initialized is set to help avoid latency issues.
  - 4.1. PAMT\_4K entries associated with a physical address that is within a reserved range are marked with PT\_RSVD.
  - 4.2. Other PAMT\_4K entries are marked with PT\_NDA.
  - 4.3. PAMT\_2M and PAMT\_1G entries are marked with PT\_NDA.
5. If the PAMT for a 1GB block of TDMR has been fully initialized, mark that 1GB block as ready for use. This means that 4KB pages in this 1GB block may be converted to private pages – e.g., by SEAMCALL(TDH.MEM.PAGE.ADD). This can be done concurrently with initializing other TDMRs.
- 10 6. Return the next-to-initialize address rounded down to 1GB. This is done so the host VMM will not attempt to use a 1GB block that is not fully initialized.

### Completion Status Codes

**Table 20.149: TDH.SYS.TDMR.INIT Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_SUCCESS	TDH.SYS.TDMR.INIT is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TDMR_ALREADY_INITIALIZED	

**20.2.38. TDH.VP.ADDCX Leaf**

Add a TDVPX page to memory as a child of a given TDVPR.

**Table 20.150: TDH.VP.ADDCX Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a page where the TDVPX page will be added
RDX	The physical address of a TDVPR page

5 **Table 20.151: TDH.VP.ADDCX Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

**Leaf Function Description**

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.VP.ADDCX adds a TDVPX page as a child of a given TDVPR.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.152: TDH.VP.ADDCX Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDVPX page	Blob	RW	Opaque	4KB	Exclusive	Shared	Shared
Explicit	RDX	HPA	TDVPR page	Blob	RW	Opaque	4KB	Exclusive	Shared	Shared
Implicit	N/A	HPA	TDR page	TDR	RW	Opaque	N/A	Shared	None	None
Implicit	N/A	N/A	TDCS structure	TDCS	R	Opaque	N/A	Exclusive(i)	N/A	N/A

- 15 In addition to the explicit memory operand checks per the table above, the function checks the following conditions:

1. The TDVPR page metadata in PAMT must be correct (PT must be PT\_TDVPR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
4. The TD has been initialized (by TDH.MNG.INIT).
5. The TD build and measurement must not have been finalized (by TDH.MR.FINALIZE).
6. The TD VCPU has not been initialized (by TDH.VP.INIT) and is not being torn down (TDVPS.STATE is VCPU\_UNINITIALIZED).
7. The new TDVPX page metadata in PAMT must be correct (PT must be PT\_NDA).
8. The maximum number of TDVPX pages per TD VCPUs (as enumerated by TDH.SYS.INFO) has not been exceeded.

- 25 If successful, the instruction does the following:

9. Zero out the TDVPX page contents using direct writes (MOVDIR64B).
10. Increment the VCPU's TDVPX counter, and set a pointer in the parent TDVPR page to the new TDVPX page.

11. Increment TDR.CHLDCNT.
12. Initialize the TDVPX page metadata in PAMT.

### Completion Status Codes

**Table 20.153: TDH.VP.ADDCX Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.VP.ADDCX is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_FINALIZED	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_INITIALIZED	
TDX_TDVPX_NUM_INCORRECT	
TDX_VCPU_STATE_INCORRECT	

5

### 20.2.39. TDH.VP.CREATE Leaf

Create a guest TD VCPU and its root TDVPR page.

**Table 20.154: TDH.VP.CREATE Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a page where TDVPR will be added
RDX	The physical address of the owner TDR page

5

**Table 20.155: TDH.VP.CREATE Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.VP.CREATE begins the build of a new guest TD VCPU. It adds a TDVPR page as a child of a TDR page.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.156: TDH.VP.CREATE Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDVPR page	Blob	RW	Opaque	4KB	Exclusive	Shared	Shared
Explicit	RDX	HPA	TDR page	TDR	RW	Opaque	4KB	Shared	Shared	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	R	Opaque	4KB	Shared(i)	N/A	N/A

- 15 In addition to the explicit memory operand checks per the table above, the function checks the following conditions:

1. The TDR page metadata in PAMT must be correct (PT must be PT\_TDR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
4. TDCS must have been initialized (TDR.INIT is TRUE).
- 20 5. The TD build and measurement must not have been finalized (by TDH.MR.FINALIZE).
6. The TDVPR page metadata in PAMT must be correct (PT must be PT\_NDA).

If successful, the instruction does the following:

7. Zero out the TDVPR page contents using direct write (MOVDIR64B).
8. Increment TDR.CHLCNT.
- 25 9. Initialize the TDVPR management fields.
10. Initialize the TDVPR page metadata in PAMT.

**Completion Status Codes****Table 20.157: TDH.VP.CREATE Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.VP.CREATE is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_FINALIZED	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_INITIALIZED	



**20.2.40. TDH.VP.ENTER Leaf**

Enter TDX non-root operation.

From the host VMM's point of view, TDH.VP.ENTER is a complex operation that normally involves TD entry followed by a TD exit. Therefore, input and output operands are specified by multiple tables below.

5

**Table 20.158: TDH.VP.ENTER Input Operands Definition in the Normal Case**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of the TD VCPU's TDVPR page

**Table 20.159: TDH.VP.ENTER Input Operands Definition Following a Previous TDCALL(TDG.VP.VMCALL)**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of the TD VCPU's TDVPR page
RBX, RDX, RBP, RDI, RSI, R8 – R15	If the corresponding bit of RCX at the previous TD exit (i.e., previous TDH.VP.ENTER termination) was set to 1, the register value is passed as-is to the guest TD – see the description of TDG.VP.VMCALL in 20.3.8 for details. Else, the register value is not used as an input.
XMM0 – XMM15	If the corresponding bit of RCX at the previous TD exit (i.e., previous TDH.VP.ENTER termination) was set to 1, the register value is passed as-is to the guest TD – see the description of TDG.VP.VMCALL in 20.3.8 for details. Else, the register value is not used as an input.

**Table 20.160: TDH.VP.ENTER Output Operands Definition on Error (No TD Entry)**

Operand	Description
RAX	SEAMCALL instruction return code – see 15.3.2
Other GPRs	Unmodified
Extended State	Any extended state that the TD is allowed to use (per TDCS.XFAM) may be cleared to its architectural INIT state.

10

**Table 20.161: TDH.VP.ENTER Output Operands Definition on Asynchronous TD Exits Following a TD Entry**

Operand	TD Exit Information	Description
RAX	Status and Exit Reason	SEAMCALL instruction return code – see 15.3.2 Note the special values of the DETAILS_L1 field in bits 39:32 which indicate that the VCPU or the whole TD is corrupt and cannot be re-entered: <ul style="list-style-type: none"> <li>• TDX_NON_RECOVERABLE_VCPU</li> <li>• TDX_NON_RECOVERABLE_TD</li> </ul> The DETAILS_L2 field in bits 31:0 contain the VMCS exit reason: <ul style="list-style-type: none"> <li>• Bit 27 (enclave mode) is not set.</li> <li>• Bit 28 (Pending MTF VM exit) is not set.</li> <li>• Bit 29 (VM exit from VMX root operation) is not set.</li> <li>• Bit 31 (VM-entry failure) is not set.</li> </ul>

Operand	TD Exit Information	Description
RCX	Exit Qualification	Format is similar to the VMCS exit qualification. When exit is due to EPT violation, bits 12-7 of the exit qualification are cleared to 0.
RDX	Extended Exit Qualification	When exit is due to EPT violation of the Secure EPT (GPA.SHARED == 0), then: <ul style="list-style-type: none"> <li>• Bit 0 indicates that EPT violation was due to a TDG.MEM.PAGE.ACCEPT.</li> <li>• Other bits are cleared to 0.</li> </ul> In other cases, RDX is cleared to 0.
R8	Guest Physical Address	When exit is due to EPT violation or EPT misconfiguration, format is similar to the VMCS guest-physical address, except that bits 11:0 are cleared to 0. In other cases, R8 is cleared to 0.
R9	VM-Exit Interruption Information	When exit is due to a vectored event, format of bits 31:0 is similar to the VMCS VM-exit interruption information. Bits 63:32 are cleared to 0. In other cases, R9 is cleared to 0.
RBX, RSI, RDI, R10 – R15	None	Cleared to 0
Extended State	Any extended state that the TD is allowed to use (per TDCS.XFAM) is cleared to its architectural INIT state.	

**Table 20.162: TDH.VP.ENTER Output Operands Definition on TDCALL(TDG.VP.VMCALL) Following a TD Entry**

Operand	Description
RAX	<ul style="list-style-type: none"> <li>• Bits 31:0 format is similar to the VMCS exit reason.</li> <li>• Bits 63:32 are cleared to 0.</li> </ul>
RCX	Value as passed in to TDCALL(TDG.VP.VMCALL) by the guest TD: indicates which part of the guest TD GPR and XMM state is passed as-is to the VMM and back. For details, see the description of TDG.VP.VMCALL in 20.3.8.
RBX, RDX, RBP, RDI, RSI, R8 – R15	If the corresponding bit in RCX is set to 1, the register value is passed as-is from the guest TD's input to TDG.VP.VMCALL. Else, the register value cleared to 0.
XMM0 – XMM15	If the corresponding bit in RCX is set to 1, the register value is passed as-is from the guest TD's input to TDG.VP.VMCALL. Else, the register value cleared to 0.
Extended State except XMM	Any extended state, except XMM, that the TD is allowed to use (per TDCS.XFAM) is cleared to its architectural INIT state.

### Leaf Function Description

- 5 **Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

TDH.VP.ENTER enters TDX non-root operation.

**VCPU Association:** TDH.VP.ENTER associates the target TD VCPU with the current LP. This requires that the VCPU will not be associated with another LP. For details, see 8.3.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.163: TDH.VP.ENTER Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDVPR page	TDVPS	RW	Opaque	4KB	Shared <sup>15</sup>	Shared <sup>15</sup>	Shared <sup>15</sup>
Implicit	N/A	HPA	TDR page	TDR	RW	Opaque	N/A	Shared <sup>15</sup>	N/A	N/A
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Shared(1) <sup>15</sup>	N/A	N/A
Implicit	N/A	N/A	TDCS TLB Tracking Fields	N/A	RW	Opaque	N/A	Shared	N/A	N/A

5 In addition to the explicit memory operand checks per the table above, the function checks the following conditions:

1. The TDVPR page metadata in PAMT must be correct (PT must be PT\_TDVPR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
4. TDCS must have been initialized (TDR.INIT is TRUE).

10 5. The TD build and measurement must have been finalized (by TDH.MR.FINALIZE).

If successful, the function does the following:

6. Associate the VCPU with the current LP and update TD VMCS.
  - 6.1. Check that the VCPU has been initialized and is not being torn down.
  - 6.2. Atomically check that the VCPU is not associated with another LP, and associate it with the current LP.
  - 6.3. If the TD's ephemeral HKID has changed since last VM entry, update all TD VMCS physical pointers and the TD HKID execution control.
  - 6.4. Update the TD VMCS host state fields with any Intel TDX module LP-specific values.

15

If passed:

7. If the TD VCPU to be entered is different than the last TD VCPU entered on the current LP, issue an indirect branch prediction barrier command to the CPU by writing to the IA32\_PRED\_CMD MSR with the IBPB bit set.
8. Update the TLB tracking state. This is done as a critical section allowing concurrent TDH.VP.ENTERS but no concurrent TDH.MEM.TRACK. A concurrent TDH.MEM.TRACK may cause this locking to fail; in this case, the caller is expected to retry TDH.VP.ENTER.
  - 8.1. Lock the TDCS epoch tracking fields in shared mode.
  - 8.2. Sample the TD's epoch counter (TDCS.TD\_EPOCH) into the VCPU's TDVPS.VCPU\_EPOCH.
  - 8.3. Atomically increment the TD's REFCOUNT that is associated with the sampled epoch (TDCS.REFCOUNT[TD\_EPOCH % 2]).
  - 8.4. Release the shared mode locking of the epoch tracking fields.

25

If successful:

9. Set TDVPS.VCPU\_STATE to VCPU\_ACTIVE.
10. Restore guest TD state:
  - 10.1. If previous TD exit was due to a TDG.VP.VMCALL:
    - 10.1.1. Restore guest XMM and GPR state that is not passed as-is from the host VMM, as controlled by the value of guest TD RCX input to TDG.VP.VMCALL.
    - 10.1.2. Set guest RAX to 0.
  - 10.2. Else (TD exit was an asynchronous exit):
    - 10.2.1. Restore CPU extended state from TDVPS (per TDCS.XFAM).
  - 10.3. Restore other guest state from TDVPS.

35

<sup>15</sup> The shared locking of TDVPS, TDR and TDCS (but not the TDCS epoch tracking fields) is for the whole duration of running in TDX non-root mode; the locks are released on TD exit.

11. Execute VMLAUNCH or VMRESUME depending on whether this VCPU has been launched on this LP since its last association with the LP (TVPS.VMLAUNCH).

**Note:** Logically, from the point of view of the host VMM, a successful TDH.VP.ENTER is terminated by the next TD exit.

### Completion Status Codes

- 5 In case of successful execution (which resulted in the TD guest running and then exiting), the status code value in RAX is encoded the same as the VMX Exit reason – see 15.3.2 for details.

**Table 20.164: TDH.VP.ENTER Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_NON_RECOVERABLE_TD	TDH.VP.ENTER launched or resumed TD VCPU operation (TDX non-root mode) – followed later by a TD exit. The TD state is non-recoverable – further TD entry is prohibited. Exit reason is in RAX bits 31:0.
TDX_NON_RECOVERABLE_VCPU	TDH.VP.ENTER launched or resumed TD VCPU operation (TDX non-root mode) – followed later by a TD exit. The TD VCPU state is non-recoverable – further TD entry to this VCPU is prohibited. Exit reason is in RAX bits 31:0.
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	Note the special case where the indicated operand is TLB_EPOCH. This may happen due to a conflict with TDH.MEM.TRACK. The host VMM may retry TDH.VP.ENTER.
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.VP.ENTER launched or resumed TD VCPU operation (TDX non-root mode) – followed later by a TD exit. Exit reason is in RAX bits 31:0.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_FINALIZED	
TDX_TD_NOT_INITIALIZED	
TDX_VCPU_ASSOCIATED	
TDX_VCPU_STATE_INCORRECT	

**20.2.41. TDH.VP.FLUSH Leaf**

Flush the address translation caches and cached TD VMCS associated with a TD VCPU on the current logical processor.

**Table 20.165: TDH.VP.FLUSH Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a TDVPR page

5

**Table 20.166: TDH.VP.FLUSH Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

**Leaf Function Description**

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.VP.FLUSH flushes the address translation caches and cached TD VMCS associated with a TD VCPU on the current LP. It then marks the VCPU as not associated with any LP.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.167: TDH.VP.FLUSH Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDVPR page	TDVPS	RW	Opaque	4KB	Exclusive	Shared	Shared
Implicit	N/A	HPA	TDR page	TDR	R	Opaque	N/A	Shared	N/A	N/A
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Shared(i)	N/A	N/A

15

In addition to the memory operand checks per the table above, the function checks the following:

1. The TDVPR page metadata in PAMT must be correct (PT must be PT\_TDVPR).
2. The TD keys are configured on the hardware, and the TD's HKID has not been freed yet (TDR.KEY\_STATE is either TD\_KEYS\_CONFIGURED or TD\_BLOCKED).
- 20 3. The current VCPU must be currently associated with the current LP.

If the above checks pass, the function does the following:

4. Flush the TLB context and extended paging structure (EPxE) caches associated with the TD using INVEPT single-context invalidation (type 1).
5. Flush the cached TD VMCS content to TDVPS using VMCLEAR.
- 25 6. Mark the current VCPU as not associated with any LP.
7. Atomically decrement (using LOCK XADD) the associated VCPUs counter (TDCS.NUM\_ASSOC\_VCPUS).

**Completion Status Codes****Table 20.168: TDH.VP.FLUSH Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_KEY_STATE_INCORRECT	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.VP.FLUSH is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_VCPU_NOT_ASSOCIATED	

## 20.2.42. TDH.VP.INIT Leaf

Initialize the saved state of a TD VCPU.

### Operands

**Table 20.169: TDH.VP.INIT Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a TDVPR page
RDX	Initial value of the guest TD VCPU RCX

5

**Table 20.170: TDH.VP.INIT Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
Other	Unmodified

### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

TDH.VP.INIT initialized the saved state of a VCPU in the TDVPR and TDPX pages.

**VCPU Association:** TDH.VP.INIT associates the target TD VCPU with the current LP – for details, see 8.3.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

15

**Table 20.171: TDH.VP.INIT Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDVPR page	TDVPS	RW	Opaque	4KB	Exclusive	Shared	Shared
Implicit	N/A	HPA	TDR page	TDR	R	Opaque	4KB	Shared	N/A	N/A
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	4KB	Shared(i)	N/A	N/A

In addition to the memory operand checks per the table above, the function checks the following:

1. The TDVPR page metadata in PAMT must be correct (PT must be PT\_TDVPR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
4. The TD build and measurement must not have been finalized (by TDH.MR.FINALIZE).
5. The TD VCPU has not been initialized (by TDH.VP.INIT) and is not being torn down (TDVPS.STATE is VCPU\_UNINITIALIZED).
6. The number of TDPX pages associated with the TDVPR page is correct.
7. Atomically Increment the TD's VCPU counter (TDCS.NUM\_VCPUS), and check that maximum number of VCPUS (TDCS.MAX\_VCPUS) has not been exceeded.

20

25

If successful, the function does the following:

8. Assign a unique sequential identifier to the VCPU.
9. Initialize the VCPU state fields in the logical TDVPS structure (TDVPR and TDVPX pages).
10. Set the VCPU state VCPU\_READY\_ASYNC since the first TD entry is the same as TD entry following an asynchronous TD exit.

5

### Completion Status Codes

**Table 20.172: TDH.VP.INIT Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_MAX_VCPUS_EXCEEDED	
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.VP.INIT is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_FINALIZED	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TDVPX_NUM_INCORRECT	
TDX_VCPU_ASSOCIATED	
TDX_VCPU_STATE_INCORRECT	
TDX_VCPU_STATE_INCORRECT	



**20.2.43. TDH.VP.RD Leaf**

Read a TDVPS field.

**Table 20.173: TDH.VP.RD Input Operands Definition**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a TDVPR page
RDX	Field code – see 18.7.3

5

**Table 20.174: TDH.VP.RD Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
R8	Field content
Other	Unmodified

**Leaf Function Description**

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.VP.RD reads a TDVPS field, given its field code. Reading is subject to the field's readability (per the TD's ATTRIBUTES.DEBUG bit).

**VCPU Association:** TDH.VP.RD associates the target TD VCPU with the current LP. This requires that the VCPU will not be associated with another LP – for details, see 8.3.

- 15 To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.175: TDH.VP.RD Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDVPR page	TDVPS	RW	Opaque	4KB	Shared	Shared	Shared
Implicit	N/A	HPA	TDR page	TDR	R	Opaque	N/A	Shared	N/A	N/A
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Shared(i)	N/A	N/A

In addition to the memory operand checks per the table above, the function checks the following:

- 20
1. The TDVPR page metadata in PAMT must be correct (PT must be PT\_TDVPR).
  2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
  3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).
  4. The TD has been initialized (by TDH.MNG.INIT).

5. The provided field code is valid.
6. The provided TDVPS field is readable per the TD's debug attribute (TDCS.ATTRIBUTES.DEBUG).

If successful, the function does the following:

7. Associate the VCPU with the current LP, and update TD VMCS.
  - 7.1. Check that the VCPU has been initialized and is not being torn down.
  - 7.2. Atomically check that the VCPU is not associated with another LP, and associate it with the current LP.
  - 7.3. If the TD's ephemeral HKID has changed since last VM entry, update all TD VMCS physical pointers and the TD HKID execution control.
  - 7.4. Update the TD VMCS host state fields with any Intel TDX module LP-specific values.

10 If passed:

8. Derive the field attributes (read mask, VMCS field code or offset in TDVPS) from the field code provided in RDX per the TD's ATTRIBUTE.DEBUG. If the read mask is 0, then fail; the field is not readable.

If passed:

9. Read the field value (VMREAD from TD VMCS, directly from other TDVPS areas).
- 15 10. Mask out the field value with the read mask derived earlier and return in R8.

### Completion Status Codes

**Table 20.176: TDH.VP.RD Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	
TDX_SUCCESS	TDH.VP.RD is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_INITIALIZED	
TDX_VCPU_ASSOCIATED	
TDX_VCPU_STATE_INCORRECT	

**20.2.44. TDH.VP.WR Leaf**

Write a TDVPS field.

**Table 20.177: TDH.VP.WR Operands**

Operand	Description
RAX	SEAMCALL instruction leaf number – see 20.2.1
RCX	The physical address of a TDVPR page
RDX	Field code – see 18.7.3
R8	64b value to write to the field
R9	64b mask to indicate which bits of the value in R8 are to be written to the field

5

**Table 20.178: TDH.VP.WR Output Operands Definition**

Operand	Description
RAX	SEAMCALL instruction return code – see 20.2.1
R8	Previous content of the field
Other	Unmodified

**Leaf Function Description**

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDH.VP.WR writes a TDVPS field, given its field code. The specific bits of the value (R8) are written as specified by the write mask (R9). Writing is subject to the field's writability (per the TD's ATTRIBUTES.DEBUG bit). Writing of specific fields is also subject to additional rules as detailed in 19.2.

TDH.VP.WR returns the previous content of the field masked by the field's readability (per the TD's ATTRIBUTES.DEBUG bit).

- 15 **VCPU Association:** TDH.VP.WR associates the target TD VCPU with the current LP. This requires that the VCPU will not be associated with another LP – for details, see 8.3.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.179: TDH.VP.WR Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions		
								Operand	Contain. 2MB	Contain. 1GB
Explicit	RCX	HPA	TDVPR page	TDVPS	RW	Opaque	4KB	Shared	Shared	Shared
Implicit	N/A	HPA	TDR page	TDR	R	Opaque	N/A	Shared	N/A	N/A
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Shared(i)	N/A	N/A

20

In addition to the memory operand checks per the table above, the function checks the following:

1. The TDVPR page metadata in PAMT must be correct (PT must be PT\_TDVPR).
2. The TD is not in a FATAL state (TDR.FATAL is FALSE).
3. The TD keys are configured on the hardware (TDR.KEY\_STATE is TD\_KEYS\_CONFIGURED).

4. TDCS must have been initialized (TDR.INIT is TRUE).
5. The provided field code is valid.
6. The provided TDVPS field is writable per the TD's debug attribute (TDCS.ATTRIBUTES.DEBUG).

If successful, the function does the following:

- 5 7. Associate the VCPU with the current LP and update TD VMCS.
  - 7.1. Check that the VCPU has been initialized and is not being torn down.
  - 7.2. Atomically check that the VCPU is not associated with another LP, and associate it with the current LP.
  - 7.3. If the TD's ephemeral HKID has changed since last VM entry, update all TD VMCS physical pointers and the TD HKID execution control.
  - 10 7.4. Update the TD VMCS host state fields with any Intel TDX module LP-specific values.

If passed:

8. Derive the field attributes (read mask, write mask, VMCS field code or offset in TDVPS) from the field code provided in RDX per the TD's ATTRIBUTE.DEBUG.

If passed:

- 15 9. Derive the effective write mask by bitwise-anding the write mask derived above with the write mask provided in R9. If the effective write mask is 0, then fail; the field is not writable.

If passed:

10. Read the field value. For a TD VMCS field, use VMREAD. For other fields, read directly from the TDVPS.
11. Update the field value from the input value in R8, per the effective write mask, and write the field (use VMWRITE to write TD VMCS, write directly to other TDVPS areas).
  - 11.1. Writes of some fields are subject to rules, as detailed per field in 19.2 – e.g., the value of fields that contain Shared physical address, such as the Shared EPT Pointer, must have a Shared HKID value and must comply with some alignment rules.
  - 25 11.2. In most cases, writes of guest state fields are subject to the same rules as if the write is done by the guest itself – e.g., writing to guest CR4 is subject to the rules described in 9.5.2. If the write operation is illegal, TDH.VP.WR fails and returns a proper error code.
  - 30 11.3. In debug mode (ATTRIBUTES.DEBUG == 1), there are some TDVPS fields where the TDH.VP.WR does not check whether the written values are architecturally valid. It is the responsibility of the host VMM, and failing to do so will later cause a VM entry failure leading to a fatal shutdown of the Intel TDX module. The security of any guest TD is not impacted.
  - 35 11.4. In other cases, in debug mode (ATTRIBUTES.DEBUG == 1), TDH.VP.WR allows setting of TDVPS fields to values that may impact the correct operation of the TD under debug. It is the responsibility of the host VMM to take this into consideration.
    - TDH.VP.WR is allowed to enable BTM by setting guest IA32\_DEBUGCTL[7:6] to 0x1 (see 13.1.3).
    - TDH.VP.WR is allowed to modify the state of IA32\_DEBUGCTL[13] (ENABLE\_UNCORE\_PMI) (see 13.1.2.2).
    - TDH.VP.WR is allowed to enable VM exits on exceptions other than MCE by setting the TD VMCS exception bitmap execution control. The Intel TDX module does not take this into account when handling VM exits that occur during event delivery.

If passed:

- 40 12. Mask out the previous field value with the read mask derived earlier, and return in R8.

## Completion Status Codes

**Table 20.180: TDH.VP.WR Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_ADDR_RANGE_ERROR	
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_OPERAND_PAGE_METADATA_INCORRECT	

Completion Status Code	Description
TDX_SUCCESS	TDH.VP.WR is successful.
TDX_SYS_NOT_READY	
TDX_SYS_SHUTDOWN	
TDX_TD_FATAL	
TDX_TD_KEYS_NOT_CONFIGURED	
TDX_TD_NOT_INITIALIZED	
TDX_TD_VMCS_FIELD_NOT_INITIALIZED	
TDX_TDVPS_FIELD_NOT_WRITABLE	
TDX_VCPU_ASSOCIATED	
TDX_VCPU_STATE_INCORRECT	
TO BE COMPLETED	

### 20.3. Guest-Side (TDCALL) Interface Functions

The TDCALL instruction causes a VM exit to the Intel TDX module. It is used to call guest-side Intel TDX functions, either local or a TD exit to the host VMM, as selected by RAX.

#### 20.3.1. TDCALL Instruction (Common)

- 5 This section describes the common functionality of TDCALL. Leaf functions are described in the following sections. As used by the Intel TDX module, TDCALL is allowed only in 64b mode.

**Table 20.181: TDCALL Input Operands Definition**

Operand	Description
RAX	Leaf number – see Table 20.183 below.
Other	See individual TDCALL leaf functions.

**Table 20.182: TDCALL Output Operands Definition**

Operand	Description
RAX	Instruction return code, indicating the outcome of execution of the instruction – see 15.3.2 for details.
Other	See individual TDCALL leaf functions.

10

**Table 20.183: TDCALL Instruction Leaf Numbers Definition**

Leaf Number	Interface Function Name
0	TDG.VP.VMCALL
1	TDG.VP.INFO
2	TDG.MR.RTMR.EXTEND
3	TDG.VP.VEINFO.GET
4	TDG.MR.REPORT
5	TDG.VP.CPUIDVE.SET
6	TDG.MEM.PAGE.ACCEPT

#### Instruction Description

- 15 **Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

This section describes how TDCALL leaf functions are implemented by the Intel TDX module.

On VM exit, the Intel TDX module performs the following checks:

- 20
1. If the CPU mode is not 64b ((IA32\_EFER.LMA == 1) && (CS.L == 1)), the Intel TDX module injects a #GP(0) fault into the guest TD.
  2. If the leaf number in RAX is not supported by the Intel TDX module, it returns a TDX\_OPERAND\_INVALID(0) status code in RAX.

If all checks pass, the Intel TDX module calls the leaf function according to the leaf number in RAX – see the following sections for individual leaf function details.

**Completion Status Codes****Table 20.184: TDCALL Completion Status Codes (Returned in RAX) Definition**

<b>Completion Status Code</b>	<b>Description</b>
TDX_SUCCESS	TDCALL is successful.
TDX_OPERAND_INVALID	Illegal leaf number
Other	See individual leaf functions

### 20.3.2. TDG.MEM.PAGE.ACCEPT Leaf

Accept a pending private page, and initialize the page to all-0 using the TD ephemeral private key.

**Table 20.185: TDG.MEM.PAGE.ACCEPT Input Operands Definition**

Operand	Description
RAX	TDCALL instruction leaf number – see 20.3.1
RCX	Guest physical address of the private page to accept

5

**Table 20.186: TDG.MEM.PAGE.ACCEPT Output Operands Definition**

Operand	Description
RAX	TDCALL instruction return code – see 20.3.1
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 Accept a pending private page, previously added by TDH.MEM.PAGE.AUG, into the TD. Initialize the page to 0.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.187 TDG.MEM.PAGE.ACCEPT Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions
Explicit	RCX	GPA	TD private page	Blob	RW	Private	4KB	None
Implicit	N/A	N/A	TDR page	TDR	None	Opaque	N/A	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	R	Opaque	N/A	Shared(i)
Implicit	N/A	N/A	TDVPS structure	TDVPS	RW	Opaque	N/A	Shared
Implicit	N/A	N/A	Secure EPT tree	N/A	RW	Private	N/A	None

- 15 TDG.MEM.PAGE.ACCEPT checks the memory operands per the table above when applicable during its flow. The text below does not explicitly mention those checks, except when necessary.

The function checks the following conditions:

In addition to the memory operand checks per the table above, the function checks the following conditions (no specific order is implied):

- 20 1. Walk the Secure EPT based on the GPA operand, and locate the leaf EPT entry of the page to be accepted.  
 1.1. If failed, TD exit with an EPT Violation exit reason and TDG.MEM.PAGE.ACCEPT indication in the extended exit qualification – see the TDH.VP.ENTER definition in 20.2.31 for details.

If successful, do the following:

- 25 2. Check that the entry state is SEPT\_PENDING:  
 2.1. If the entry state is SEPT\_BLOCKED or SEPT\_PENDING\_BLOCKED, TD exit with an EPT Violation exit reason and TDG.MEM.PAGE.ACCEPT indication in the extended exit qualification – see the TDH.VP.ENTER definition in 20.2.31 for details.



- 2.2. If the entry state is SEPT\_PRESENT, terminate TDG.MEM.PAGE.ACCEPT with an indication that the page has already been accepted.

If successful, do the following:

3. Initialize the page to 0 using the TD's ephemeral private HKID and direct writes (MOVDIR64B).

- 5 **Note:** TDG.MEM.PAGE.ACCEPT does not protect against the guest TD attempting to accept the same page concurrently on more than one thread. Such an attempt may result in page content corruption but not in an incorrect state.

If successful, do the following:

- 10 4. Atomically (using LOCK CMPXCHG), check that the entry state is still SEPT\_PENDING, and set it to SEPT\_PRESENT. Note that TDG.MEM.PAGE.ACCEPT does not acquire any lock on the Secure EPT, thus a concurrent thread may change the Secure EPT entry state.
- 15 4.1. If it fails because the entry state is SEPT\_BLOCKED or SEPT\_PENDING\_BLOCKED, TD exit with an EPT Violation exit reason and TDG.MEM.PAGE.ACCEPT indication in the extended exit qualification – see the TDH.VP.ENTER definition in 20.2.31 for details.
- 4.2. If it fails because the entry state is SEPT\_PRESENT, terminate TDG.MEM.PAGE.ACCEPT with an indication that the page has already been accepted.

### Completion Status Codes

**Table 20.188: TDG.MEM.PAGE.ACCEPT Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_INVALID	
TDX_PAGE_ALREADY_ACCEPTED	
TDX_SUCCESS	TDG.MEM.PAGE.ACCEPT is successful.

### 20.3.3. TDG.MR.REPORT Leaf

TDG.MR.REPORT creates a TDREPORT\_STRUCT structure that contains the measurements/configuration information of the guest TD that called the function, measurements/configuration information of the Intel TDX module and a REPORTMACSTRUCT.

5

**Table 20.189: TDG.MR.REPORT Input Operands Definition**

Operand	Description		
RAX	TDCALL instruction leaf number – see 20.3.1		
RCX	1024B-aligned guest physical address of newly created report structure		
RDX	64B-aligned guest physical address of additional data to be signed		
R8	Bits	Name	Description
	7:0	Report sub type	Must be 0
	63:8	Reserved	Reserved: must be 0

**Table 20.190: TDG.MR.REPORT Output Operands Definition**

Operand	Description
RAX	TDCALL instruction return code – see 20.3.1
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

This function creates a TDREPORT\_STRUCT structure that contains the measurements/configuration information of the guest TD that called the function, measurements/configuration information of the Intel TDX module and a REPORTMACSTRUCT. The REPORTMACSTRUCT is integrity-protected with a MAC, and it contains the hash of the measurements and configuration as well as additional REPORTDATA provided by the TD software.

Additional REPORTDATA, a 64-byte value, is provided by the guest TD to be included in the TDG.MR.REPORT.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.191: TDG.MR.REPORT Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions
Explicit	RCX	GPA	Output report	TDREPORT_STRUCT	RW	Private/ Shared	1024B	None
Explicit	RDX	GPA	Input report data	REPORTDATA	R	Private/ Shared	64B	None
Implicit	N/A	N/A	TDR page	TDR	None	Opaque	N/A	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	R	Opaque	N/A	Shared(i)
Implicit	N/A	N/A	TDCS.RTMR	SHA384_HASH	N/A	Opaque	N/A	Shared
Implicit	N/A	N/A	TDVPS structure	TDVPS	None	Opaque	N/A	Shared

20

In addition to the memory operand checks per the table above, the function checks the following conditions (no specific order is implied):

1. R8 must specify report sub type 0.

If passed, the function does the following:

- 5 2. Assemble a report type structure based on the report sub type provided in R8.
3. Assemble the output report's TDG.VP.INFO fields from the TDCS reported fields (ATTRIBUTES, XFAM, MRTD, MRCONFIGID, MROWNER, MROWNERCONFIG and RTMRs).
4. Calculate a SHA384 hash over TDG.VP.INFO.
- 10 5. Execute SEAMREPORT to complete the output report, based on the input report data, the TDG.VP.INFO hash calculated above and the report type structure.
6. Write the output report to memory.

### Completion Status Codes

**Table 20.192: TDG.MR.REPORT Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_SUCCESS	TDG.MR.REPORT is successful.

### 20.3.4. TDG.MR.RTMR.EXTEND Leaf

Extend a TDCS.RTMR measurement register.

**Table 20.193: TDG.MR.RTMR.EXTEND Input Operands Definition**

Operand	Description
RAX	TDCALL instruction leaf number – see 20.3.1
RCX	64B-aligned guest physical address of a 48B extension data buffer
RDX	Index of the measurement register to be extended

5

**Table 20.194: TDG.MR.RTMR.EXTEND Output Operands Definition**

Operand	Description
RAX	TDCALL instruction return code – see 20.3.1
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

10 This function extends one of the RTMR measurement registers in TDCS with the provided extension data in memory.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.195 TDG.MR.RTMR.EXTEND Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions
Explicit	RCX	GPA	EXTEND_DATA	Blob	R	Private	64B	None
Implicit	N/A	N/A	TDR page	TDR	None	Opaque	N/A	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	RW	Opaque	N/A	Shared(i)
Implicit	N/A	N/A	TDCS.RTMR	SHA384_HASH	N/A	Opaque	N/A	Exclusive
Implicit	N/A	N/A	TDVPR page	TDVPS	None	Opaque	N/A	Shared

15 In addition to the memory operand checks per the table above, the function checks the following conditions (no specific order is implied):

1. RDX must contain a valid RTMR index.

If successful, the function does the following:

2. Extend the RTMR indexed by RDX with the extension data. Extension is done by calculating SHA384 hash over a 96B buffer, composed as follows:
    - Bytes 0 through 47 contain the current RTMR value.
    - Bytes 48 through 95 contain the extension data.
- 20

**Completion Status Codes****Table 20.196: TDG.MR.RTMR.EXTEND Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_BUSY	
TDX_OPERAND_INVALID	
TDX_SUCCESS	TDG.MR.RTMR.EXTEND is successful.

### 20.3.5. TDG.VP.CPUIDVE.SET Leaf

TDG.VP.CPUIDVE.SET controls unconditional #VE on CPUID execution by the guest TD.

**Table 20.197: TDG.VP.CPUIDVE.SET Input Operands Definition**

Operand	Description		
RAX	TDCALL instruction leaf number – see 20.3.1		
RCX	Controls whether CPUID executed by the guest TD will cause #VE unconditionally		
	Bits	Name	Description
	0	SUPERVISOR	Flags that when CPL is 0, a CPUID executed by the guest TD will cause a #VE unconditionally
	1	USER	Flags that when CPL > 0, a CPUID executed by the guest TD will cause a #VE unconditionally
63:2	RESERVED	Reserved: must be 0	

**Table 20.198: TDG.VP.CPUIDVE.SET Output Operands Definition**

Operand	Description
RAX	TDCALL instruction return code – see 20.3.1
Other	Unmodified

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

This function controls whether execution of CPUID by the guest TD, when running in supervisor mode and/or in user mode, will unconditionally result in a #VE.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.199 TDG.VP.CPUIDVE.SET Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions
Implicit	N/A	N/A	TDR page	TDR	None	Opaque	N/A	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	R	Opaque	N/A	Shared(i)
Implicit	N/A	N/A	TDVPS structure	TDVPS	RW	Opaque	N/A	Shared

In addition to the memory operand checks per the table above, the function checks the following conditions (no specific order is implied):

- Reserved bits of RCX must be 0.

If successful, the function does the following:

- Update the TDVPS.CPUID\_VE flags which control unconditional #VE injection for CPUID for the current VCPU.

**Completion Status Codes****Table 20.200: TDG.VP.CPUIIDVE.SET Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_INVALID	
TDX_SUCCESS	TDG.VP.CPUIIDVE.SET is successful.

### 20.3.6. TDG.VP.INFO Leaf

Get guest TD execution environment information.

**Table 20.201: TDG.VP.INFO Input Operands Definition**

Operand	Description
RAX	TDCALL instruction leaf number – see 20.3.1

5

**Table 20.202: TDG.VP.INFO Output Operands Definition**

Operand	Description		
RAX	TDCALL instruction return code – see 20.3.1 – returns a constant value of TDX_SUCCESS (0)		
RCX	<b>Bits</b>	<b>Name</b>	<b>Description</b>
	5:0	GPAW	The effective GPA width (in bits) for this TD (do not confuse with MAXPA). SHARED bit is at GPA bit GPAW-1. Only GPAW values 48 and 52 are possible.
	63:6	RESERVED	Reserved: 0
RDX	The TD's ATTRIBUTES (provided as input to TDH.MNG.INIT)		
R8	<b>Bits</b>	<b>Name</b>	<b>Description</b>
	31:0	NUM_VCPUS	Number of Virtual CPUs that are usable (i.e. either active or ready) – see 8.4
	63:32	MAX_VCPUS	TD's maximum number of Virtual CPUs (provided as input to TDH.MNG.INIT)
R9	<b>Bits</b>	<b>Name</b>	<b>Description</b>
	31:0	VCPU_INDEX	Virtual CPU index, starting from 0 and allocated sequentially on each successful TDH.VP.INIT
	63:32	RESERVED	Reserved for enumerating future Intel TDX module capabilities, etc.: set to 0
R10	Reserved for enumerating future Intel TDX module capabilities, etc.: set to 0		
R11	Reserved for enumerating future Intel TDX module capabilities, etc.: set to 0		
Other	Unmodified		

#### Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 10 TDG.VP.INFO provides the TD software with execution environment information – beyond information that is provided by CPUID.



To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.203: TDG.VP.INFO Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions
Implicit	N/A	N/A	TDR page	TDR	None	Opaque	N/A	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	R	Opaque	N/A	Shared(i)
Implicit	N/A	N/A	TDVPS structure	TDVPS	R	Opaque	N/A	Shared

## 5 Completion Status Codes

**Table 20.204: TDG.VP.INFO Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_SUCCESS	TDG.VP.INFO is successful.

### 20.3.7. TDG.VP.VEINFO.GET Leaf

Intel SDM, Vol. 3, 24.9.4 Information for VM Exits Due to Instruction Execution  
 Intel SDM, Vol. 3, 25.5.6 Virtualization Exceptions  
 Intel SDM, Vol. 3, 27.2.5 Information for VM Exits Due to Instruction Execution

- 5 Get Virtualization Exception Information for the recent #VE exception.

**Table 20.205: TDG.VP.VEINFO.GET Input Operands Definition**

Operand	Description
RAX	TDCALL instruction leaf number – see 20.3.1

**Table 20.206: TDG.VP.VEINFO.GET Output Operands Definition**

Operand	Description		
RAX	TDCALL instruction return code – see 20.3.1		
RCX	<b>Bits</b>	<b>Name</b>	<b>Description</b>
	31:0	Exit Reason	The 32-bit value that would have been saved into the VMCS as an exit reason if a VM exit had occurred instead of the virtualization exception
	63:32	Reserved	Reserved: 0
RDX	Exit Qualification: the 64-bit value that would have been saved into the VMCS as an exit qualification if a legacy VM exit had occurred instead of the virtualization exception		
R8	Guest Linear Address: the 64-bit value that would have been saved into the VMCS as a guest-linear address if a legacy VM exit had occurred instead of the virtualization exception		
R9	Guest Physical Address: the 64-bit value that would have been saved into the VMCS as a guest-physical address if a legacy VM exit had occurred instead of the virtualization exception		
R10	<b>Bits</b>	<b>Name</b>	<b>Description</b>
	31:0	VM-exit instruction length	The 32-bit value that would have been saved into the VMCS as VM-exit instruction length if a legacy VM exit had occurred instead of the virtualization exception
	63:32	VM-exit instruction information	The 32-bit value that would have been saved into the VMCS as VM-exit instruction information if a legacy VM exit had occurred instead of the virtualization exception
Other	Unmodified		

#### 10 Leaf Function Description

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

TDG.VP.VEINFO.GET returns the virtualization exception information of a #VE exception that was previously delivered to the guest TD.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.207: TDG.VP.VEINFO.GET Memory Operands Information Definition**

Explicit/ Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions
Implicit	N/A	N/A	TDR page	TDR	None	Opaque	N/A	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	None	Opaque	N/A	Shared(i)
Implicit	N/A	N/A	TDVPS structure	TDVPS	RW	Opaque	N/A	Shared

5 The function checks the following conditions (no specific order is implied):

- The VALID field in TDVPS.VE\_INFO must non-0 to indicate that a valid virtualization information is available.

If successful, the function does the following:

1. Return the EXIT\_REASON, EXIT\_QUALIFICATION, GLA, GPA, INSTRUCTION\_LENGTH and INSTRUCTION\_INFORMATION from TDVPS.VE\_INFO in GPRs.
- 10 2. Clear the VALID field in TDVPS.VE\_INFO to 0 to indicate that the virtualization information has been read.

#### Completion Status Codes

**Table 20.208: TDG.VP.VEINFO.GET Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_NO_VE_INFO	There is no Virtualization Exception information.
TDX_SUCCESS	TDG.VP.VEINFO.GET is successful.

## 20.3.8. TDG.VP.VMCALL Leaf

Perform a TD Exit to the host VMM.

**Table 20.209: TDG.VP.VMCALL Input Operands Definition**

Operand	Description												
RAX	TDCALL instruction leaf number – see 20.3.1												
RCX	<p>A bitmap that controls which part of the guest TD GPR and XMM state is passed as-is to the VMM and back</p> <p>A bit value of 0 indicates that the corresponding register is saved by the Intel TDX module, scrubbed to 0 before SEAMRET to the host VMM, and restored by the Intel TDX module on the following TDH.VP.ENTER.</p> <p>A bit value of 1 indicates that the corresponding register is passed as-is to the host VMM, and on the following TDH.VP.ENTER, the register value is used as input from the host VMM and passed as-is to the guest TD.</p> <p>The value of RCX is passed to the host VMM.</p> <table border="1"> <thead> <tr> <th>Bits</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>15:0</td> <td>GPR Mask</td> <td>           Controls the transfer of GPR values:            Bit 0: RAX (must be 0)            Bit 1: RCX (must be 0)            Bit 2: RDX            Bit 3: RBX            Bit 4: RSP (must be 0)            Bit 5: RBP            Bit 6: RSI            Bit 7: RDI            Bits 15:8: R15 – R8         </td> </tr> <tr> <td>31:16</td> <td>XMM Mask</td> <td>Controls the transfer of XMM15 – XMM0 register values</td> </tr> <tr> <td>63:32</td> <td>Reserved</td> <td>Reserved: must be 0</td> </tr> </tbody> </table>	Bits	Name	Description	15:0	GPR Mask	Controls the transfer of GPR values: Bit 0: RAX (must be 0) Bit 1: RCX (must be 0) Bit 2: RDX Bit 3: RBX Bit 4: RSP (must be 0) Bit 5: RBP Bit 6: RSI Bit 7: RDI Bits 15:8: R15 – R8	31:16	XMM Mask	Controls the transfer of XMM15 – XMM0 register values	63:32	Reserved	Reserved: must be 0
Bits	Name	Description											
15:0	GPR Mask	Controls the transfer of GPR values: Bit 0: RAX (must be 0) Bit 1: RCX (must be 0) Bit 2: RDX Bit 3: RBX Bit 4: RSP (must be 0) Bit 5: RBP Bit 6: RSI Bit 7: RDI Bits 15:8: R15 – R8											
31:16	XMM Mask	Controls the transfer of XMM15 – XMM0 register values											
63:32	Reserved	Reserved: must be 0											
RBX, RDX, RBP, RDI, RSI, R8 – R15	<p>If the corresponding bit in RCX is set to 1, the register value passed as-is to the host VMM on SEAMRET.</p> <p>Else, the register value is not used as an input and is preserved.</p>												
XMM0 – XMM15	<p>If the corresponding bit in RCX is set to 1, the register value passed as-is to the host VMM on SEAMRET.</p> <p>Else, the register value is not used as an input and is preserved.</p>												

**Table 20.210: TDG.VP.VMCALL Output Operands Definition**

Operand	Description
RAX	TDCALL instruction return code: returns a constant value of TDX_SUCCESS (0)
RCX	Unmodified
RBX, RDX, RBP, RDI, RSI, R8 – R15	If the corresponding bit in RCX is set to 1, the register value passed as-is from the host VMM's SEAMCALL(TDH.VP.ENTER) input. Else, the register value is unmodified.
XMM0 – XMM15	If the corresponding bit in RCX is set to 1, the register value passed as-is from the host VMM's SEAMCALL(TDH.VP.ENTER) input. Else, the register value is unmodified.
Other	Unmodified

**Leaf Function Description**

**Note:** The description below is provided at a high level. Actual details, order of checks, returned status codes, etc. may vary.

- 5 TDG.VP.VMCALL performs a TD exit to the host VMM. From the VMM's point of view, this is the termination of a previous SEAMCALL(TDH.VP.ENTER). Selected GPR and XMM state is passed to the VMM host, controlled by RCX as shown above. The rest of the CPU state is saved in TDVPS and replaced with a synthetic state.

10 From the guest TD's point of view, a subsequent SEAMCALL(TDH.VP.ENTER) from the host VMM terminates the TDG.VP.VMCALL function. Most GPR state, and if the value of RCX bit 1 is set, all XMM state, is passed to the TD guest as shown above.

To understand the table and text below, refer to Chapter 15, which explains the general aspects of the Intel TDX interface functions.

**Table 20.211: TDG.VP.VMCALL Memory Operands Information Definition**

Explicit/Implicit	Reg.	Addr. Type	Resource	Resource Type	Access	Access Semantics	Align. Check	Concurrency Restrictions
Implicit	N/A	N/A	TDR page	TDR	None	Opaque	N/A	Shared
Implicit	N/A	N/A	TDCS structure	TDCS	None	Opaque	N/A	Shared(i)
Implicit	N/A	N/A	TDVPS structure	TDVPS	R/W	Opaque	N/A	Shared

- 15 1. Save guest TD CPU state to TDVPS (including TD VMCS):
- 1.1. Save extended state per TDCS.XFAM. There is no strict requirement to save XMM state that will be passed to the host VMM as controlled by RCX. This state will be overwritten on the next TD entry.
  - 1.2. Save GPR state. There is no strict requirement to save GPR state that will be passed to the host VMM as controlled by RCX (but RCX itself must be saved). This state will be overwritten on the next TD entry.
  - 1.3. Advance the saved RIP to the instruction following TDCALL.
- 20 2. Adjust the TDCS TLB tracking counters.
3. Release the shared locking – acquired on TDH.VP.ENTER of TDR, TDCS and TDVPS.
4. Load host VMM state:
- 4.1. Clear the extended state except XMM (per TDCS.XFAM) to synthetic INIT values.
  - 4.2. As controlled by RCX, either clear or set to the guest TD's value the state of XMM0 – XMM15.
  - 4.3. As controlled by RCX, either clear or set to the guest TD's value the state of RBX, RDX, RBP, RDI, RSI and R8 – R15.
  - 4.4. Set RCX to the guest TD's value.
  - 4.5. Set RAX to the TDCALL exit reason.
  - 4.6. Restore other host VMM state – saved during TDH.VP.ENTER.
- 25 5. Execute SEAMRET to return to the host VMM.
- 30

**Note:** Logically, from the point of view of the guest TD, TDG.VP.VMCALL is terminated by the next TDH.VP.ENTER.

**Completion Status Codes****Table 20.212: TDG.VP.VMCALL Completion Status Codes (Returned in RAX) Definition**

Completion Status Code	Description
TDX_OPERAND_INVALID	
TDX_SUCCESS	TDG.VP.VMCALL is successful. TD exit was done, resulting a in a completion of SEAMCALL(TDH.VP.ENTER) on the host VMM side. Later, the host VMM executed SEAMCALL(TDH.VP.ENTER) again, and execution returned to the guest TD VCPU (in TDX non-root mode) completing TDG.VP.VMCALL.