First (H)	Last (H)	Size (H)	MSR Architectural Name	MSR Value after TDH.VP.ENTER
0x001C	0x001C	0x1	IA32_USER_MSR_CTL	Init(native CPUID(7,1).EDX[15])
0x00C1	0x00C8	0x8	IA32_PMCx	Implicit (via IA32_A_PMCx): Init(PERFMON)
0x00E1	0x00E1	0x1	IA32_UMWAIT_CONTROL	Init(virt. CPUID(7,0).ECX[5])
0x0122	0x0122	0x1	IA32_TSX_CTRL	Init(virt. TSX enabled)
0x0186	0x0186	0x1	IA32_PERFEVTSEL0	if CPUID(0xA).EAX[7:0] >= 6 Aliased via new range Else Modified(PERFMON)
0x0187	0x0187	0x1	IA32_PERFEVTSEL1	if CPUID(0xA).EAX[7:0] >= 6 Aliased via new range Else Modified(PERFMON)
0x0188	0x0188	0x1	IA32_PERFEVTSEL2	if CPUID(0xA).EAX[7:0] >= 6 Aliased via new range Else Modified(PERFMON)
0x0189	0x0189	0x1	IA32_PERFEVTSEL3	if CPUID(0xA).EAX[7:0] >= 6 Aliased via new range Else Modified(PERFMON)
0x018A	0x018A	0x1	IA32_PERFEVTSEL4	if CPUID(0xA).EAX[7:0] >= 6 Aliased via new range Else Modified(PERFMON)
0x018B	0x018B	0x1	IA32_PERFEVTSEL5	if CPUID(0xA).EAX[7:0] >= 6 Aliased via new range Else Modified(PERFMON)
0x018C	0x018C	0x1	IA32_PERFEVTSEL6	if CPUID(0xA).EAX[7:0] >= 6 Aliased via new range Else Modified(PERFMON)
0x018D	0x018D	0x1	IA32_PERFEVTSEL7	if CPUID(0xA).EAX[7:0] >= 6 Aliased via new range Else Modified(PERFMON)
0x018E	0x018E	0x1	IA32_PERFEVTSEL8	if CPUID(0xA).EAX[7:0] >= 6 Aliased via new range Else Modified(PERFMON)
0x018F	0x018F	0x1	IA32_PERFEVTSEL9	if CPUID(0xA).EAX[7:0] >= 6 Aliased via new range Else Modified(PERFMON)
0x01A6	0x01A7	0x2	MSR_OFFCORE_RSPx	Init(PERFMON)
0x01C4	0x01C4	0x1	IA32_XFD	Init(virt. CPUID(0xD,0x1).EAX[4])
0x01C5	0x01C5	0x1	IA32_XFD_ERR	Init(virt. CPUID(0xD,0x1).EAX[4])
0x01CC	0x01CC	0x1	IA32_FRED_RSP0	Init(virt. CPUID(7,1).EAX[17])
0x01D9	0x01D9	0x1	IA32_DEBUGCTL	INIT, except for the following bits which are preserved: Bit 1 (BTF) Bit 12 (FREEZE_PERFMON_ON_PMI) Bit 14 (FREEZE_WHILE_SMM)
0x0309	0x0310	0x8	IA32_FIXED_CTRx	if CPUID(0xA).EAX[7:0] Aliased via new range Else Init(PERFMON)
0x0329	0x0329	0x1	IA32_PERF_METRICS	Init(PERFMON && IA32_PERF_CAPABILITIES[15])
0x038D	0x038D	0x1	IA32_FIXED_CTR_CTRL	Modified(PERFMON)
0x038E	0x038E	0x1	IA32_PERF_GLOBAL_STATUS	Init(PERFMON)
0x038F	0x038F	0x1	IA32_PERF_GLOBAL_CTRL	Init(PERFMON)
0x03F1	0x03F1	0x1	IA32_PEBS_ENABLE	Modified(PERFMON && ~IA32_MISC_ENABLE[12])
0x03F2	0x03F2	0x1	MSR_PEBS_MATRIX_VECT	Modified(PERFMON && ~IA32_MISC_ENABLE[12])
0x03F4	0x03F4	0x1	IA32_PEBS_BASE	Init(virt. CPUID(0x23,0).EAX[5])

0x03F5	0x03F5	0x1	IA32_PEBS_INDEX	Init(virt. CPUID(0x23,0).EAX[5])
0x03F6	0x03F6	0x1	MSR_PEBS_LD_LATENCY	Modified(PERFMON && ~IA32_MISC_ENABLE[12])
0x03F7	0x03F7	0x1	MSR_PEBS_FRONTEND	Modified(PERFMON && ~IA32_MISC_ENABLE[12])
0x04C1	0x04C8	0x8	IA32_A_PMCx	if CPUID(0xA).EAX[7:0] Aliased via new range Else Init(PERFMON)
0x0550	0x0550	0x1	MSR_SEAM_SAI_MODE	None
0x0560	0x0560	0x1	IA32_RTIT_OUTPUT_BASE	Init(XFAM(8))
0x0561	0x0561	0x1	IA32_RTIT_OUTPUT_MASK_PTRS	Init(XFAM(8))
0x0570	0x0570	0x1	IA32_RTIT_CTL	Init(XFAM(8))
0x0571	0x0571	0x1	IA32_RTIT_STATUS	Init(XFAM(8))
0x0572	0x0572	0x1	IA32_RTIT_CR3_MATCH	Init(XFAM(8))
0x0580	0x0580	0x1	IA32_RTIT_ADDR0_A	Init(XFAM(8))
0x0581	0x0581	0x1	IA32_RTIT_ADDR0_B	Init(XFAM(8))
0x0582	0x0582	0x1	IA32_RTIT_ADDR1_A	Init(XFAM(8))
0x0583	0x0583	0x1	IA32_RTIT_ADDR1_B	Init(XFAM(8))
0x0584	0x0584	0x1	IA32_RTIT_ADDR2_A	Init(XFAM(8))
0x0585	0x0585	0x1	IA32_RTIT_ADDR2_B	Init(XFAM(8))
0x0586	0x0586	0x1	IA32_RTIT_ADDR3_A	Init(XFAM(8))
0x0587	0x0587	0x1	IA32_RTIT_ADDR3_B	Init(XFAM(8))
0x06A0	0x06A0	0x1	IA32_U_CET	Init(XFAM[11] | XFAM[12])
0x06A4	0x06A4	0x1	IA32_PL0_SSP	Init(XFAM[11] | XFAM[12] | virt. CPUID(7,1).EAX[17])
0x06A5	0x06A5	0x1	IA32_PL1_SSP	Init(XFAM[11] | XFAM[12])
0x06A6	0x06A6	0x1	IA32_PL2_SSP	Init(XFAM[11] | XFAM[12])
0x06A7	0x06A7	0x1	IA32_PL3_SSP	Init(XFAM[11] | XFAM[12])
0x0985	0x0985	0x1	IA32_UINTR_RR	Init(XFAM[14])
0x0986	0x0986	0x1	IA32_UINTR_HANDLER	Init(XFAM[14])
0x0987	0x0987	0x1	IA32_UINTR_STACKADJUST	Init(XFAM[14])
0x0988	0x0988	0x1	IA32_UINTR_MISC	Init(XFAM[14])
0x0989	0x0989	0x1	IA32_UINTR_PD	Init(XFAM[14])
0x098A	0x098A	0x1	IA32_UINTR_TT	Init(XFAM[14])
0x09FD	0x09FD	0x1	TSX_STORE_ADDRESS	Init((virt. CPUID(0x7,0).EBX[4] || virt. CPUID(0x7,0).EBX[11]) && PERFMON_&& IA32_PERF_CAPABILITIES[18])
0x0DA0	0x0DA0	0x1	IA32_XSS	Supervisor-mode feature bits of XFAM (bits 8, 16:10)
0x1200	0x12FF	0x100	IA32_LBR_INFO	Init(XFAM[15])
0x14CE	0x14CE	0x1	IA32_LBR_CTL	Init(XFAM[15])
0x14CF	0x14CF	0x1	IA32_LBR_DEPTH	Modified(XFAM[15])
0x1500	0x15FF	0x100	IA32_LBR_x_FROM_IP	Init(XFAM[15])
0x1600	0x16FF	0x100	IA32_LBR_x_TO_IP	Init(XFAM[15])
0x1900	0x1900	0x1	IA32_PMC_GP0_CTR	Init(PERFMON && (CPUID(0xa).EAX[7:0] >= 6))
0x1901	0x1901	0x1	IA32_PMC_GP0_CFG_A	Modified(PERFMON && (CPUID(0xa).EAX[7:0] >= 6))
0x1903	0x1903	0x1	IA32_PMC_GP0_CFG_C	Init(virt CPUID(0x23,5).EAX[0])
0x1904	0x1904	0x1	IA32_PMC_GP1_CTR	Init(PERFMON && (CPUID(0xa).EAX[7:0] >= 6))
0x1905	0x1905	0x1	IA32_PMC_GP1_CFG_A	Modified(PERFMON && (CPUID(0xa).EAX[7:0] >= 6))
0x1907	0x1907	0x1	IA32_PMC_GP1_CFG_C	Init(virt CPUID(0x23,5).EAX[1])
0x1908	0x1908	0x1	IA32_PMC_GP2_CTR	Init(PERFMON && (CPUID(0xa).EAX[7:0] >= 6))
0x1909	0x1909	0x1	IA32_PMC_GP2_CFG_A	Modified(PERFMON && (CPUID(0xa).EAX[7:0] >= 6))
0x190B	0x190B	0x1	IA32_PMC_GP2_CFG_C	Init(virt CPUID(0x23,5).EAX[2])
0x190C	0x190C	0x1	IA32_PMC_GP3_CTR	Init(PERFMON && (CPUID(0xa).EAX[7:0] >= 6))
0x190D	0x190D	0x1	IA32_PMC_GP3_CFG_A	Modified(PERFMON && (CPUID(0xa).EAX[7:0] >= 6))
0x190F	0x190F	0x1	IA32_PMC_GP3_CFG_C	Init(virt CPUID(0x23,5).EAX[3])
0x1910	0x1910	0x1	IA32_PMC_GP4_CTR	Init(PERFMON && (CPUID(0xa).EAX[7:0] >= 6))
0x1911	0x1911	0x1	IA32_PMC_GP4_CFG_A	Modified(PERFMON && (CPUID(0xa).EAX[7:0] >= 6))
0x1913	0x1913	0x1	IA32_PMC_GP4_CFG_C	Init(virt CPUID(0x23,5).EAX[4])
0x1914	0x1914	0x1	IA32_PMC_GP5_CTR	Init(PERFMON && (CPUID(0xa).EAX[7:0] >= 6))
0x1915	0x1915	0x1	IA32_PMC_GP5_CFG_A	Modified(PERFMON && (CPUID(0xa).EAX[7:0] >= 6))
0x1917	0x1917	0x1	IA32_PMC_GP5_CFG_C	Init(virt CPUID(0x23,5).EAX[5])

0x1918	0x1918	0x1	IA32_PMC_GP6_CTR	Init(PERFMON && (CPUID(0xa).EAX[7:0) >= 6))
0x1919	0x1919	0x1	IA32_PMC_GP6_CFG_A	Modified(PERFMON && (CPUID(0xa).EAX[7:0) >= 6))
0x191B	0x191B	0x1	IA32_PMC_GP6_CFG_C	Init(virt CPUID(0x23,5).EAX[6])
0x191C	0x191C	0x1	IA32_PMC_GP7_CTR	Init(PERFMON && (CPUID(0xa).EAX[7:0) >= 6))
0x191D	0x191D	0x1	IA32_PMC_GP7_CFG_A	Modified(PERFMON && (CPUID(0xa).EAX[7:0) >= 6))
0x191F	0x191F	0x1	IA32_PMC_GP7_CFG_C	Init(virt CPUID(0x23,5).EAX[7])
0x1980	0x1980	0x1	IA32_PMC_FX0_CTR	Init(PERFMON && (CPUID(0xa).EAX[7:0) >= 6))
0x1983	0x1983	0x1	IA32_PMC_FX0_CFG_C	Init(virt CPUID(0x23,5).ECX[0])
0x1984	0x1984	0x1	IA32_PMC_FX1_CTR	Init(PERFMON && (CPUID(0xa).EAX[7:0) >= 6))
0x1987	0x1987	0x1	IA32_PMC_FX1_CFG_C	Init(virt CPUID(0x23,5).ECX[1])
0x1988	0x1988	0x1	IA32_PMC_FX2_CTR	Init(PERFMON && (CPUID(0xa).EAX[7:0) >= 6))
0x198B	0x198B	0x1	IA32_PMC_FX2_CFG_C	Init(virt CPUID(0x23,5).ECX[2])
0x198C	0x198C	0x1	IA32_PMC_FX3_CTR	Init(PERFMON && (CPUID(0xa).EAX[7:0) >= 6))
0x198F	0x198F	0x1	IA32_PMC_FX3_CFG_C	Init(virt CPUID(0x23,5).ECX[3])
0x1990	0x1990	0x1	IA32_PMC_FX4_CTR	Init(PERFMON && (CPUID(0xa).EAX[7:0) >= 6))
0x1993	0x1993	0x1	IA32_PMC_FX4_CFG_C	Init(virt CPUID(0x23,5).ECX[4])
0x1994	0x1994	0x1	IA32_PMC_FX5_CTR	Init(PERFMON && (CPUID(0xa).EAX[7:0) >= 6))
0x1997	0x1997	0x1	IA32_PMC_FX5_CFG_C	Init(virt CPUID(0x23,5).ECX[5])
0x1998	0x1998	0x1	IA32_PMC_FX6_CTR	Init(PERFMON && (CPUID(0xa).EAX[7:0) >= 6))
0x199B	0x199B	0x1	IA32_PMC_FX6_CFG_C	Init(virt CPUID(0x23,5).ECX[6])
0x1B01	0x1B01	0x1	IA32_UARCH_MISC_CTL	INIT
0xC0000081	0xC0000081	0x1	IA32_STAR	INIT
0xC0000082	0xC0000082	0x1	IA32_LSTAR	INIT
0xC0000084	0xC0000084	0x1	IA32_FMASK	INIT
0xC0000102	0xC0000102	0x1	IA32_KERNEL_GS_BASE	INIT
0xC0000103	0xC0000103	0x1	IA32_TSC_AUX	INIT