First (H)	Last (H)	Size (H)	MSR Architectural Name	On RDMSR	On WRMSR	#VE on RD and WR
Default	Default	N/A	Any MSR not in this table whose index is in 0x0-0x1FFF nor 0xC0000000-0xC0001FFF	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
Out of Ranges	Out of Ranges	N/A	Any MSR whose index is not in 0x0-0x1FFF nor 0xC0000000-0xC0001FFF	#VE	#VE	#VE
0x0000	0x0000	0x1	IA32_P5_MC_ADDR	#VE	#VE	#VE
0x0001	0x0001	0x1	IA32_P5_MC_TYPE	#VE	#VE	#VE
0x0006	0x0006	0x1	IA32_MONITOR_FILTER_SIZE	#VE	#VE	#VE
0x0010	0x0010	0x1	IA32_TIME_STAMP_COUNTER	Native	#VE	
0x0017	0x0017	0x1	IA32_PLATFORM_ID	#VE	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x001B	0x001B	0x1	IA32_APIC_BASE	#VE	#VE	#VE
0x001C	0x001C	0x1	IA32_USER_MSR_CTL	Inject_GP(~virt. CPUID(7,1).EDX[15])	Inject_GP(~virt. CPUID(7,1).EDX[15])	
0x002F	0x002F	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0033	0x0033	0x1	MSR_MEMORY_CTRL	inject_GP_or_VE(~virt. CPUID(7,0).EDX[30])	inject_GP_or_VE(~virt. CPUID(7,0).EDX[30])	

0x0034	0x0034	0x1	MSR_SMI_COUNT	if TD_CTLS.REDUCE_VE
				  read from TDVPS
				else
				  #VE(CONFIG_PARAVIRT)
					if TD_CTLS.REDUCE_VE
					  write to TDVPS
					else
					  #VE(CONFIG_PARAVIRT)	

0x003A	0x003A	0x1	IA32_FEATURE_CONTROL	if TD_CTLS.REDUCE_VE
				  return 1 (locked)
				else
				  #VE(CONFIG_PARAVIRT)
					inject_GP_or_VE(TD_CTLS.REDUCE_VE)	

0x003B	0x003B	0x1	IA32_TSC_ADJUST	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0048	0x0048	0x1	IA32_SPEC_CTRL	Native	Native	
0x0049	0x0049	0x1	IA32_PRED_CMD	Native	Native	

0x004E	0x004E	0x1	IA32_PPIN_CTL	if TD_CTLS.REDUCE_VE
				  return 1 (locked, disabled)
				else
				  #VE(CONFIG_PARAVIRT)
					inject_GP_or_VE(TD_CTLS.REDUCE_VE)	

0x004F	0x004F	0x1	IA32_PPIN	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	

0x0079	0x0079	0x1	IA32_BIOS_UPDT_TRIG	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	if TD_CTLS.REDUCE_VE
					  ignore
					else
					  #VE(CONFIG_PARAVIRT	

0x007A	0x007A	0x1	IA32_FEATURE_ACTIVATION	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0082	0x0082	0x1	IA32_FZM_RANGE_INDEX	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0083	0x0083	0x1	IA32_FZM_DOMAIN_CONFIG	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0084	0x0084	0x1	IA32_FZM_RANGE_STARTADDR	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0085	0x0085	0x1	IA32_FZM_RANGE_ENDADDR	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0086	0x0086	0x1	IA32_FZM_RANGE_WRITESTATUS	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0087	0x0087	0x1	IA32_MKTME_PARTITIONING	Inject_GP_or_VE (~virt. CPUID(7,0).EDX[18])	Inject_GP_or_VE (~virt. CPUID(7,0).EDX[18])	

0x008B	0x008B	0x1	IA32_BIOS_SIGN_ID	if TD_CTLS.REDUCE_VE
				  return 0xFFFFFFFF
				else
				  #VE(CONFIG_PARAVIRT)
					if TD_CTLS.REDUCE_VE
					  ignore
					else
					  #VE(CONFIG_PARAVIRT)	

0x008C	0x008F	0x4	IA32_SGXLEPUBKEYHASHx	#GP(0)	#GP(0)	
0x0098	0x0098	0x1	MSR_WBINVDP	#GP(0)	#GP(0)	
0x0099	0x0099	0x1	MSR_WBNOINVDP	#GP(0)	#GP(0)	
0x009A	0x009A	0x1	MSR_INTR_PENDING	#GP(0)	#GP(0)	
0x009B	0x009B	0x1	IA32_SMM_MONITOR_CTL	#GP(0)	#GP(0)	
0x009E	0x009E	0x1	IA32_SMBASE	#GP(0)	#GP(0)	
0x00BC	0x00BC	0x1	IA32_MISC_PACKAGE_CTLS	Native	#VE	
0x00BD	0x00BD	0x1	IA32_XAPIC_DISABLE_STATUS	Bit 0 (LEGACY_APIC_DISABLED) = 1 Other bits are 0	Native	
0x00C1	0x00C8	0x8	IA32_PMCx	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	

0x00CE	0x00CE	0x1	MSR_PLATFORM_INFO	if TD_CTLS.REDUCE_VE
				  return 0
				else
				  #VE(CONFIG_PARAVIRT)
					inject_GP_or_VE(TD_CTLS.REDUCE_VE)	

0x00CF	0x00CF	0x1	IA32_CORE_CAPABILITIES	inject_GP_or_VE(~virt. CPUID(7,0).EDX[30])	#GP(0)	
0x00E1	0x00E1	0x1	IA32_UMWAIT_CONTROL	Inject_GP(~virt. CPUID(7,0).ECX[5])	Inject_GP(~virt. CPUID(7,0).ECX[5])	
0x00E7	0x00E7	0x1	IA32_MPERF	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x00E8	0x00E8	0x1	IA32_APERF	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x00ED	0x00ED	0x1	MSR_RAR_CONTROL	inject_GP_or_VE(~virt. CPUID(7,0).EDX[30])	inject_GP_or_VE(~virt. CPUID(7,0).EDX[30])	
0x00EE	0x00EE	0x1	MSR_RAR_ACTION_VECTOR	inject_GP_or_VE(~virt. CPUID(7,0).EDX[30])	inject_GP_or_VE(~virt. CPUID(7,0).EDX[30])	
0x00EF	0x00EF	0x1	MSR_RAR_PAYLOAD_TABLE_BASE	inject_GP_or_VE(~virt. CPUID(7,0).EDX[30])	inject_GP_or_VE(~virt. CPUID(7,0).EDX[30])	
0x00F0	0x00F0	0x1	MSR_RAR_INFO	inject_GP_or_VE(~virt. CPUID(7,0).EDX[30])	inject_GP_or_VE(~virt. CPUID(7,0).EDX[30])	
0x00FE	0x00FE	0x1	IA32_MTRRCAP	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	#GP(0)	
0x010A	0x010A	0x1	IA32_ARCH_CAPABILITIES	See the [Base Spec] section on IA32_ARCH_CAPABILITIES MSR	Native	
0x010B	0x010B	0x1	IA32_FLUSH_CMD	Native	Native	
0x010F	0x010F	0x1	IA32_TSX_FORCE_ABORT	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0122	0x0122	0x1	IA32_TSX_CTRL	Inject_GP(~(virt. TSX enabled))	Inject_GP(~(virt. TSX enabled))	
0x0123	0x0123	0x1	IA32_MCU_OPT_CTRL	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	

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0x0140	0x0140	0x1	MSR_FEATURE_ENABLES	if TD_CTLS.REDUCE_VE
				  return 0
				else
				  #VE(CONFIG_PARAVIRT)
					if TD_CTLS.REDUCE_VE
					  if value == 0, ignore
					  else #GP
					else
					  #VE(CONFIG_PARAVIRT)	

0x0174	0x0174	0x1	IA32_SYSENTER_CS	Native	Native	
0x0175	0x0175	0x1	IA32_SYSENTER_ESP	Native	Native	
0x0176	0x0176	0x1	IA32_SYSENTER_EIP	Native	Native	
0x0179	0x0179	0x1	IA32_MCG_CAP	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	#GP(0)	
0x017A	0x017A	0x1	IA32_MCG_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x017B	0x017B	0x1	IA32_MCG_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0186	0x018D	0x8	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	

0x0186	0x0186	0x1	IA32_PERFEVTSEL0	if (~PERFMON)
				  #GP(0)
				else if (EVENT_FILTERS_NUM > 0)
				  Special event filtering
					if (~PERFMON)
					  #GP(0)
					else if ((EN_LBR_LOG(bit 35) == 1) && (virt. CPUID(0x1C).ECX[16] == 0))
					  #GP(0)
					else if (EVENT_FILTERS_NUM > 0)
					  Special event filtering	

0x0187	0x0187	0x1	IA32_PERFEVTSEL1	if (~PERFMON)
				  #GP(0)
				else if (EVENT_FILTERS_NUM > 0)
				  Special event filtering
					if (~PERFMON)
					  #GP(0)
					else if ((EN_LBR_LOG(bit 35) == 1) && (virt. CPUID(0x1C).ECX[17] == 0))
					  #GP(0)
					else if (EVENT_FILTERS_NUM > 0)
					  Special event filtering	

0x0188	0x0188	0x1	IA32_PERFEVTSEL2	if (~PERFMON)
				  #GP(0)
				else if (EVENT_FILTERS_NUM > 0)
				  Special event filtering
					if (~PERFMON)
					  #GP(0)
					else if ((EN_LBR_LOG(bit 35) == 1) && (virt. CPUID(0x1C).ECX[18] == 0))
					  #GP(0)
					else if (EVENT_FILTERS_NUM > 0)
					  Special event filtering	

0x0189	0x0189	0x1	IA32_PERFEVTSEL3	if (~PERFMON)
				  #GP(0)
				else if (EVENT_FILTERS_NUM > 0)
				  Special event filtering
					if (~PERFMON)
					  #GP(0)
					else if ((EN_LBR_LOG(bit 35) == 1) && (virt. CPUID(0x1C).ECX[19] == 0))
					  #GP(0)
					else if (EVENT_FILTERS_NUM > 0)
					  Special event filtering	

0x018A	0x018A	0x1	IA32_PERFEVTSEL4	if (~PERFMON)
				  #GP(0)
				else if (EVENT_FILTERS_NUM > 0)
				  Special event filtering
					if (~PERFMON)
					  #GP(0)
					else if ((EN_LBR_LOG(bit 35) == 1) && (virt. CPUID(0x1C).ECX[20] == 0))
					  #GP(0)
					else if (EVENT_FILTERS_NUM > 0)
					  Special event filtering	

0x018B	0x018B	0x1	IA32_PERFEVTSEL5	if (~PERFMON)
				  #GP(0)
				else if (EVENT_FILTERS_NUM > 0)
				  Special event filtering
					if (~PERFMON)
					  #GP(0)
					else if ((EN_LBR_LOG(bit 35) == 1) && (virt. CPUID(0x1C).ECX[21] == 0))
					  #GP(0)
					else if (EVENT_FILTERS_NUM > 0)
					  Special event filtering	

0x018C	0x018C	0x1	IA32_PERFEVTSEL6	if (~PERFMON)
				  #GP(0)
				else if (EVENT_FILTERS_NUM > 0)
				  Special event filtering
					if (~PERFMON)
					  #GP(0)
					else if ((EN_LBR_LOG(bit 35) == 1) && (virt. CPUID(0x1C).ECX[22] == 0))
					  #GP(0)
					else if (EVENT_FILTERS_NUM > 0)
					  Special event filtering	

0x018D	0x018D	0x1	IA32_PERFEVTSEL7	if (~PERFMON)
				  #GP(0)
				else if (EVENT_FILTERS_NUM > 0)
				  Special event filtering
					if (~PERFMON)
					  #GP(0)
					else if ((EN_LBR_LOG(bit 35) == 1) && (virt. CPUID(0x1C).ECX[23] == 0))
					  #GP(0)
					else if (EVENT_FILTERS_NUM > 0)
					  Special event filtering	

0x018E	0x018E	0x1	IA32_PERFEVTSEL8	if (~PERFMON)
				  #GP(0)
				else if (EVENT_FILTERS_NUM > 0)
				  Special event filtering
					if (~PERFMON)
					  #GP(0)
					else if ((EN_LBR_LOG(bit 35) == 1) && (virt. CPUID(0x1C).ECX[24] == 0))
					  #GP(0)
					else if (EVENT_FILTERS_NUM > 0)
					  Special event filtering	

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0x018F	0x018F	0x1	IA32_PERFEVTSEL9	if (~PERFMON) #GP(0) else if (EVENT_FILTERS_NUM > 0) Special event filtering	if (~PERFMON) #GP(0) else if ((EN_LBR_LOG(bit 35) == 1) && (virt. CPUID(0x1C).ECX[25] == 0)) #GP(0) else if (EVENT_FILTERS_NUM > 0) Special event filtering	
0x0195	0x0195	0x1	IA32_OVERCLOCKING_STATUS	#GP(0)	#GP(0)	
0x0198	0x0198	0x1	IA32_PERF_STATUS	inject_GP_or_VE(~virt. CPUID(1).ECX[7])	inject_GP_or_VE(~virt. CPUID(1).ECX[7])	
0x0199	0x0199	0x1	IA32_PERF_CTL	inject_GP_or_VE(~virt. CPUID(1).ECX[7])	inject_GP_or_VE(~virt. CPUID(1).ECX[7])	
0x019A	0x019A	0x1	IA32_CLOCK_MODULATION	inject_GP_or_VE(~virt. CPUID(1).EDX[22])	inject_GP_or_VE(~virt. CPUID(1).EDX[22])	
0x019B	0x019B	0x1	IA32_THERM_INTERRUPT	inject_GP_or_VE(~virt. CPUID(1).EDX[22])	inject_GP_or_VE(~virt. CPUID(1).EDX[22])	
0x019C	0x019C	0x1	IA32_THERM_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[22])	inject_GP_or_VE(~virt. CPUID(1).EDX[22])	
0x019D	0x019D	0x1	MSR_THERM2_CTL	inject_GP_or_VE(~virt. CPUID(1).ECX[8])	inject_GP_or_VE(~virt. CPUID(1).ECX[8])	
0x019E	0x019E	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x01A0	0x01A0	0x1	IA32_MISC_ENABLE	Read from TDVPS	if TD_CTLS.REDUCE_VE write to TDVPS, see [ABI Spec] for details else #VE(CONFIG_PARAVIRT)	
0x01A6	0x01A7	0x2	MSR_OFFCORE_RSPx	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x01B0	0x01B0	0x1	IA32_ENERGY_PERF_BIAS	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x01B1	0x01B1	0x1	IA32_PACKAGE_THERM_STATUS	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x01B2	0x01B2	0x1	IA32_PACKAGE_THERM_INTERRUPT	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x01C2	0x01C2	0x1	IA32_HW_GET_LP_PM_META_DATA	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x01C3	0x01C3	0x1	IA32_HW_SET_LP_PM_META_DATA	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x01C4	0x01C4	0x1	IA32_XFD	Inject_GP(~(virt. CPUID(0xD,0x1).EAX[4]))	Inject_GP(~(virt. CPUID(0xD,0x1).EAX[4]))	
0x01C5	0x01C5	0x1	IA32_XFD_ERR	Inject_GP(~(virt. CPUID(0xD,0x1).EAX[4]))	Inject_GP(~(virt. CPUID(0xD,0x1).EAX[4]))	
0x01C7	0x01C7	0x1	IA32_DD_TRHTTLE_DEACTIVATE_MSR	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x01CA	0x01CA	0x1	IA32_DD_DI_CAPABILITY_MSR	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x01CB	0x01CB	0x1	IA32_DD_DI_ACTIVATE_MSR	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x01CC	0x01CC	0x1	IA32_FRED_RSP0	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	
0x01CD	0x01CD	0x1	IA32_FRED_RSP1	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	
0x01CE	0x01CE	0x1	IA32_FRED_RSP2	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	
0x01CF	0x01CF	0x1	IA32_FRED_RSP3	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	
0x01D0	0x01D0	0x1	IA32_FRED_STKLVLS	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	
0x01D1	0x01D1	0x1	IA32_FRED_SSP1	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	
0x01D2	0x01D2	0x1	IA32_FRED_SSP2	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	
0x01D3	0x01D3	0x1	IA32_FRED_SSP3	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	
0x01D4	0x01D4	0x1	IA32_FRED_CONFIG	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	Inject_GP(~(virt. CPUID(7,1).EAX[17]))	
0x01D9	0x01D9	0x1	IA32_DEBUGCTL	Clear ENABLE_UNCORE_PMI (bit 13)	#GP if invalid, #VE if value is not supported for TD. For details see the [Base Spec] Debug and Profiling Architecture chapter.	
0x01F2	0x01F2	0x1	IA32_SMRR_PHYSBASE	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x01F3	0x01F3	0x1	IA32_SMRR_PHYSMASK	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x01F6	0x01F6	0x1	IA32_SMRR2_PHYSBASE	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x01F7	0x01F7	0x1	IA32_SMRR2_PHYSMASK	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x01F8	0x01F8	0x1	IA32_PLATFORM_DCA_CAP	Inject_GP_or_VE(~virt. CPUID(0x1).ECX[18])	Inject_GP_or_VE(~virt. CPUID(0x1).ECX[18])	
0x01F9	0x01F9	0x1	IA32_CPU_DCA_CAP	Inject_GP_or_VE(~virt. CPUID(0x1).ECX[18])	Inject_GP_or_VE(~virt. CPUID(0x1).ECX[18])	
0x01FA	0x01FA	0x1	IA32_DCA_0_CAP	Inject_GP_or_VE(~virt. CPUID(0x1).ECX[18])	Inject_GP_or_VE(~virt. CPUID(0x1).ECX[18])	
0x0200	0x0200	0x1	IA32_MTRR_PHYSBASE0	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0201	0x0201	0x1	IA32_MTRR_PHYSMASK0	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0202	0x0202	0x1	IA32_MTRR_PHYSBASE1	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0203	0x0203	0x1	IA32_MTRR_PHYSMASK1	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0204	0x0204	0x1	IA32_MTRR_PHYSBASE2	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0205	0x0205	0x1	IA32_MTRR_PHYSMASK2	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0206	0x0206	0x1	IA32_MTRR_PHYSBASE3	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0207	0x0207	0x1	IA32_MTRR_PHYSMASK3	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0208	0x0208	0x1	IA32_MTRR_PHYSBASE4	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0209	0x0209	0x1	IA32_MTRR_PHYSMASK4	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x020A	0x020A	0x1	IA32_MTRR_PHYSBASE5	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x020B	0x020B	0x1	IA32_MTRR_PHYSMASK5	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x020C	0x020C	0x1	IA32_MTRR_PHYSBASE6	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x020D	0x020D	0x1	IA32_MTRR_PHYSMASK6	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x020E	0x020E	0x1	IA32_MTRR_PHYSBASE7	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x020F	0x020F	0x1	IA32_MTRR_PHYSMASK7	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0210	0x0210	0x1	IA32_MTRR_PHYSBASE8	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0211	0x0211	0x1	IA32_MTRR_PHYSMASK8	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0212	0x0212	0x1	IA32_MTRR_PHYSBASE9	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0213	0x0213	0x1	IA32_MTRR_PHYSMASK9	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0250	0x0250	0x1	IA32_MTRR_FIX64K_00000	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0258	0x0258	0x1	IA32_MTRR_FIX16K_80000	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0259	0x0259	0x1	IA32_MTRR_FIX16K_A0000	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0268	0x0268	0x1	IA32_MTRR_FIX4K_C0000	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0269	0x0269	0x1	IA32_MTRR_FIX4K_C8000	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x026A	0x026A	0x1	IA32_MTRR_FIX4K_D0000	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x026B	0x026B	0x1	IA32_MTRR_FIX4K_D8000	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	

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0x026C	0x026C	0x1	IA32_MTRR_FIX4K_E0000	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x026D	0x026D	0x1	IA32_MTRR_FIX4K_E8000	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x026E	0x026E	0x1	IA32_MTRR_FIX4K_F0000	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x026F	0x026F	0x1	IA32_MTRR_FIX4K_F8000	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0276	0x0276	0x1	MSR_SLAM_ENABLE	#GP(0)	#GP(0)	
0x0277	0x0277	0x1	IA32_PAT	Native	Native	
0x0280	0x029F	0x20	IA32_MCx_CTL2	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x02A0	0x02A7	0x8	IA32_PRMRR_BASEx	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x02C0	0x02C0	0x1	IA32_FUSARR_BASE	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x02C1	0x02C1	0x1	IA32_FUSARR_MASK	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x02FF	0x02FF	0x1	IA32_MTRR_DEF_TYPE	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	inject_GP_or_VE(~virt. CPUID(1).EDX[12])	
0x0302	0x0302	0x1	BIOS_SE_SVN	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0303	0x0303	0x1	Future BIOS_SE_SVN Expansion	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0309	0x0310	0x8	IA32_FIXED_CTRx	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x0329	0x0329	0x1	IA32_PERF_METRICS	#GP(0)	#GP(0)	

0x0345	0x0345	0x1	IA32_PERF_CAPABILITIES	if ~PERFMON
				  return 0
				else if ~XFAM[8]
				  clear bit 16
				  clear bit 18
				else
				  Native
					Inject_GP(~PERFMON)	

0x038D	0x038D	0x1	IA32_FIXED_CTR_CTRL	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x038E	0x038E	0x1	IA32_PERF_GLOBAL_STATUS	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x038F	0x038F	0x1	IA32_PERF_GLOBAL_CTRL	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x0390	0x0390	0x1	IA32_PERF_GLOBAL_STATUS_RESET	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x0391	0x0391	0x1	IA32_PERF_GLOBAL_STATUS_SET	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x0392	0x0392	0x1	IA32_PERF_GLOBAL_INUSE	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x03F1	0x03F1	0x1	IA32_PEBS_ENABLE	Inject_GP(~PERFMON || IA32_MISC_ENABLE[12])	Inject_GP(~PERFMON || IA32_MISC_ENABLE[12])	
0x03F2	0x03F2	0x1	MSR_PEBS_MATRIX_VECT	Inject_GP(~PERFMON || IA32_MISC_ENABLE[12])	Inject_GP(~PERFMON || IA32_MISC_ENABLE[12])	
0x03F3	0x03F3	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x03F4	0x03F4	0x1	IA32_PEBS_BASE	inject_GP(~virt. CPUID(0x23,0).EAX[5])	inject_GP(~virt. CPUID(0x23,0).EAX[5])	
0x03F5	0x03F5	0x1	IA32_PEBS_INDEX	inject_GP(~virt. CPUID(0x23,0).EAX[5])	inject_GP(~virt. CPUID(0x23,0).EAX[5])	
0x03F6	0x03F6	0x1	MSR_PEBS_LD_LATENCY	Inject_GP(~PERFMON || IA32_MISC_ENABLE[12])	Inject_GP(~PERFMON || IA32_MISC_ENABLE[12])	
0x03F7	0x03F7	0x1	MSR_PEBS_FRONTEND	Inject_GP(~PERFMON || IA32_MISC_ENABLE[12])	Inject_GP(~PERFMON || IA32_MISC_ENABLE[12])	
0x0400	0x0400	0x1	IA32_MC0_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0401	0x0401	0x1	IA32_MC0_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0402	0x0402	0x1	IA32_MC0_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0403	0x0403	0x1	IA32_MC0_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0404	0x0404	0x1	IA32_MC1_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0405	0x0405	0x1	IA32_MC1_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0406	0x0406	0x1	IA32_MC1_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0407	0x0407	0x1	IA32_MC1_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0408	0x0408	0x1	IA32_MC2_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0409	0x0409	0x1	IA32_MC2_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x040A	0x040A	0x1	IA32_MC2_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x040B	0x040B	0x1	IA32_MC2_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x040C	0x040C	0x1	IA32_MC3_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x040D	0x040D	0x1	IA32_MC3_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x040E	0x040E	0x1	IA32_MC3_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x040F	0x040F	0x1	IA32_MC3_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0410	0x0410	0x1	IA32_MC4_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0411	0x0411	0x1	IA32_MC4_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0412	0x0412	0x1	IA32_MC4_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0413	0x0413	0x1	IA32_MC4_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0414	0x0414	0x1	IA32_MC5_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0415	0x0415	0x1	IA32_MC5_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0416	0x0416	0x1	IA32_MC5_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0417	0x0417	0x1	IA32_MC5_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0418	0x0418	0x1	IA32_MC6_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0419	0x0419	0x1	IA32_MC6_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x041A	0x041A	0x1	IA32_MC6_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x041B	0x041B	0x1	IA32_MC6_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x041C	0x041C	0x1	IA32_MC7_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x041D	0x041D	0x1	IA32_MC7_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x041E	0x041E	0x1	IA32_MC7_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x041F	0x041F	0x1	IA32_MC7_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0420	0x0420	0x1	IA32_MC8_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0421	0x0421	0x1	IA32_MC8_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0422	0x0422	0x1	IA32_MC8_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0423	0x0423	0x1	IA32_MC8_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0424	0x0424	0x1	IA32_MC9_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0425	0x0425	0x1	IA32_MC9_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0426	0x0426	0x1	IA32_MC9_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0427	0x0427	0x1	IA32_MC9_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0428	0x0428	0x1	IA32_MC10_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0429	0x0429	0x1	IA32_MC10_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	

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0x042A	0x042A	0x1	IA32_MC10_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x042B	0x042B	0x1	IA32_MC10_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x042C	0x042C	0x1	IA32_MC11_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x042D	0x042D	0x1	IA32_MC11_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x042E	0x042E	0x1	IA32_MC11_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x042F	0x042F	0x1	IA32_MC11_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0430	0x0430	0x1	IA32_MC12_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0431	0x0431	0x1	IA32_MC12_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0432	0x0432	0x1	IA32_MC12_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0433	0x0433	0x1	IA32_MC12_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0434	0x0434	0x1	IA32_MC13_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0435	0x0435	0x1	IA32_MC13_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0436	0x0436	0x1	IA32_MC13_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0437	0x0437	0x1	IA32_MC13_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0438	0x0438	0x1	IA32_MC14_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0439	0x0439	0x1	IA32_MC14_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x043A	0x043A	0x1	IA32_MC14_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x043B	0x043B	0x1	IA32_MC14_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x043C	0x043C	0x1	IA32_MC15_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x043D	0x043D	0x1	IA32_MC15_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x043E	0x043E	0x1	IA32_MC15_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x043F	0x043F	0x1	IA32_MC15_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0440	0x0440	0x1	IA32_MC16_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0441	0x0441	0x1	IA32_MC16_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0442	0x0442	0x1	IA32_MC16_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0443	0x0443	0x1	IA32_MC16_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0444	0x0444	0x1	IA32_MC17_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0445	0x0445	0x1	IA32_MC17_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0446	0x0446	0x1	IA32_MC17_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0447	0x0447	0x1	IA32_MC17_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0448	0x0448	0x1	IA32_MC18_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0449	0x0449	0x1	IA32_MC18_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x044A	0x044A	0x1	IA32_MC18_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x044B	0x044B	0x1	IA32_MC18_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x044C	0x044C	0x1	IA32_MC19_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x044D	0x044D	0x1	IA32_MC19_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x044E	0x044E	0x1	IA32_MC19_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x044F	0x044F	0x1	IA32_MC19_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0450	0x0450	0x1	IA32_MC20_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0451	0x0451	0x1	IA32_MC20_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0452	0x0452	0x1	IA32_MC20_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0453	0x0453	0x1	IA32_MC20_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0454	0x0454	0x1	IA32_MC21_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0455	0x0455	0x1	IA32_MC21_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0456	0x0456	0x1	IA32_MC21_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0457	0x0457	0x1	IA32_MC21_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0458	0x0458	0x1	IA32_MC22_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0459	0x0459	0x1	IA32_MC22_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x045A	0x045A	0x1	IA32_MC22_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x045B	0x045B	0x1	IA32_MC22_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x045C	0x045C	0x1	IA32_MC23_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x045D	0x045D	0x1	IA32_MC23_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x045E	0x045E	0x1	IA32_MC23_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x045F	0x045F	0x1	IA32_MC23_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0460	0x0460	0x1	IA32_MC24_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0461	0x0461	0x1	IA32_MC24_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0462	0x0462	0x1	IA32_MC24_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0463	0x0463	0x1	IA32_MC24_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0464	0x0464	0x1	IA32_MC25_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0465	0x0465	0x1	IA32_MC25_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0466	0x0466	0x1	IA32_MC25_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0467	0x0467	0x1	IA32_MC25_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0468	0x0468	0x1	IA32_MC26_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0469	0x0469	0x1	IA32_MC26_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x046A	0x046A	0x1	IA32_MC26_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x046B	0x046B	0x1	IA32_MC26_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x046C	0x046C	0x1	IA32_MC27_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x046D	0x046D	0x1	IA32_MC27_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x046E	0x046E	0x1	IA32_MC27_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x046F	0x046F	0x1	IA32_MC27_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0470	0x0470	0x1	IA32_MC28_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0471	0x0471	0x1	IA32_MC28_STATUS	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0472	0x0472	0x1	IA32_MC28_ADDR	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0473	0x0473	0x1	IA32_MC28_MISC	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	

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0x0480	0x0480	0x1	IA32_VMX_BASIC	For L1: Bit 54 (VM exit info on INS/OUTS) = 1 Bit 55(true VMX controls) = 1 Bit 56 (VOE w/o err code) = 1 Bit 58 (Nested Exc.) = virt. CPUID(7,1).EAX[17] Other bits = 0 For L2: inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x0481	0x0481	0x1	IA32_VMX_PINBASED_CTLS	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x0482	0x0482	0x1	IA32_VMX_PROCBASED_CTLS	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x0483	0x0483	0x1	IA32_VMX_EXIT_CTLS	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x0484	0x0484	0x1	IA32_VMX_ENTRY_CTLS	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x0485	0x0485	0x1	IA32_VMX_MISC	For L1: Bit 5 (unrestricted guest) = 1 Bit 6 (HLT activity state) = 1 Bit 7 (shutdown activity state) = 1 Bit 14 (PT in VMX) = 1 Bits 24:16 (CR3 target count) = 4 Bit 29 (VMWRITE any field) = 1 Bit 30 (VOE with 0 inst length) = 1 Other bits = 0 For L2: inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x0486	0x0486	0x1	IA32_VMX_CR0_FIXED0	For L1: See L2 VMCS guest CR0 field description For L2: inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x0487	0x0487	0x1	IA32_VMX_CR0_FIXED1	For L1: See L2 VMCS guest CR0 field description For L2: inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x0488	0x0488	0x1	IA32_VMX_CR4_FIXED0	For L1: See L2 VMCS guest CR4 field description For L2: inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x0489	0x0489	0x1	IA32_VMX_CR4_FIXED1	For L1: See L2 VMCS guest CR4 field description For L2: inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x048A	0x048A	0x1	IA32_VMX_VMCS_ENUM	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x048B	0x048B	0x1	IA32_VMX_PROCBASED_CTLS2	For L1: See L2 VMCS controls 2 field description For L2: inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x048C	0x048C	0x1	IA32_VMX_EPT_VPID_CAP	For L1: Execute-only (bit 0) = 1 2MB pages (bit 16) = 1 1GB pages (bit 17) = 1 A/D (bit 21) = 0 EPT violation info (bit 22) = 1 SSS (bit 23) = XFAM.CET_S (bit 12) HLAT prefix size (bits 53:48) taken from real MSR Other bits = 0 For L2: inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x048D	0x048D	0x1	IA32_VMX_TRUE_PINBASED_CTLS	For L1: See L2 VMCS pinbased controls field description For L2: inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x048E	0x048E	0x1	IA32_VMX_TRUE_PROCBASED_CTLS	For L1: See L2 VMCS procbased controls field description For L2: inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x048F	0x048F	0x1	IA32_VMX_TRUE_EXIT_CTLS	For L1: See L2 VMCS VM exit controls field description For L2: inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x0490	0x0490	0x1	IA32_VMX_TRUE_ENTRY_CTLS	For L1: See L2 VMCS VM entry controls field description For L2: inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x0491	0x0491	0x1	IA32_VMX_VMFUNC	For L1: All-0 For L2: inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x0492	0x0492	0x1	IA32_VMX_PROCBASED_CTLS3	For L1: See L2 VMCS procbased controls3 field description For L2: inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x0493	0x0493	0x1	IA32_VMX_VM_EXIT_CTLS2	For L1: See L2 VMCS VM exit controls2 field description. #GP(0) if not supported. For L2: inject_GP_or_VE(TD_CTLS.REDUCE_VE)	#GP(0)	
0x04C0	0x04C0	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x04C1	0x04C8	0x8	IA32_A_PMCx	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x04D0	0x04D0	0x1	IA32_MCG_EXT_CTL	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	inject_GP_or_VE(~virt. CPUID(1).EDX[14])	
0x0500	0x0500	0x1	IA32_SGX_SVN_STATUS	#GP(0)	#GP(0)	
0x0501	0x0501	0x1	Future IA32_SE_SVN Expansion	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0550	0x0550	0x1	MSR_SEAM_SAI_MODE	#GP(0)	#GP(0)	
0x0551	0x0551	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0560	0x0560	0x1	IA32_RTIT_OUTPUT_BASE	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])	
0x0561	0x0561	0x1	IA32_RTIT_OUTPUT_MASK_PTRS	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])	
0x0570	0x0570	0x1	IA32_RTIT_CTL	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])	
0x0571	0x0571	0x1	IA32_RTIT_STATUS	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])	
0x0572	0x0572	0x1	IA32_RTIT_CR3_MATCH	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])	
0x0580	0x0580	0x1	IA32_RTIT_ADDR0_A	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])	
0x0581	0x0581	0x1	IA32_RTIT_ADDR0_B	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])	
0x0582	0x0582	0x1	IA32_RTIT_ADDR1_A	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])	
0x0583	0x0583	0x1	IA32_RTIT_ADDR1_B	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])	

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0x0584	0x0584	0x1	IA32_RTIT_ADDR2_A	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])	
0x0585	0x0585	0x1	IA32_RTIT_ADDR2_B	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])	
0x0586	0x0586	0x1	IA32_RTIT_ADDR3_A	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])	
0x0587	0x0587	0x1	IA32_RTIT_ADDR3_B	Inject_GP(~XFAM[8])	Inject_GP(~XFAM[8])	
0x05D0	0x05D0	0x1	IA32_MPRR_CAP	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05D1	0x05D1	0x1	IA32_MPRR_EN_ATTR_DEFAULT	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05D2	0x05D2	0x1	IA32_MPRR_LOW_ADDR1	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05D3	0x05D3	0x1	IA32_MPRR_HIGH_ADDR1	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05D4	0x05D4	0x1	IA32_MPRR_EN_ATTR_ATTR1	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05D5	0x05D5	0x1	IA32_MPRR_LOW_ADDR2	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05D6	0x05D6	0x1	IA32_MPRR_HIGH_ADDR2	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05D7	0x05D7	0x1	IA32_MPRR_EN_ATTR_ATTR2	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05D8	0x05D8	0x1	IA32_MPRR_LOW_ADDR3	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05D9	0x05D9	0x1	IA32_MPRR_HIGH_ADDR3	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05DA	0x05DA	0x1	IA32_MPRR_EN_ATTR_ATTR3	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05DB	0x05DB	0x1	IA32_MPRR_LOW_ADDR4	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05DC	0x05DC	0x1	IA32_MPRR_HIGH_ADDR4	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05DD	0x05DD	0x1	IA32_MPRR_EN_ATTR_ATTR4	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05DE	0x05DE	0x1	IA32_MPRR_LOW_ADDR5	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05DF	0x05DF	0x1	IA32_MPRR_HIGH_ADDR5	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05E0	0x05E0	0x1	IA32_MPRR_EN_ATTR_ATTR5	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05E1	0x05E1	0x1	IA32_MPRR_LOW_ADDR6	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05E2	0x05E2	0x1	IA32_MPRR_HIGH_ADDR6	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05E3	0x05E3	0x1	IA32_MPRR_EN_ATTR_ATTR6	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05E4	0x05E4	0x1	IA32_MPRR_LOW_ADDR7	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05E5	0x05E5	0x1	IA32_MPRR_HIGH_ADDR7	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05E6	0x05E6	0x1	IA32_MPRR_EN_ATTR_ATTR7	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05E7	0x05E7	0x1	IA32_MPRR_LOW_ADDR8	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05E8	0x05E8	0x1	IA32_MPRR_HIGH_ADDR8	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05E9	0x05E9	0x1	IA32_MPRR_EN_ATTR_ATTR8	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05EA	0x05EA	0x1	IA32_MPRR_LOW_ADDR9	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05EB	0x05EB	0x1	IA32_MPRR_HIGH_ADDR9	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05EC	0x05EC	0x1	IA32_MPRR_EN_ATTR_ATTR9	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05ED	0x05ED	0x1	IA32_MPRR_LOW_ADDR10	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05EE	0x05EE	0x1	IA32_MPRR_HIGH_ADDR10	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05EF	0x05EF	0x1	IA32_MPRR_EN_ATTR_ATTR10	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05F0	0x05F0	0x1	IA32_MPRR_LOW_ADDR11	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05F1	0x05F1	0x1	IA32_MPRR_HIGH_ADDR11	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05F2	0x05F2	0x1	IA32_MPRR_EN_ATTR_ATTR11	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05F3	0x05F3	0x1	IA32_MPRR_LOW_ADDR12	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05F4	0x05F4	0x1	IA32_MPRR_HIGH_ADDR12	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05F5	0x05F5	0x1	IA32_MPRR_EN_ATTR_ATTR12	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05F6	0x05F6	0x1	IA32_MPRR_LOW_ADDR13	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05F7	0x05F7	0x1	IA32_MPRR_HIGH_ADDR13	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05F8	0x05F8	0x1	IA32_MPRR_EN_ATTR_ATTR13	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05F9	0x05F9	0x1	IA32_MPRR_LOW_ADDR14	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05FA	0x05FA	0x1	IA32_MPRR_HIGH_ADDR14	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05FB	0x05FB	0x1	IA32_MPRR_EN_ATTR_ATTR14	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05FC	0x05FC	0x1	IA32_MPRR_LOW_ADDR15	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x05FD	0x05FD	0x1	IA32_MPRR_HIGH_ADDR15	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0600	0x0600	0x1	IA32_DS_AREA	Native	Native	
0x06A0	0x06A0	0x1	IA32_U_CET	Inject_GP(~(XFAM[11] | XFAM[12]))	Inject_GP(~(XFAM[11] | XFAM[12]))	
0x06A2	0x06A2	0x1	IA32_S_CET	Inject_GP(~(XFAM[11] | XFAM[12]))	Inject_GP(~(XFAM[11] | XFAM[12]))	
0x06A4	0x06A4	0x1	IA32_PL0_SSP	Inject_GP(~(XFAM[11] | XFAM[12] | virt. CPUID(7,1).EAX[17])	Inject_GP(~(XFAM[11] | XFAM[12] | virt. CPUID(7,1).EAX[17])	
0x06A5	0x06A5	0x1	IA32_PL1_SSP	Inject_GP(~(XFAM[11] | XFAM[12]))	Inject_GP(~(XFAM[11] | XFAM[12]))	
0x06A6	0x06A6	0x1	IA32_PL2_SSP	Inject_GP(~(XFAM[11] | XFAM[12]))	Inject_GP(~(XFAM[11] | XFAM[12]))	
0x06A7	0x06A7	0x1	IA32_PL3_SSP	Inject_GP(~(XFAM[11] | XFAM[12]))	Inject_GP(~(XFAM[11] | XFAM[12]))	
0x06A8	0x06A8	0x1	IA32_INTERRUPT_SSP_TABLE_ADDR	Inject_GP(~(XFAM[11] | XFAM[12]))	Inject_GP(~(XFAM[11] | XFAM[12]))	
0x06E0	0x06E0	0x1	IA32_TSC_DEADLINE	inject_GP_or_VE(~virt. CPUID(0x1).ECX[24])	inject_GP_or_VE(~virt. CPUID(0x1).ECX[24])	
0x06E1	0x06E1	0x1	IA32_PKRS	Inject_GP(~PKS)	Inject_GP(~PKS)	
0x0770	0x0770	0x1	IA32_PM_ENABLE	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0771	0x0771	0x1	IA32_HWP_CAPABILITIES	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0772	0x0772	0x1	IA32_HWP_REQUEST_PKG	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0773	0x0773	0x1	IA32_HWP_INTERRUPT	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0774	0x0774	0x1	IA32_HWP_REQUEST	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0775	0x0775	0x1	IA32_HWP_PECI_REQUEST_INFO	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0776	0x0776	0x1	IA32_HWP_CTL	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0777	0x0777	0x1	IA32_HWP_STATUS	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0793	0x0793	0x1	EXTENDED_MCG_PTR	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0800	0x0801	0x2	Reserved for xAPIC MSRs	#GP(0)	#GP(0)	

0x0802	0x0802	0x1	IA32_X2APIC_APICID	if TD_CTLS.ENUM_TOPOLOGY
				  return virtual x2APIC ID
				else
				  #VE(CONFIG_PARAVIRT)
					#GP(0)	

0x0803	0x0803	0x1	IA32_X2APIC_VERSION	#VE	#GP(0)	
0x0804	0x0807	0x4	Reserved for xAPIC MSRs	#GP(0)	#GP(0)	
0x0808	0x0808	0x1	IA32_X2APIC_TPR	Native	Native	

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0x0809	0x0809	0x1	Reserved for xAPIC MSRs	Native	Native	
0x080A	0x080A	0x1	IA32_X2APIC_PPR	Native	Native	
0x080B	0x080B	0x1	IA32_X2APIC_EOI	Native	Native	
0x080C	0x080C	0x1	Reserved for xAPIC MSRs	Native	Native	
0x080D	0x080D	0x1	IA32_X2APIC_LDR	#VE	#GP(0)	
0x080E	0x080E	0x1	Reserved for xAPIC MSRs	Native	Native	
0x080F	0x080F	0x1	IA32_X2APIC_SIVR	#VE	#VE	#VE
0x0810	0x0817	0x8	IA32_X2APIC_ISRx	Native	Native	
0x0818	0x081F	0x8	IA32_X2APIC_TMRx	Native	Native	
0x0820	0x0827	0x8	IA32_X2APIC_IRRx	Native	Native	
0x0828	0x0828	0x1	IA32_X2APIC_ESR	#VE	#VE	#VE
0x0829	0x082E	0x6	Reserved for xAPIC MSRs	#GP(0)	#GP(0)	
0x082F	0x082F	0x1	IA32_X2APIC_LVT_CMCI	#VE	#VE	#VE
0x0830	0x0830	0x1	IA32_X2APIC_ICR	Native	Native	
0x0831	0x0831	0x1	Reserved for xAPIC MSRs	#GP(0)	#GP(0)	
0x0832	0x0832	0x1	IA32_X2APIC_LVT_TIMER	#VE	#VE	#VE
0x0833	0x0833	0x1	IA32_X2APIC_LVT_THERMAL	#VE	#VE	#VE
0x0834	0x0834	0x1	IA32_X2APIC_LVT_PMI	#VE	#VE	#VE
0x0835	0x0835	0x1	IA32_X2APIC_LVT_LINT0	#VE	#VE	#VE
0x0836	0x0836	0x1	IA32_X2APIC_LVT_LINT1	#VE	#VE	#VE
0x0837	0x0837	0x1	IA32_X2APIC_LVT_ERROR	#VE	#VE	#VE
0x0838	0x0838	0x1	IA32_X2APIC_INIT_COUNT	#VE	#VE	#VE
0x0839	0x0839	0x1	IA32_X2APIC_CUR_COUNT	#VE	#GP(0)	
0x083A	0x083A	0x1	IA32_X2APIC_LVT_HWP	#VE	#VE	#VE
0x083B	0x083D	0x3	Reserved for xAPIC MSRs	#GP(0)	#GP(0)	
0x083E	0x083E	0x1	IA32_X2APIC_DIV_CONF	#VE	#VE	#VE
0x083F	0x083F	0x1	IA32_X2APIC_SELF_IPI	Native	Native	
0x0840	0x087F	0x40	Reserved for xAPIC MSRs	#GP(0)	#GP(0)	
0x0880	0x08BF	0x40	Reserved for xAPIC MSRs	#GP(0)	#GP(0)	
0x08C0	0x08FF	0x40	Reserved for xAPIC MSRs	#GP(0)	#GP(0)	
0x0980	0x0980	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0981	0x0981	0x1	IA32_TME_CAPABILITY	Inject_GP_or_VE (~virt. CPUID(7,0).ECX[13])	Inject_GP_or_VE (~virt. CPUID(7,0).ECX[13])	
0x0982	0x0982	0x1	IA32_TME_ACTIVATE	Inject_GP_or_VE (~virt. CPUID(7,0).ECX[13])	Inject_GP_or_VE (~virt. CPUID(7,0).ECX[13])	
0x0983	0x0983	0x1	IA32_TME_EXCLUDE_MASK	Inject_GP_or_VE (~virt. CPUID(7,0).ECX[13])	Inject_GP_or_VE (~virt. CPUID(7,0).ECX[13])	
0x0984	0x0984	0x1	IA32_TME_EXCLUDE_BASE	Inject_GP_or_VE (~virt. CPUID(7,0).ECX[13])	Inject_GP_or_VE (~virt. CPUID(7,0).ECX[13])	
0x0985	0x0985	0x1	IA32_UINTR_RR	Inject_GP(~XFAM[14])	Inject_GP(~XFAM[14])	
0x0986	0x0986	0x1	IA32_UINTR_HANDLER	Inject_GP(~XFAM[14])	Inject_GP(~XFAM[14])	
0x0987	0x0987	0x1	IA32_UINTR_STACKADJUST	Inject_GP(~XFAM[14])	Inject_GP(~XFAM[14])	
0x0988	0x0988	0x1	IA32_UINTR_MISC	Inject_GP(~XFAM[14])	Inject_GP(~XFAM[14])	
0x0989	0x0989	0x1	IA32_UINTR_PD	Inject_GP(~XFAM[14])	Inject_GP(~XFAM[14])	
0x098A	0x098A	0x1	IA32_UINTR_TT	Inject_GP(~XFAM[14])	Inject_GP(~XFAM[14])	
0x098B	0x098B	0x1	IA32_MPRR-High-ADDR15	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x098C	0x098C	0x1	IA32_MPRR_EN_ATTR15	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x098D	0x098D	0x1	IA32_MPRR-Low-ADDR16	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x098E	0x098E	0x1	IA32_MPRR-High-ADDR16	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x098F	0x098F	0x1	IA32_MPRR_EN_ATTR16	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0990	0x0990	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0991	0x0991	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x09A0	0x09A3	0x4	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x09C0	0x09C3	0x4	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x09E0	0x09E7	0x8	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x09F0	0x09F7	0x8	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x09FD	0x09FD	0x1	TSX_STORE_ADDRESS	#GP(0)	#GP(0)	
0x0A80	0x0AFF	0x80	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0B00	0x0B7F	0x80	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0B80	0x0BFF	0x80	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0C80	0x0C80	0x1	IA32_DEBUG_INTERFACE	#GP(0)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0C81	0x0C81	0x1	IA32_L3_QOS_CFG	inject_GP_or_VE(~virt. CPUID(7,0).EBX[15])	inject_GP_or_VE(~virt. CPUID(7,0).EBX[15])	
0x0C82	0x0C82	0x1	IA32_L2_QOS_CFG	inject_GP_or_VE(~virt. CPUID(7,0).EBX[15])	inject_GP_or_VE(~virt. CPUID(7,0).EBX[15])	
0x0C8D	0x0C8D	0x1	IA32_QM_EVTSEL	inject_GP_or_VE(~virt. CPUID(7,0).EBX[12])	inject_GP_or_VE(~virt. CPUID(7,0).EBX[12])	
0x0C8E	0x0C8E	0x1	IA32_QM_CTR	inject_GP_or_VE(~virt. CPUID(7,0).EBX[12])	inject_GP_or_VE(~virt. CPUID(7,0).EBX[12])	
0x0C8F	0x0C8F	0x1	IA32_PQR_ASSOC	inject_GP_or_VE(~virt. CPUID(7,0).EBX[12])	inject_GP_or_VE(~virt. CPUID(7,0).EBX[12])	
0x0C90	0x0D0F	0x80	IA32_L3_QOS_MASK_x	inject_GP_or_VE(~virt. CPUID(7,0).EBX[15])	inject_GP_or_VE(~virt. CPUID(7,0).EBX[15])	
0x0D10	0x0D4F	0x40	IA32_L2_QOS_MASK_x	inject_GP_or_VE(~virt. CPUID(7,0).EBX[15])	inject_GP_or_VE(~virt. CPUID(7,0).EBX[15])	
0x0D50	0x0D8F	0x40	IA32_L2_QOS_Ext_BW_Thrtl_x	inject_GP_or_VE(~virt. CPUID(7,0).EBX[15])	inject_GP_or_VE(~virt. CPUID(7,0).EBX[15])	
0x0D90	0x0D90	0x1	IA32_BNDCFGS	#GP(0)	#GP(0)	
0x0D91	0x0D91	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0D92	0x0D92	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0D93	0x0D93	0x1	IA32_PASID	#GP(0)	#GP(0)	

0x0DA0	0x0DA0	0x1	IA32_XSS	Native	if invalid or does not match XFAM
					  #GP(0)
					else
					  Write to CPU	

0x0DB0	0x0DB0	0x1	IA32_PKG_HDC_CTL	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0DB1	0x0DB1	0x1	IA32_PM_CTL1	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0DB2	0x0DB2	0x1	IA32_THREAD_STALL	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x0DC0	0x0DFF	0x40	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1000	0x1000	0x1	IA32_MPX_LAX	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	

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0x1200	0x12FF	0x100	IA32_LBR_INFO	Inject_GP(~XFAM[15])	Inject_GP(~XFAM[15])	
0x1309	0x130B	0x3	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1400	0x1400	0x1	IA32_SEAMRR_BASE	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1401	0x1401	0x1	IA32_SEAMRR_MASK	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1402	0x1402	0x1	IA32_SEAM_EXTEND	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x14C1	0x14C8	0x8	IA32_RELOAD_PMCx	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x14CE	0x14CE	0x1	IA32_LBR_CTL	Inject_GP(~XFAM[15])	Inject_GP(~XFAM[15])	
0x14CF	0x14CF	0x1	IA32_LBR_DEPTH	Inject_GP(~XFAM[15])	Inject_GP(~XFAM[15])	
0x1500	0x15FF	0x100	IA32_LBR_x_FROM_IP	Inject_GP(~XFAM[15])	Inject_GP(~XFAM[15])	
0x1600	0x16FF	0x100	IA32_LBR_x_TO_IP	Inject_GP(~XFAM[15])	Inject_GP(~XFAM[15])	
0x17D0	0x17D0	0x1	IA32_HW_FEEDBACK_PTR	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x17D1	0x17D1	0x1	IA32_HW_FEEDBACK_CONFIG	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x17D2	0x17D2	0x1	IA32_THREAD_FEEDBACK_CHAR	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x17D4	0x17D4	0x1	IA32_HW_FEEDBACK_THREAD_CONFIG	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x17DA	0x17DA	0x1	IA32_HRESET_ENABLE	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1900	0x1900	0x1	IA32_PMC_GP0_CTR	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	

0x1901	0x1901	0x1	IA32_PMC_GP0_CFG_A	if (~PERFMON)
				  #GP(0)
				else if (EVENT_FILTERS_NUM > 0)
				  Special event filtering
					if (~PERFMON)
					  #GP(0)
					else if ((EN_LBR_LOG(bit 35) == 1) && (virt.
					CPUID(0x1C).ECX[16+x] == 0))
					  #GP(0)
					else if (EVENT_FILTERS_NUM > 0)
					  Special event filtering	

0x1902	0x1902	0x1	IA32_PMC_GP0_CFG_B	#GP(0)	#GP(0)	
0x1903	0x1903	0x1	IA32_PMC_GP0_CFG_C	Inject_GP(~virt CPUID(0x23,5).EAX[0])	Inject_GP(~virt CPUID(0x23,5).EAX[0])	
0x1904	0x1904	0x1	IA32_PMC_GP1_CTR	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	

0x1905	0x1905	0x1	IA32_PMC_GP1_CFG_A	if (~PERFMON)
				  #GP(0)
				else if (EVENT_FILTERS_NUM > 0)
				  Special event filtering
					if (~PERFMON)
					  #GP(0)
					else if ((EN_LBR_LOG(bit 35) == 1) && (virt.
					CPUID(0x1C).ECX[16+x] == 0))
					  #GP(0)
					else if (EVENT_FILTERS_NUM > 0)
					  Special event filtering	

0x1906	0x1906	0x1	IA32_PMC_GP1_CFG_B	#GP(0)	#GP(0)	
0x1907	0x1907	0x1	IA32_PMC_GP1_CFG_C	Inject_GP(~virt CPUID(0x23,5).EAX[1])	Inject_GP(~virt CPUID(0x23,5).EAX[1])	
0x1908	0x1908	0x1	IA32_PMC_GP2_CTR	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	

0x1909	0x1909	0x1	IA32_PMC_GP2_CFG_A	if (~PERFMON)
				  #GP(0)
				else if (EVENT_FILTERS_NUM > 0)
				  Special event filtering
					if (~PERFMON)
					  #GP(0)
					else if ((EN_LBR_LOG(bit 35) == 1) && (virt.
					CPUID(0x1C).ECX[16+x] == 0))
					  #GP(0)
					else if (EVENT_FILTERS_NUM > 0)
					  Special event filtering	

0x190A	0x190A	0x1	IA32_PMC_GP2_CFG_B	#GP(0)	#GP(0)	
0x190B	0x190B	0x1	IA32_PMC_GP2_CFG_C	Inject_GP(~virt CPUID(0x23,5).EAX[2])	Inject_GP(~virt CPUID(0x23,5).EAX[2])	
0x190C	0x190C	0x1	IA32_PMC_GP3_CTR	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	

0x190D	0x190D	0x1	IA32_PMC_GP3_CFG_A	if (~PERFMON)
				  #GP(0)
				else if (EVENT_FILTERS_NUM > 0)
				  Special event filtering
					if (~PERFMON)
					  #GP(0)
					else if ((EN_LBR_LOG(bit 35) == 1) && (virt.
					CPUID(0x1C).ECX[16+x] == 0))
					  #GP(0)
					else if (EVENT_FILTERS_NUM > 0)
					  Special event filtering	

0x190E	0x190E	0x1	IA32_PMC_GP3_CFG_B	#GP(0)	#GP(0)	
0x190F	0x190F	0x1	IA32_PMC_GP3_CFG_C	Inject_GP(~virt CPUID(0x23,5).EAX[3])	Inject_GP(~virt CPUID(0x23,5).EAX[3])	
0x1910	0x1910	0x1	IA32_PMC_GP4_CTR	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	

0x1911	0x1911	0x1	IA32_PMC_GP4_CFG_A	if (~PERFMON)
				  #GP(0)
				else if (EVENT_FILTERS_NUM > 0)
				  Special event filtering
					if (~PERFMON)
					  #GP(0)
					else if ((EN_LBR_LOG(bit 35) == 1) && (virt.
					CPUID(0x1C).ECX[16+x] == 0))
					  #GP(0)
					else if (EVENT_FILTERS_NUM > 0)
					  Special event filtering	

0x1912	0x1912	0x1	IA32_PMC_GP4_CFG_B	#GP(0)	#GP(0)	
0x1913	0x1913	0x1	IA32_PMC_GP4_CFG_C	Inject_GP(~virt CPUID(0x23,5).EAX[4])	Inject_GP(~virt CPUID(0x23,5).EAX[4])	
0x1914	0x1914	0x1	IA32_PMC_GP5_CTR	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	

0x1915	0x1915	0x1	IA32_PMC_GP5_CFG_A	if (~PERFMON)
				  #GP(0)
				else if (EVENT_FILTERS_NUM > 0)
				  Special event filtering
					if (~PERFMON)
					  #GP(0)
					else if ((EN_LBR_LOG(bit 35) == 1) && (virt.
					CPUID(0x1C).ECX[16+x] == 0))
					  #GP(0)
					else if (EVENT_FILTERS_NUM > 0)
					  Special event filtering	

0x1916	0x1916	0x1	IA32_PMC_GP5_CFG_B	#GP(0)	#GP(0)	
0x1917	0x1917	0x1	IA32_PMC_GP5_CFG_C	Inject_GP(~virt CPUID(0x23,5).EAX[5])	Inject_GP(~virt CPUID(0x23,5).EAX[5])	
0x1918	0x1918	0x1	IA32_PMC_GP6_CTR	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	

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0x1919	0x1919	0x1	IA32_PMC_GP6_CFG_A	if (~PERFMON) #GP(0) else if (EVENT_FILTERS_NUM > 0) Special event filtering	if (~PERFMON) #GP(0) else if ((EN_LBR_LOG(bit 35) == 1) && (virt. CPUID(0x1C).ECX[16+x] == 0)) #GP(0) else if (EVENT_FILTERS_NUM > 0) Special event filtering	
0x191A	0x191A	0x1	IA32_PMC_GP6_CFG_B	#GP(0)	#GP(0)	
0x191B	0x191B	0x1	IA32_PMC_GP6_CFG_C	Inject_GP(~virt CPUID(0x23,5).EAX[6])	Inject_GP(~virt CPUID(0x23,5).EAX[6])	
0x191C	0x191C	0x1	IA32_PMC_GP7_CTR	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x191D	0x191D	0x1	IA32_PMC_GP7_CFG_A	if (~PERFMON) #GP(0) else if (EVENT_FILTERS_NUM > 0) Special event filtering	if (~PERFMON) #GP(0) else if ((EN_LBR_LOG(bit 35) == 1) && (virt. CPUID(0x1C).ECX[16+x] == 0)) #GP(0) else if (EVENT_FILTERS_NUM > 0) Special event filtering	
0x191E	0x191E	0x1	IA32_PMC_GP7_CFG_B	#GP(0)	#GP(0)	
0x191F	0x191F	0x1	IA32_PMC_GP7_CFG_C	Inject_GP(~virt CPUID(0x23,5).EAX[7])	Inject_GP(~virt CPUID(0x23,5).EAX[7])	
0x1920	0x1920	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1921	0x1921	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1922	0x1922	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1923	0x1923	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1924	0x1924	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1925	0x1925	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1926	0x1926	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1927	0x1927	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1980	0x1980	0x1	IA32_PMC_FX0_CTR	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x1981	0x1981	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1982	0x1982	0x1	IA32_PMC_FX0_CFG_B	#GP(0)	#GP(0)	
0x1983	0x1983	0x1	IA32_PMC_FX0_CFG_C	Inject_GP(~virt CPUID(0x23,5).ECX[0])	Inject_GP(~virt CPUID(0x23,5).ECX[0])	
0x1984	0x1984	0x1	IA32_PMC_FX1_CTR	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x1985	0x1985	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1986	0x1986	0x1	IA32_PMC_FX1_CFG_B	#GP(0)	#GP(0)	
0x1987	0x1987	0x1	IA32_PMC_FX1_CFG_C	Inject_GP(~virt CPUID(0x23,5).ECX[1])	Inject_GP(~virt CPUID(0x23,5).ECX[1])	
0x1988	0x1988	0x1	IA32_PMC_FX2_CTR	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x1989	0x1989	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x198A	0x198A	0x1	IA32_PMC_FX2_CFG_B	#GP(0)	#GP(0)	
0x198B	0x198B	0x1	IA32_PMC_FX2_CFG_C	Inject_GP(~virt CPUID(0x23,5).ECX[2])	Inject_GP(~virt CPUID(0x23,5).ECX[2])	
0x198C	0x198C	0x1	IA32_PMC_FX3_CTR	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x198D	0x198D	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x198E	0x198E	0x1	IA32_PMC_FX3_CFG_B	#GP(0)	#GP(0)	
0x198F	0x198F	0x1	IA32_PMC_FX3_CFG_C	Inject_GP(~virt CPUID(0x23,5).ECX[3])	Inject_GP(~virt CPUID(0x23,5).ECX[3])	
0x1990	0x1990	0x1	IA32_PMC_FX4_CTR	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x1991	0x1991	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1992	0x1992	0x1	IA32_PMC_FX4_CFG_B	#GP(0)	#GP(0)	
0x1993	0x1993	0x1	IA32_PMC_FX4_CFG_C	Inject_GP(~virt CPUID(0x23,5).ECX[4])	Inject_GP(~virt CPUID(0x23,5).ECX[4])	
0x1994	0x1994	0x1	IA32_PMC_FX5_CTR	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x1995	0x1995	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x1996	0x1996	0x1	IA32_PMC_FX5_CFG_B	#GP(0)	#GP(0)	
0x1997	0x1997	0x1	IA32_PMC_FX5_CFG_C	Inject_GP(~virt CPUID(0x23,5).ECX[5])	Inject_GP(~virt CPUID(0x23,5).ECX[5])	
0x1998	0x1998	0x1	IA32_PMC_FX6_CTR	Inject_GP(~PERFMON)	Inject_GP(~PERFMON)	
0x1999	0x1999	0x1	Reserved	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	inject_GP_or_VE(TD_CTLS.REDUCE_VE)	
0x199A	0x199A	0x1	IA32_PMC_FX6_CFG_B	#GP(0)	#GP(0)	
0x199B	0x199B	0x1	IA32_PMC_FX6_CFG_C	Inject_GP(~virt CPUID(0x23,5).ECX[6])	Inject_GP(~virt CPUID(0x23,5).ECX[6])	
0x1B01	0x1B01	0x1	IA32_UARCH_MISC_CTL	Native	Native	
0xC0000080	0xC0000080	0x1	IA32_EFER	Native	If TD Partitioning is supported: - Ignore read-only bit LMA (10) - Allow update of bit SCE (0) - For L2, allow update of bit LME (8) - #VE(UNSUPPORTED_FEATURE) on any other change Else: - #VE(UNSUPPORTED_FEATURE)	
0xC0000081	0xC0000081	0x1	IA32_STAR	Native	Native	
0xC0000082	0xC0000082	0x1	IA32_LSTAR	Native	Native	
0xC0000083	0xC0000083	0x1	IA32_CSTAR	#VE	#VE	#VE
0xC0000084	0xC0000084	0x1	IA32_FMASK	Native	Native	
0xC0000100	0xC0000100	0x1	IA32_FSBASE	Native	Native	
0xC0000101	0xC0000101	0x1	IA32_GSBASE	Native	Native	
0xC0000102	0xC0000102	0x1	IA32_KERNEL_GS_BASE	Native	Native	
0xC0000103	0xC0000103	0x1	IA32_TSC_AUX	Native	Native	

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