Intel® Processors based on Gracemont Microarchitecture

Instruction Throughput and Latency

February 2022

Revision 1.0

350391-001US

Revision History		
Document ID	**Description**	**Date**
350391-001	Initial Release	Feb-22

Notices & Disclaimers

Instruction	Throughput	Throughput VEX256	Latency	MSROM
ADC/SBB r32, imm8	0.5		2	N
ADC/SBB r32, r32	0.5		2	N
ADC/SBB r64, r64	0.5		2	N
ADCX/ADOX r32, r32	0.5		2	N
ADCX/ADOX r64, r64	0.5		2	N
ADD/AND/CMP/OR/SUB/XOR/TEST r32, r32	0.25		1	N
ADD/AND/CMP/OR/SUB/XOR/TEST r64, r64	0.25		1	N
ADDPD/ADDSUBPD/MAXPD/MINPD/SUBPD xmm, xmm	0.5	1	3	N
ADDPS/ADDSD/ADDSS/ADDSUBPS/SUBPS/SUBSD/SUBSS	0.5	1	3	N
MAXPS/MAXSD/MAXSS/MINPS/MINSD/MINSS xmm, xmm	0.5	1	3	N
ANDNPD/ANDNPS/ANDPD/ANDPS/ORPD/ORPS/XORPD/XORPS	0.33	0.66	1	N
AESDEC/AESDECLAST/AESENC/AESENCLAST	0.5	1	3(between AES)/ 4	N
AESIMC/AESKEYGEN	0.5	1	3(between AES)/ 4	N
BEXTR r32, r32, r32	1		4	N
BEXTR r64, r64, r64	1		4	N
BLENDPD/BLENDPS xmm, xmm, imm8	0.33	0.66	1	N
BLENDVPD/BLENDVPS xmm, xmm, <xmm0> VBLENDVPD/PS ymm, ymm, ymm, ymm	0.5	4	3	N Y
BLSI r32, r32, r32	1		3	N
BLSI r64, r64, r64	1		3	N
BLSMSK r32, r32, r32	1		3	N
BLSMSK r64, r64, r64	1		3	N
BLSR r32, r32, r32	1		3	N
BLSR r64, r64, r64	1		3	N
BSF/BSR r32, r32	1		3	Y
BSF/BSR r64, r64	1		3	Y
BSWAP r32	0.25		1	N
BSWAP r64	0.25		1	N
BT r32, r32	0.25		1	N
BT r64, r64	0.25		1	N
BTC/BTR/BTS r32, r32	0.5		1	N
BTC/BTR/BTS r64, r64	0.5		1	N
BZHI r32, r32, r32	1		3	N
BZHI r64, r64, r64	1		3	N
CBW/CWDE/CDQE	0.25		1	N
CWD	4		2	Y
CDQ/CQO/CLC/CMC	0.25		1	N
CMOVxx r32, r32	0.5		2	N
CMPPD xmm, xmm, imm	0.5	1	3	N
CMPSD/CMPPS/CMPSS xmm, xmm, imm	0.5	1	3	N
CMPXCHG r32, r32	5		5	Y
CMPXCHG r64, r64	5		5	Y
(U)COMISD/(U)COMISS xmm, xmm	1		5	N
CPUID	~58		~58	Y
CRC32 r32, r32	1		3	N
CRC32 r64, r64	1		3	N
CVTDQ2PD/CVTDQ2PS/CVTPD2DQ/CVTPD2PS xmm, xmm	1	2	4	N
CVT(T)PD2PI mm, xmm	1		4	N
CVT(T)PI2PD xmm, mm	1		4	N
CVT(T)PS2DQ xmm, xmm	1	2	4	N
CVTPS2PD xmm, xmm	1	2	4	N
CVT(T)SD2SS/CVTSS2SD xmm, xmm	1		4	N
CVTSI2SD/SS xmm, r32	1		7	N
CVTSD2SI/SS2SI r32, xmm	1		5	N
DEC/INC r32	0.5		1	N
DEC/INC r64	0.5		1	N
DIV r8	4.5-6		9-12	N
DIV r16	4.5-8.5		10-17	Y
DIV r32	4.5-12.5		10-25	Y
DIV r64	4.5-20.5		10-41	Y
DIVPD	16	32	21	N
DIVPS	10	20	15	N
DIVSD	8	16	13	N
DIVSS	5	10	10	N
DPPD xmm, xmm, imm	4	4	10	Y
DPPS xmm, xmm, imm	6	6	16	Y
EMMS	~23		~23	Y
EXTRACTPS r32, xmm	1		5	N
F2XM1	~87		~87	Y
FABS/FCHS	0.5		1	N
FCOM	1		3	N
FADD/FSUB	1		3	N
FCOS	~154		~154	Y
FDECSTP/FINCSTP	0.5		1	N
FDIV	5(SP)/8(DP)/9(EP)		10(SP)/13(DP)/14(EP)	N
FLDZ	1		4	N
FMUL	2		5	N
FPATAN/FYL2X/FYL2XP1	~303		~303	Y
FPTAN/FSINCOS	~287		~287	Y
FRNDINT	~41		~41	Y
FSCALE	~32		~32	Y
FSIN	~140		~140	Y
FSQRT	6(SP)/12(DP)/14(EP)		11(SP)/17(DP)/19(EP)	N
GF2P8AFFINEQB/GF2P8AFFINEINVQB	0.5	1	4	N
GF2P8MULB	1	2	4	N
HADDPD/HSUBPD xmm, xmm	5	5	5	Y
HADDPS/HSUBPS xmm, xmm	6	6	6	Y
IDIV r8	4.5-6		9-12	N
IDIV r16	4.5-8.5		9-17	Y
IDIV r32	4.5-12.5		9-25	Y
IDIV r64	4.5-20.5		9-41	Y
IMUL r32, r32 (single dest)	0.5		3	N
IMUL r32 (dual dest)	1		3 (4, EDX)	N
IMUL r64, r64 (single dest)	0.5		5	N
IMUL r64 (dual dest)	1		5 (6,RDX)	N
INSERTPS xmm, xmm, imm8	0.33		1	N
LZCNT r32, r32	1		3	N
LZCNT r64, r64	1		3	N

MASKMOVDQU xmm, xmm	4		n/a store to memory	Y
MOVAPD/MOVAPS/MOVDQA/MOVDQU/MOVUPD/MOVUPS xmm, xmm;	0.25[1]/0.33	0.66	0/1	N
MOVBE	0.25		1	N
MOVD r32, xmm; MOVQ r64, xmm	1		5	N
MOVD xmm, r32 ; MOVQ xmm, r64	1		4	N
MOVDDUP/MOVSHDUP/MOVSLDUP xmm, xmm	0.33	0.66	1	N
MOVHLPS/MOVLHPS/MOVLPD/MOVLPS xmm,xmm	0.33		1	N
MOVDQ2Q/MOVQ/MOVQ2DQ	0.33		1	N
MOVSD/MOVSS xmm, xmm	0.33		1	N
MPSADBW	4	4	5	Y
MUL r32 (dual dest)	1		3 (4, EDX)	N
MUL r64 (dual dest)	1		5 (6,RDX)	N
MULX r32,r32,r32	0.5		3	N
MULX r64,r64,r64	0.5		5	N
MULPD xmm,xmm	0.5	1	4	N
MULPS xmm,xmm	0.5	1	4	N
MULSS/MULSD xmm, xmm	0.5		4	N
NEG/NOT r32	0.25		1	N
NEG/NOT r64	0.25		1	N
PACKSSDW/WB xmm, xmm; PACKUSWB xmm, xmm	0.33	0.66	1	N
PABSB/D/W xmm, xmm	0.33	0.66	1	N
PADDB/D/W xmm, xmm; PSUBB/D/W xmm, xmm	0.33	0.66	1	N
PADDQ/PSUBQ/PCMPEQQ xmm, xmm	0.33	0.66	1	N
PADDSB/W; PADDUSB/W; PSUBSB/W; PSUBUSB/W	0.33	0.66	1	N
PALIGNR xmm, xmm	0.33	0.66	1	N
PAND/PANDN/POR/PXOR xmm, xmm	0.33	0.66	1	N
PAVGB/W xmm, xmm	0.33	0.66	1	N
PBLENDW xmm, xmm, imm	0.33	0.66	1	N
PBLENDVB xmm, xmm, <xmm0>	0.5	1	3	N
PCLMULQDQ xmm, xmm, imm	1	2	4	N
PCMPEQB/D/W xmm, xmm	0.33	0.66	1	N
PCMPEQQ xmm,xmm	1	2	4	N
PCMPESTRI xmm, xmm, imm	8		16(C)/ 17(F)[2]	Y
PCMPESTRM xmm, xmm, imm	8		11(X)/ 16(F)[2]	Y
PCMPGTB/D/W xmm, xmm	0.33		1	N
PCMPGTQ/PHMINPOSUW xmm, xmm	1		4	N
PCMPISTRI xmm, xmm, imm	8		11(C)/ 12(F)[2]	Y
PCMPISTRM xmm, xmm, imm	8		6(X)/ 11(F)[2]	Y
PDEP r32, r32, r32	1		3	N
PDEP r64, r64, r64	1		3	N
PEXT r32, r32, r32	1		3	N
PEXT r64, r64, r64	1		3	N
PEXTRB/D/Q r8/r32/r64, xmm, imm	1		5	N
PEXTRW r32, xmm, imm	1		5	N
PINSRB/D/Q xmm, r8/r32/r64, imm	1		4	N
PINSRW xmm, r32, imm	1		4	N
PHADDD/PHSUBD xmm, xmm	4	4	4	Y
PHADDW/PHADDSW xmm,xmm	6	6	6	Y
PHSUBW/PHSUBSW xmm, xmm	6	6	6	Y
PMADDUBSW/PMADDWD/PMULHRSW/PSADBW xmm, xmm	0.5	1	4	N
PMAXSB/W/D xmm, xmm; PMAXUB/W/D xmm, xmm	0.33	0.66	1	N
PMINSB/W/D xmm, xmm; PMINUB/W/D xmm, xmm	0.33	0.66	1	N
PMOVMSKB r32, xmm	1		5	N
PMOVSXBW/BD/BQ/WD/WQ/DQ xmm, xmm	0.33	0.66	1	N
PMOVZXBW/BD/BQ/WD/WQ/DQ xmm, xmm	0.33	0.66	1	N
PMULDQ/PMULUDQ xmm, xmm	0.5	1	3	N
PMULHUW/PMULHW/PMULLW xmm, xmm	0.5	1	3	N
PMULLD xmm, xmm	1	2	4	N
POPCNT r32, r32	1		3	N
POPCNT r64, r64	1		3	N
PSHUFB xmm, xmm	1	2	1	N
PSHUFD xmm, mem, imm	0.33	0.66	1	N
PSHUFHW; PSHUFLW; PSHUFW	0.33	0.66	1	N
PSIGNB/D/W xmm, xmm	0.33	0.66	1	N
PSLLDQ/PSRLDQ xmm, imm; SHUFPD/SHUFPS	0.33	0.66	1	N
PSLLD/Q/W xmm, xmm	0.33	0.66	1	N
PSRAD/W xmm, imm;	0.33	0.66	1	N
PSRAD/W xmm, xmm;	0.33	0.66	1	N
PSRLD/Q/W xmm, imm;	0.33	0.66	1	N
PSRLD/Q/W xmm, xmm	0.33	0.66	1	N
PTEST xmm, xmm (update eflags)	1	1	5(xmm), 7(ymm)	N
PUNPCKHBW/DQ/WD; PUNPCKLBW/DQ/WD	0.33	0.66	1	N
PUNPCKHQDQ; PUNPCKLQDQ	0.33	0.66	1	N
RCPPS/RSQRTPS	2	4	5	N
RCPSS/RSQRTSS	1	2	4	N
RDTSC	20		20	Y
ROUNDPD/PS	1	2	4	N
ROUNDSD/SS	1		4	N
ROL; ROR; SAL; SAR; SHL; SHR (count in CL)	0.25		1 (2 for CL source)	N
ROL; ROR; SAL; SAR; SHL; SHR (count in imm8)	0.25		1	N
SHA1MSG1/SHA1MSG2/SHA1NEXTE	1		3	N
SHA1RNDS4 xmm, xmm, imm	1		4	N
SHA256MSG1/SHA256MSG2	1		3	N
SHA256RNDS2	2		3	N
SAHF	0.25		1	N
SARX/SHLX/SHRX/RORX r32, r32, r32	0.25		1 (2 for shift count)	N
SHLD r32, r32, imm	0.5		2	N
SHRD r32, r32, imm	0.5		2	N
SHLD/SHRD r64, r64, imm	12		12	Y
SHLD/SHRD r64, r64, CL	14		14	Y
SHLD/SHRD r32, r32, CL	4		4	Y
SHUFPD/SHUFPS xmm, xmm, imm	0.33	0.66	1	N
SQRTPD	24	48	29	N
SQRTPS	12	24	17	N
SQRTSD	12	24	17	N

SQRTSS	6	12	11	N
TEST r32, r32	0.25		1	N
TZCNT r32, r32	1		3	N
TZCNT r64, r64	1		3	N
UNPCKHPD; UNPCKHPS; UNPCKLPD, UNPCKLPS	0.33	0.66	1	N
VBROADCAST reg VBROADCAST mem	0.33 0.5	0.66 1	1 1	N
VCVTPH2PS	1	2	4	N
VCVTPS2PH	1	1	4	N
VEXTRACTI128/F128 xmm, ymm, imm8	n/a	0.33	1	N
VF(N)MADD/SUB	0.5	1	6	N
VGATHER*PS	~30	~50	~50	Y
VGATHER*PD	~20	~30	~30	Y
VINSERT ymm, ymm, xmm, imm8	n/a	0.66	1	N
VPMASKMOV/VMASKMOV (load)	1	2	load latency +1	N
VPMASKMOV/VMASKMOV (store)	1	2	4+store latency	N
VPMOVMSKB r64, ymm	n/a	1	5	N
VPBLENDD	0.33	0.66	1	N
VPERMILPS/PD	0.33	0.66	1	N
VPERMPS/PD; VPERMD/Q	n/a	2	7	N
VPSLLVD/Q; VPSRAVD; VPSRLVQ	0.33	0.66	1	N
VTESTPD/PS	1		3 (xmm source), 7 (ymm source)	N
VZEROALL/VZEROUPPER	5	5	0	N
XADD r32, r32	4		4	Y
XCHG r32, r32	5		5	Y
XCHG r64, r64	5		5	Y

[1]Throughput is 0.25 cycles if move elimination is effect, otherwise 0.33 cycle.
[2]Latency values are for ECX/EFLAGS/XMM0 dependency: (C/F/X)