

Intel® Thread Director and CPPC Compatibility

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Revision History

Revision	Description	Date
1.0	Initial release.	October 2026

CHAPTER 1
INTEL® THREAD DIRECTOR AND CPPC BACKGROUND

Intel® Thread Director helps monitor and analyze performance data in real time to seamlessly place the right application thread on the right core and optimize performance per watt. It supplies the behind-the-scenes magic that maximizes hybrid performance.

Built directly into the hardware, Intel Thread Director uses machine learning to schedule tasks on the right core at the right time (as opposed to relying on static rules). This helps ensure that Performance-cores and Efficient-cores work in concert, background tasks don't slow you down, and you can have more apps open simultaneously.

Intel Thread Director:

- Monitors the runtime instruction mix of each thread and the state of each core with nanosecond precision.
- Provides runtime feedback to the OS to make the optimal decision for any workload.
- Dynamically adapts its guidance according to the Thermal Design Point (TDP) of the system, operating conditions, and power settings.

The Intel Thread Director provides hints to the OS scheduler with thread-related information. Using these hints, the OS can choose between energy efficiency (EE) and performance (PERF) depending on system parameters like power policy, battery slider, etc. This performance and efficiency depend greatly on the software profile and microarchitecture capabilities.

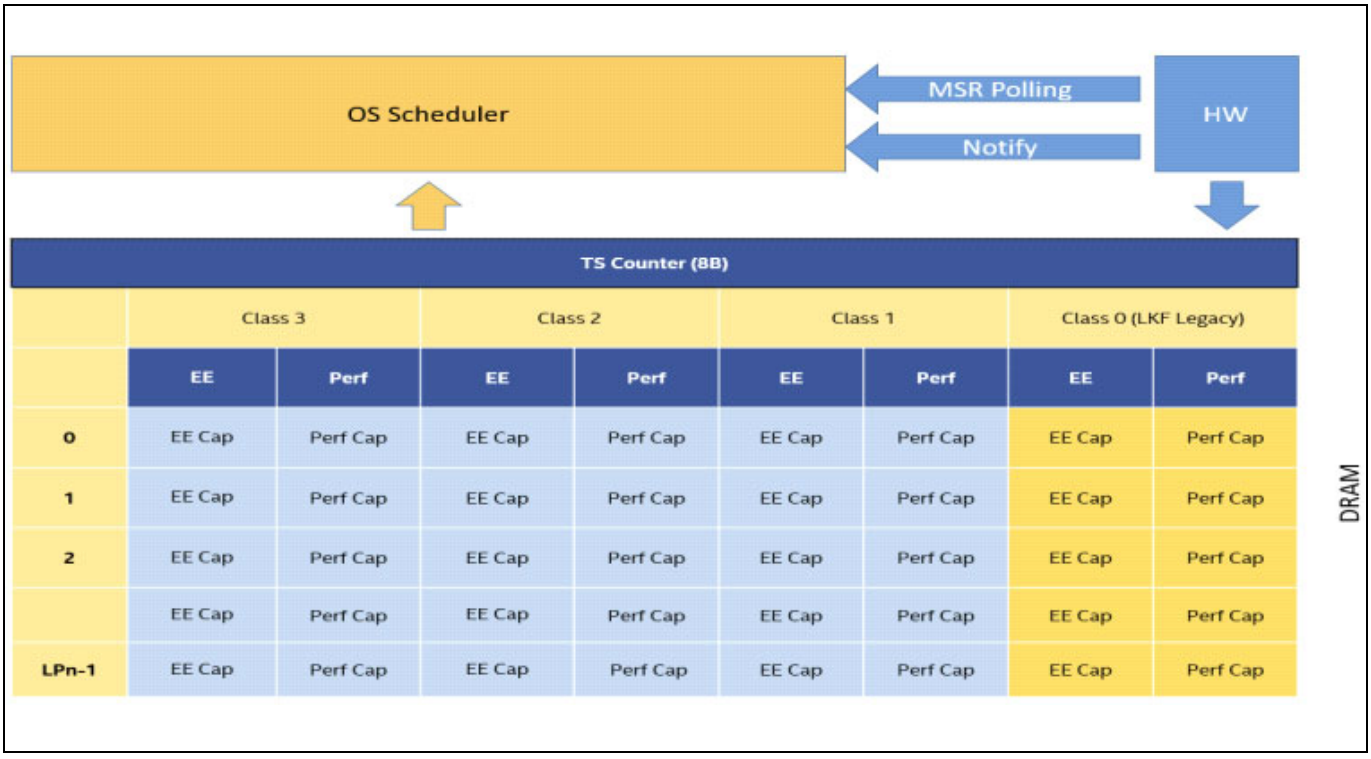

Figure 1-1. Intel Thread Director Interface to the OS

Per Class ID,

- PERF capabilities provide relative performance level of the larger and efficient logical processor (higher values indicate higher performance). The Operating System can sort the threads by core-to-core performance ratio and schedule by core performance order.

- EE capability provides relative energy efficiency level of a logical processor (higher EE values indicate higher energy efficiency requirement for thread).

Hardware determines which class to assign each thread and provides this hint back to the operating system. The various classes indicate performance difference between the P-cores and E-cores. Class 0 represents the true capabilities and utilization thresholds of each core. Classes beyond 0 are model-specific and their meanings are not enumerable to software.

An example platform could internally assign these meanings to the workload classes.

- Class 1 could indicate ISAs (like AVX2-FP32) where P-cores are more performant than E-cores.
- Class 2 could indicate emerging ISAs (such as AI) where P-cores are more performant than E-cores.
- Class 3 could indicate spin-waits and work that does not scale with higher performance. Note that classes were also introduced to track lightweight waits like TPAUSE/UMWAIT so that the OS prioritizes threads with a high amount of time in busy lightweight waits to E-cores for enhanced power gains.

Collaborative Processor Performance Control

The Collaborative Processor Performance Control (CPPC) is defined by ACPI to manage the performance of a logical processor. The CPPC provides several performance values that can be used to determine the performance range for that logical processor relative to other logical processors. Refer to "_CPC (Continuous Performance Control)" in the *Advanced Configuration and Power Interface (ACPI) Specification*, Release 5.0 or later.

These values have historically been the frequency on the platform; however, on a heterogeneous platform this is a performance number that also must consider a scalar value that represents the IPC difference between different core types. As operating systems today use the CPPC for utilization and other metrics, there are scenarios where they must be able to relate the value from HFI back to the values from the CPPC.

CHAPTER 2
WORKLOAD CLASS 0 PERFORMANCE AND CPPC CALCULATIONS

Intel® Thread Director provides a table of values that provides performance and energy efficiency capability, which is not the same as delivered performance, across classes of workloads. The values provide a relative comparison between all logical processors in the system. The operating system can use this information to make intelligent scheduling decisions, for example:

The values provided by the table are otherwise opaque to the operating system and cannot be directly utilized beyond a relative comparison. There is no architectural method to enumerate any information that could convert these values into frequency or any other known type.

The scaling factor used by Intel Thread Director is relatively the same as the scaling factor used in Hardware Controlled Performance States (HWP). The calculation is to take a scaling factor and multiply it by frequency. The BIOS uses HWP values to program the performance fields in the CPPC. However, BIOS reports the nominal performance based on a conservative static frequency whereas the Intel Thread Director uses the current frequency to report performance. The scaling factor used today is based on scaling relative performance capabilities between the different core types.

The BIOS uses this scaling factor in calculating the "CPC.Nominal Performance" in the Continuous Performance Control (_CPC) object of the processor device as shown by Equation 2-1.

Equation 2-1. BIOS Calculation for _CPC.Nominal Performance

$$\text{CPC.Nominal Performance} = \text{Relative Performance Scalar} * \text{Nominal Frequency}^{1}$$

NOTES:

1. The BIOS CPC.Nominal Frequency and the Nominal Frequency are different values but are related via the calculation.

The relative performance scaling value can be extracted from this value using the Nominal Frequency information provided by the same ACPI structure. The calculation used by BIOS for the CPC.Nominal Frequency is shown in Equation 2-2.

Equation 2-2. BIOS Calculation for _CPC.Nominal Frequency

$$\text{CPC.Nominal Frequency} = \text{Nominal Frequency}^{1} * \text{Bus Reference Frequency}$$

NOTES:

1. The BIOS CPC.Nominal Frequency and the Nominal Frequency are different values but are related via the calculation.

These values are provided by the BIOS on a per-logical processor basis as each logical processor has a scaling factor relative to other logical processors in the platform.

Relative Performance Scalar Value

The following calculation shown in Equation 2-3 provides the details on how to obtain the relative performance scalar in a non-architectural manner.

Equation 2-3. Calculating the Relative Performance Scaling Value Using the BIOS _CPC Fields

$$\frac{\text{Logical Processor CPC.Nominal Performance} * \text{Bus Reference Frequency}}{\text{Logical Processor CPC.Nominal Frequency}} = \text{Logical Processor Class 0 Relative Performance Scalar}$$

The Bus Reference Frequency on Intel platforms today is 100 and can be enumerated using CPUID.16H:ECX[15:0] as shown in Figure 2-1. Relative Performance Scalar calculated here may be subject to rounding errors and may lead to errors with frequency calculations.

CPUID.16H -- Processor Frequency Information

CPUID.16H returns information about processor frequency information.
Data is returned from this interface in accordance with the processor's specification and does not reflect actual values. Suitable use of this data includes the display of processor information in like manner to the processor brand string and for determining the appropriate range to use when displaying processor information e.g. frequency history graphs. The returned information should not be used for any other purpose as the returned information does not accurately correlate to information / counters returned by other processor interfaces.
While a processor may support the Processor Frequency Information leaf, fields that return a value of zero are not supported.

- This leaf is valid if MAX_LEAF ≥ 16H.
- This leaf does not contain sub-leaves and provides the same information regardless of the value of ECX.

Leaf 16H Processor Frequency Information

Register	Field Name	Description	Domain
EAX[15:0]	PROCESSOR_BASE_FREQUENCY	Processor Base Frequency (in MHz).	Logical Processor
EAX[31:16]	Reserved	Reserved.	
EBX[15:0]	MAXIMUM_FREQUENCY	Maximum Frequency (in MHz).	Logical Processor
EBX[31:16]	Reserved	Reserved.	
ECX[15:0]	BUS_FREQUENCY	Bus (Reference) Frequency (in MHz).	Logical Processor
ECX[31:16]	Reserved	Reserved.	
EDX[31:0]	Reserved	Reserved.	

Figure 2-1. CPUID Leaf 16H – Processor Frequency Information

The relative performance scaling factor must be determined for each logical processor. This scaling factor can be used with the Performance values from Class 0 in the Hardware Feedback Interface (HFI) table for that logical processor to obtain the current frequency that relates to its current capable capacity.

The equation to determine the logical processor’s current frequency is provided in Equation 2-4 below.

Equation 2-4. Calculating the Capable Frequency of HGS Class 0 Performance

$$\frac{\text{Logical Processor Class 0 Performance} * \text{Bus Reference Frequency}}{\text{Logical Processor Class 0 Relative Performance Scalar}} = \text{Class 0 Capable Frequency}$$

Substituting Nominal Performance for HGS Class 0 Performance

The relationship between these values as shown allows the direct replacement for usages of _CPC.Nominal Performance with the HFI Class 0 Performance value for the logical processor. Instead of providing a static view of the capacity for the logical processor, the HFI value provides the current capacity of that logical processor. This will provide a more realistic current view of the logical processor when considering placement of workloads relative to logical processor utilization than using _CPC.Nominal Performance.

Overclocking Implications

Overclocking has the potential for computations to exceed the 8-bit relative performance values provided by the Hardware Feedback Interface (HFI) table. Today these values will be capped at "< 255" to prevent this overflow. This will create a compression of relative performance in the upper ranges.